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MOTOROLA

AM26LS31

Quad Line Driver with NAND Enabled Three-State Outputs

QUAD EIA–422 LINE DRIVER WITH THREE–STATE OUTPUTS

SEMICONDUCTOR TECHNICAL DATA

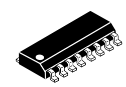
The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA–422 Standard and Federal Standard 1020.

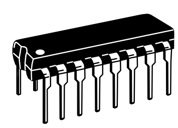
The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 EIA–422 driver.

The high impedance output state is assured during power down.

- Full EIA–422 Standard Compliance
- Single +5.0 V Supply
- Meets Full V_O = 6.0 V, V_{CC} = 0 V, I_O < 100 µA Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

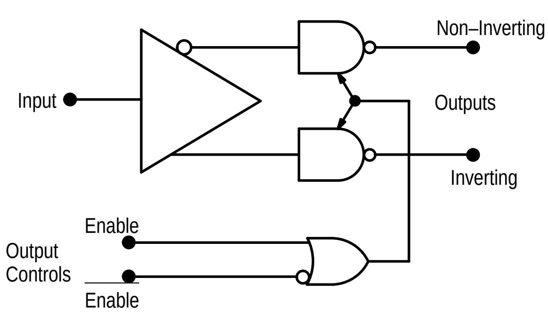
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



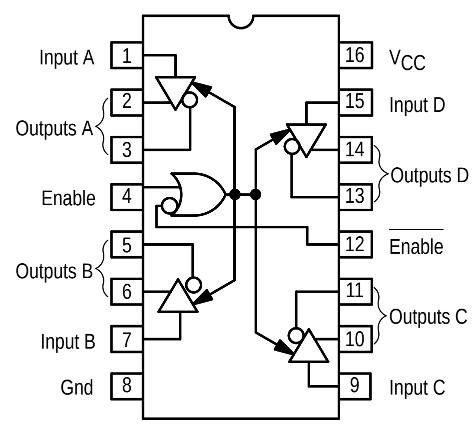


PC SUFFIX
PLASTIC PACKAGE
CASE 648

Representative Block Diagrams



PIN CONNECTIONS



TRUTH TABLE			
Input	**Control Inputs (E/E)**	**Non–Inverting Output**	**Inverting Output**
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third–State (High Impedance)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
AM26LS31PC	T_A = 0 to +70°C	Plastic DIP
MC26LS31D*		SO–16

* Note that the surface mount MC26LS31D device uses the same die as in the plastic DIP AM26LS31DC device, but with an MC prefix to prevent confusion with the package suffix.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to + 70	°C
Operating Junction Temperature Range	T_J	150	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}	–	–	– 360	µA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 7.0 V)	I_{IH}	 – –	 – –	 + 20 + 100	µA
Input Clamp Voltage (I_{IK} = – 18 mA)	V_{IK}	–	–	– 1.5	V
Output Voltage – Low Logic State (I_{OL} = 20 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = –20 mA)	V_{OH}	2.5	–	–	V
Output Short Circuit Current (V_{IH} = 2.0 V) Note 1	I_{OS}	– 30	–	– 150	mA
Output Leakage Current – Hi–Z State (V_{OL} = 0.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V) (V_{OH} = 2.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(E)}$ = 2.0 V)	$I_{O(Z)}$	 – –	 – –	 – 20 + 20	µA
Output Leakage Current – Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = – 0.25 V, V_{CC} = 0 V)	$I_{O(off)}$	 – –	 – –	 + 100 – 100	µA
Output Offset Voltage Difference, Note 2	$V_{OS} - \overline{V_{OS}}$	–	–	± 0.4	V
Output Differential Voltage, Note 2	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference, Note 2	$\lvert\Delta V_{OD}\rvert$	–	–	± 0.4	V
Power Supply Current (Output Disabled) Note 3	I_{CCX}	–	60	80	mA

NOTES: 1. Only one output may be shorted at a time.
2. See EIA Specification EIA–422 for exact test conditions.
3. Circuit in three–state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 – –	 – –	 20 20	ns
Output Skew		–	–	6.0	ns
Propagation Delay – Control to Output (C_L = 10 pF, R_L = 75 Ω to Gnd) (C_L = 10 pF, R_L = 180 Ω to V_{CC}) (C_L = 30 pF, R_L = 75 Ω to Gnd) (C_L = 30 pF, R_L = 180 Ω to V_{CC})	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 – – – –	 – – – –	 30 35 40 45	ns

Figure 1. Three–State Enable Test Circuit and Waveforms

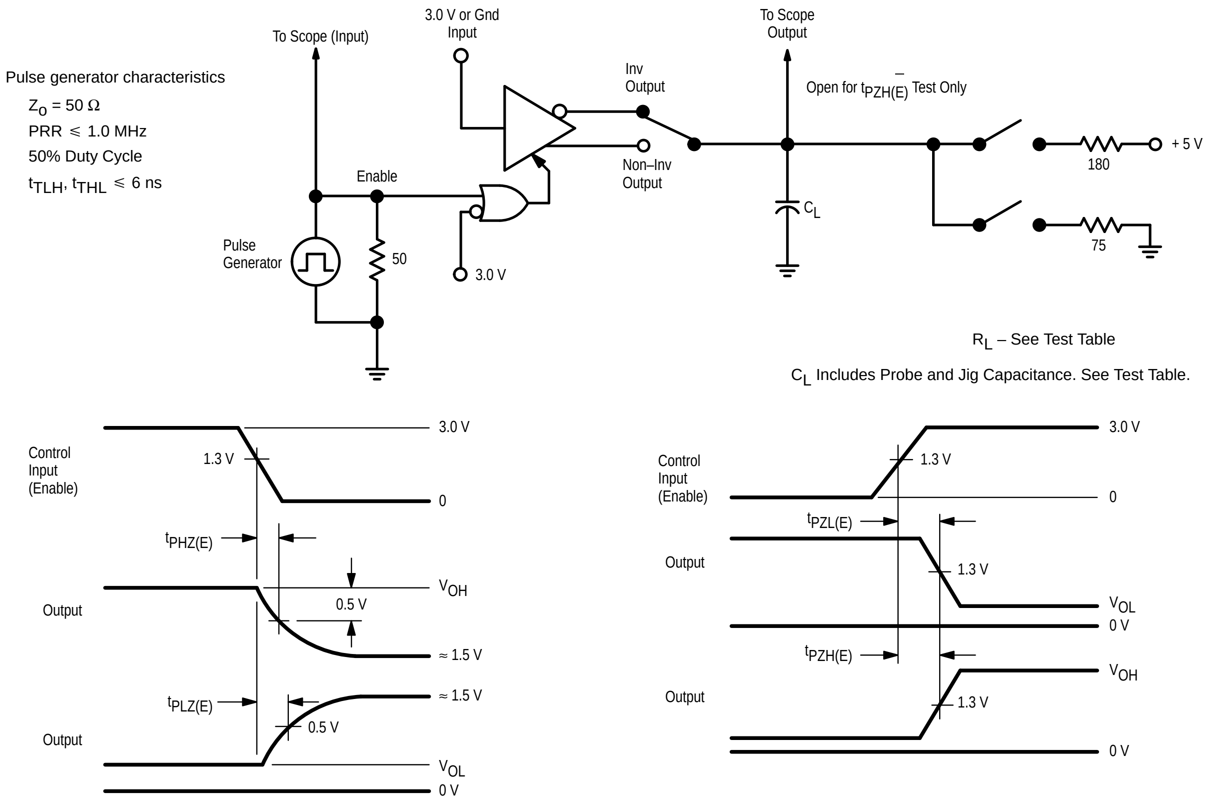
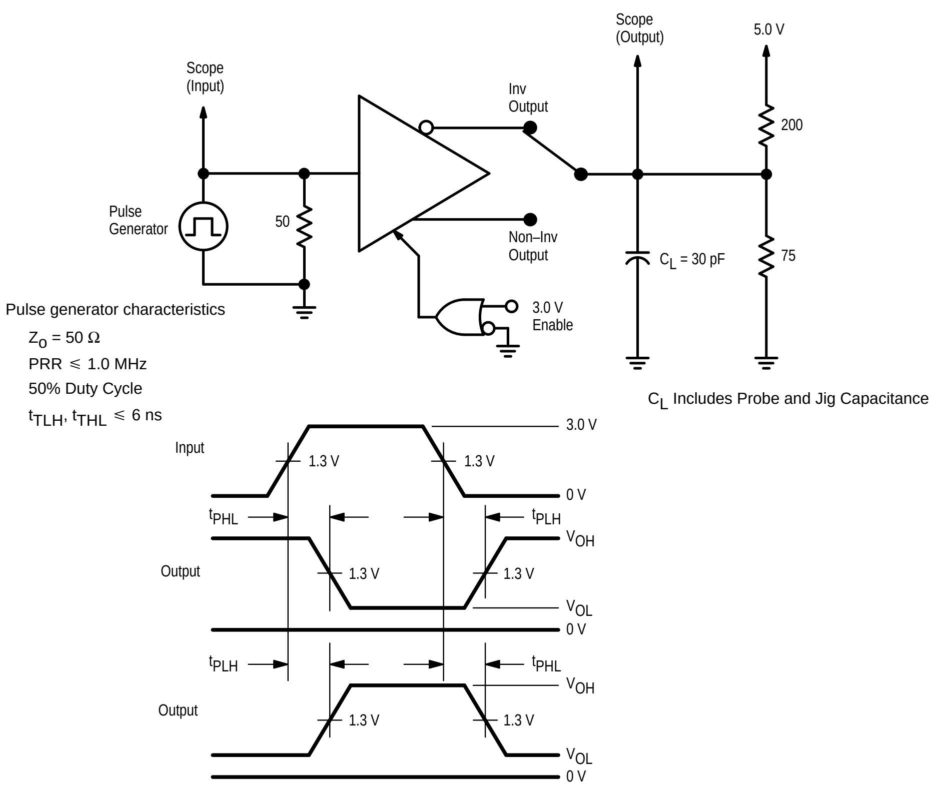
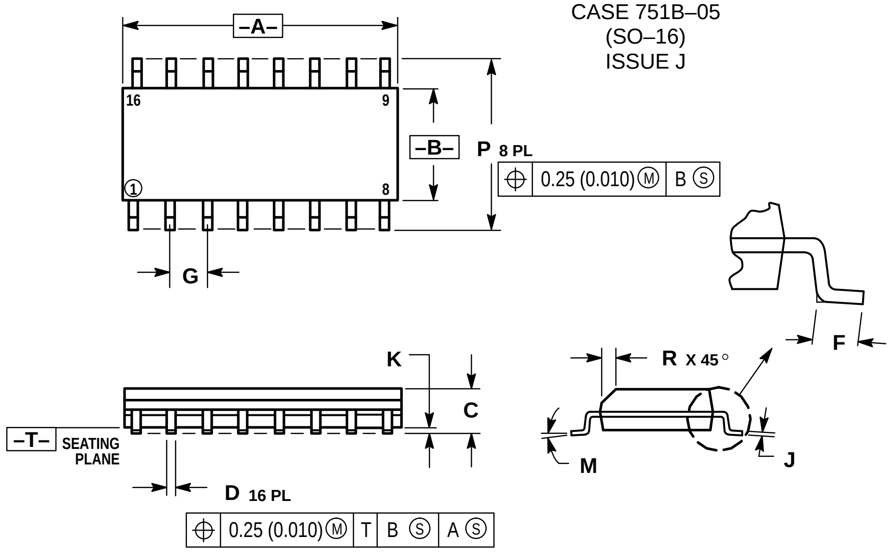


Figure 2. Propagation Delay Times Input to Output Waveforms and Test Circuit



OUTLINE DIMENSIONS

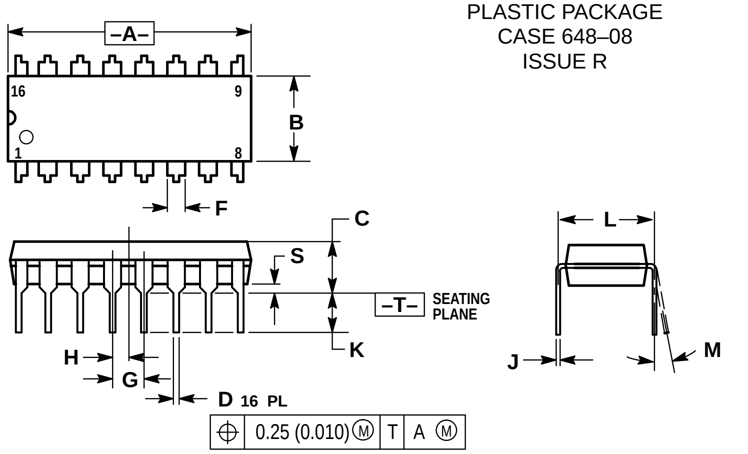
D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PC SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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