PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

M54965ASP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

DESCRIPTION

The M54965ASP is a semiconductor integrated circuit consisting of an oxide-film separated ECL/I^2L PLL frequency synthesizer. A prescaler and PLL capable of withstanding operating at a maximum frequency of 1.0GHz are housed in a single chip.

FEATURES

- Built-in prescaler with input amplifier f_{max}=1.0GHz
- Serial data input
- Fine tuning capability (31.25KHz/step)
- Built-in band output
- 5V single power supply

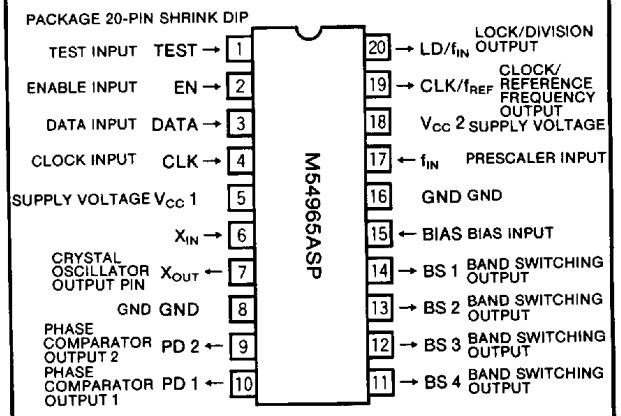
APPLICATION

TV and VTR tuners

FUNCTION

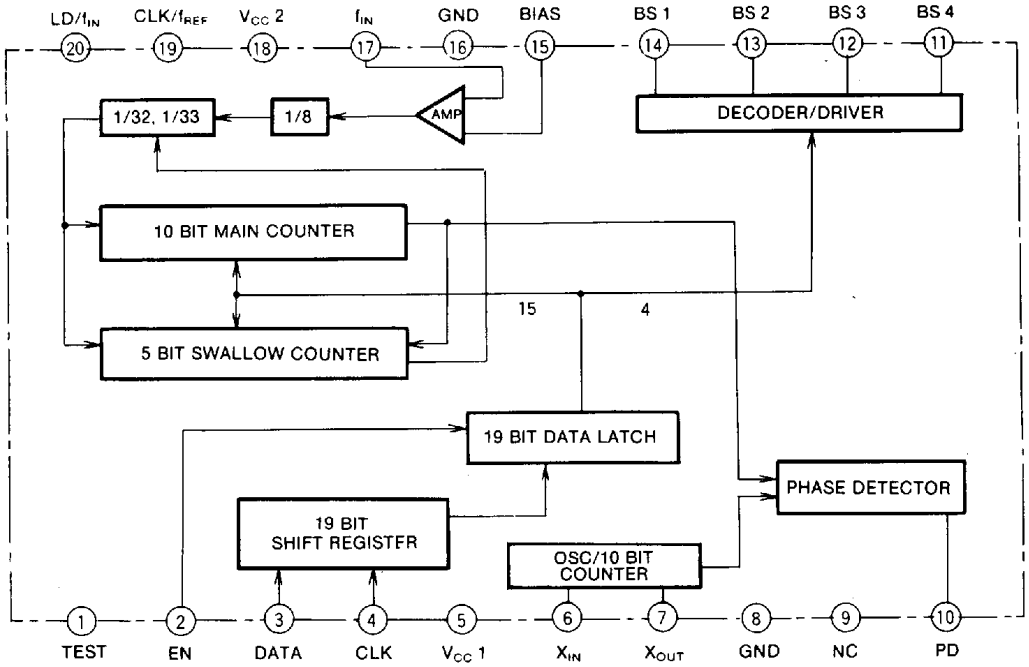
The M54965ASP is a PLL frequency synthesizer IC for TV applications. The prescaler employs emitter-coupled logic, and the PLL, I^2L. The maximum operating frequency of the prescaler is 1.0GHz. The first stage is a fixed 1/8 2-modulus prescaler and the second stage is a 1/32, 1/33 2-modulus prescaler. The PLL consists of a 4MHz crystal oscillator, a 10-bit reference frequency divider, a programmable divider (a 10-bit M counter and a 5-bit S counter), a phase comparator, and a lock detector. Four band switching circuits are also provided.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

BLOCK DIAGRAM



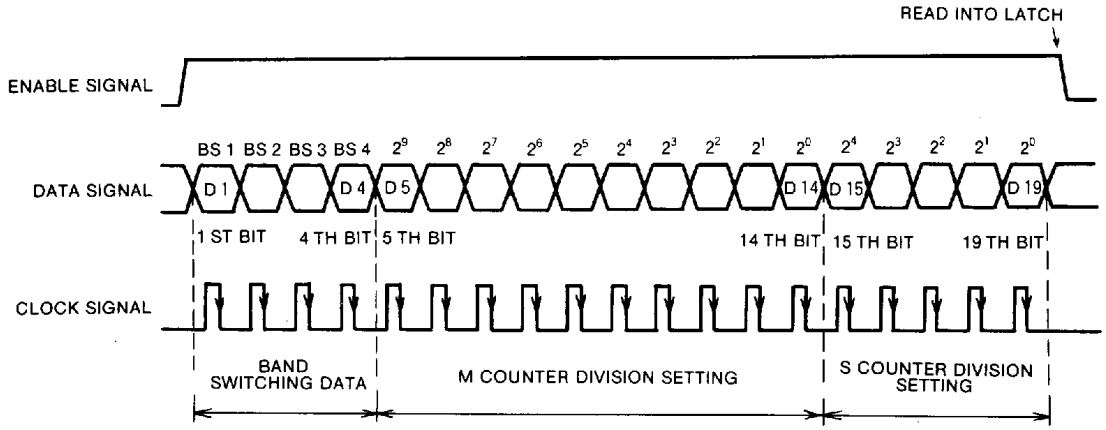
SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

PIN DESCRIPTION

Pin number	Symbol	Pin name	Functional description
5 18	$V_{CC}1$ (IIL) $V_{CC}2$ (ECL)	Supply voltage 1 (I^2L) Supply voltage 2 (ECL)	Prescaler supply voltage pin 5.0+0.5V is applied I_2L supply voltage pin 5.0+0.5V is applied
8 16	GND 1 (IIL) GND2(ECL)	GND 1 (I^2L) GND 2 (ECL)	Connect to 0V Connect to 0V
6 7	X_{IN} X_{OUT}	Crystal oscillator output pin	4.0MHz crystal oscillator is connected.
17 15	f_{IN} BIAS	Prescaler input pin Bias pin	Prescaler input pin, V, C, O frequency is applied Prescaler bias pin, capacitance of 1000pF is inserted between GND and this pin.
2	ENABLE	Enable input	Normally set low. When high, 19-bit data is read into the shift register. When it drops from high to low, the contents of the shift registers are read into the latch.
4	CLOCK	Clock input	Data is read into shift register at the falling edge of the clock signal.
3	DATA	Data input	Programmable divider division setting input
19	CLK/f_{REF}	Clock/reference frequency output	When the TEST input is low, the 500kHz clock frequency (CLK) is output. When TEST is high, the reference frequency output f_{REF} is output. The reference frequency is 3.90625kHz. (Open-collector output)
20	LD/f_{IN}	Lock detector/division output	When the TEST input is low, the lock detector output (LD) is selected ; when TEST is high, the programmable divider output (f 1/N) is selected. The lock detector output is normally high and becomes low for a period corresponding to the phase difference between f_{REF} and f 1/N. (Open collector output)
1	TEST	TEST input	This pin is used for testing and is normally set low. When set high, f_{REF} and f 1/N outputs are selected for CLK/f_{REF} and LD/f 1/N, and the phase comparator output enters the high-impedance state.
10 9	PD 1 PD 2	Phase comparator output 1 Phase comparator output 2	When the phase programmable divider output (f 1/N) is advanced with respect to the reference frequency (f_{REF}), this output becomes high, and when the programmable divider output is delayed, it becomes low. When the two are in sync, this output enters the high-impedance state.
14 13 12 11	BS 1 BS 2 BS 3 BS 4	Band switching output pin	Open-collector outputs are used at all four band switching output pins. When the band switching data is high, the output is ON, and when low, the output is OFF.

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

How to set the dividing ratio of programmable divider and select the band switching output
The output is read into the latch at the falling edge of enable signal, as shown below.



Total divisor N is given by the following formulas in addition to the prescaler used in the previous stage.

$N = 8(32M+S)$

M : 10-bit main counter division
S : 5-bit swallow counter division

The M and S counters are binary and the possible ranges of division are as follows.

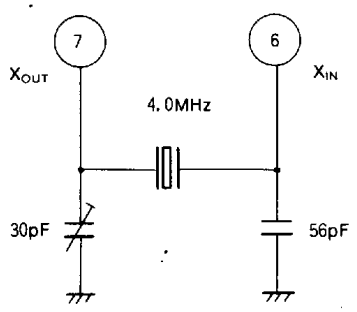
$32 \leqq M \leqq 1023$
$0 \leqq S \leqq 31$

The range of divisors N is 8, 136 and 192~262.
The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO} = f_{REF} \times N$
$= 3.90625 \times 8(32M+S)$
$= 31.25(32M+S)(kHz)$

Therefore, the range of tuning frequencies is 32MHz — 1000MHz.

CRYSTAL OSCILLATOR CONNECTION DIAGRAM



CRYSTAL OSCILLATOR CHARACTERISTICS

Actual resistance : less than 50Ω
Load capacitance : 20pF

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

ABSOLUTE MAXIMUM RATINGS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
VI	Input voltage	Do not exceed supply voltage (V_{CC})	6.5	V
V_O 1	Output voltage (1)	Do not exceed PD output supply voltage	5.5	V
V_O 2	Output voltage (2)	Do not exceed output supply voltage (V_{CC}) other than mentioned above	6.5	V
VBD	Output withstanding voltage	Band switching switch	13.5	V
P_d	Power dissipation		650	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Conditions	Limits	Unit
V_{CC}	Supply voltage			4.5∼5.5	V
fopr 1	Operating frequency (1)		Crystal oscillator	4.0	MHz
fopr 2	Operating frequency (2)		f_{IN} input	80∼1000	MHz
I_{OL}	Low-level output current	19 20		0∼5	mA
IBDL	Low-level band output current	11 12 13 14		0∼1	mA

ELECTRICAL CHARACTERISTICS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage		1, 2, 3, 4		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		1, 2, 3, 4				0.7	V
I_{IH}	High-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=2.7V			50	μA
I_{IL} 1	Low-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=0.4V		−100	−200	μA
I_{IL} 2	Low-level input current 2		2	V_{CC}=5.5V, V_I=0.4V		−550	−900	μA
I_{IC}	Input clamp voltage		1, 2, 3, 4	V_{CC}=4.5V, V_{IC}=1.0mA		−1.3	−1.8	V
V_{OH}	High-level output voltage	PD output	10	V_{CC}=4.5V, I_{OH}=−1.0mA	2.5	3.0		V
V_{OL} 1	Low-level output voltage	PD output	10	V_{CC}=4.5V, I_{OL}=−1.0mA		0.2	0.4	V
V_{OL} 2		Other than above	19, 20	V_{CC}=4.5V, I_{OL}=5mA		0.3	0.5	V
I_{OLK} 1	Output leakage current	PD output	10	V_{CC}=5.5V, V_O=0.5∼4.8V	−1.0		+1.0	μA
I_{OLK} 2		Other than above	19, 20	V_{CC}=5.5V, V_O=5.5V	−10		+10	μA
I_{CC}	Supply current		5, 18	V_{CC}=5.5V		70	100	mA

Typical values are at V_{CC}=5.0V, T_a=25℃.

SWITCHING CHARACTERISTICS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
f_{opr}	Prescaler operating frequency	17	V_{CC}=4.5∼5.5V V_{IN}=V_{INmin}∼V_{INmax}		80		1000	V
V_{IN}	Operating input voltage	17	80∼150MHz 150∼1000MHz	V_{CC}=4.5∼5.5V	−20 −27		4 4	dBm
t_{PWC}	Clock pulse width	4	V_{CC}=4.5∼5.5V		10			μA
$t_{SU(D)}$	Data setup time	3			10			μA
$t_{H(D)}$	Data hold time	3			10			μA
$t_{SU(E)}$	Enable setup time	2			20			μA
$t_{H(E)}$	Enable hold time	2			20			μA
t_{INT}	Enable data interval time	2, 3			10			μA
t_r	Rising time	2, 3, 4					1	μA
t_f	Falling time	2, 3, 4					1	μA

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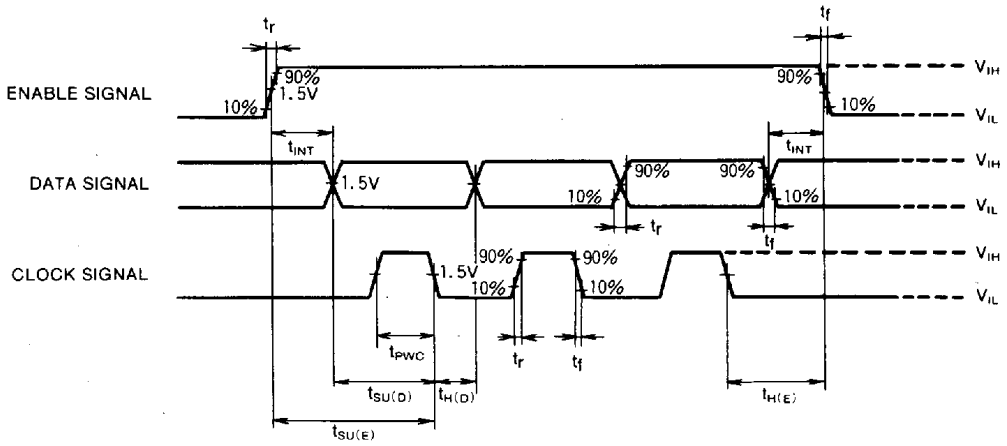
TIMING DIAGRAM



APPLICATION EXAMPLE