# HM6147H Series———Maintenance Only

4096-word x 1-bit High Speed CMOS Static RAM

■FEATURES
- High Speed: Fast Access Time 35ns/45ns/55ns (max.)
- Low Power Standby and Low Power Operation, Standby: 100µW (typ.)/5µW (typ.) (L-version), Operation: 150mW typ.
- Single 5V Supply and High Density 18 Pin Package
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
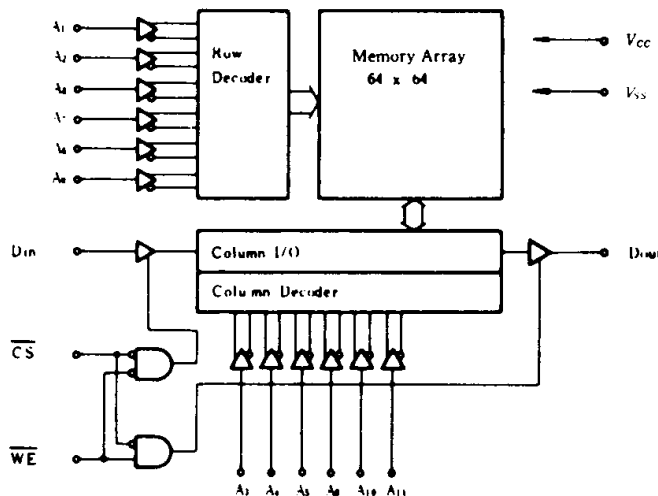- Capability of Battery Back Up Operation (L-version)

(DP-18)

■PIN ARRANGEMENT

(Top View)
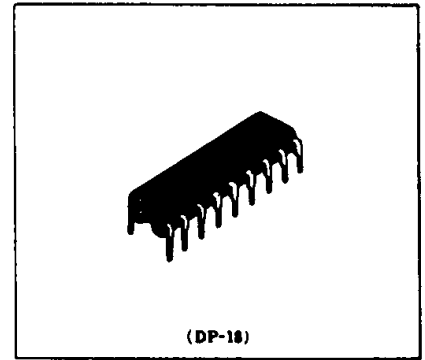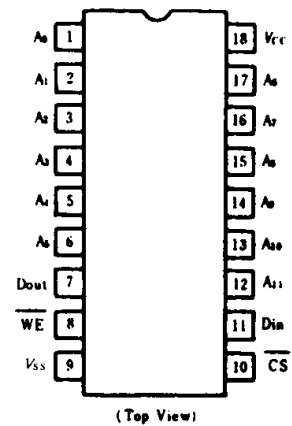
■ORDERING INFORMATION

Type No.	Access Time	Package
HM6147HP-35	35ns	
HM6147HP-45	45ns	
HM6147HP-55	55ns	300mil 18pin Plastic DIP
HM6147HLP-35	35ns	
HM6147HLP-45	45ns	
HM6147HLP-55	55ns	

■BLOCK DIAGRAM

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to V_{SS}	V_T	-0.5^{*1} to $+7.0$	V
DC Output Current	I_o	20	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature under bias	$T_{stg(bias)}$	-10 to $+85$	°C
Storage Temperature	T_{stg}	-55 to $+125$	°C

Note) *1 -3.5V for pulse width $\leq$ 20ns

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■RECOMMENDED DC OPERATING CONDITIONS $(0°C \leq Ta \leq 70°C)$

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5^{*1}	—	0.8	V

Note) *1. $-3.0V$ for pulse width $\leq 20ns$

■DC AND OPERATING CHARACTERISTICS $(0°C \leq Ta \leq 70°C, \; V_{CC}=5V\pm10\%, \; V_{SS}=0V)$

Parameter	Symbol	Test Condition	min	typ*2	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5V, \; V_{SS}$ to V_{CC}	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}, \; V_{out}=V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current (1)	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current (2)	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current (1)	I_{SB}	$\overline{CS}=V_{IH}, \; V_{CC}=$ Min to Max	—	8	20	mA
			—	5^{*3}	15^{*3}	
Standby Power Supply Current (2)	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V,$ $V_{IN} \geq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	20	800	μA
			—	1^{*3}	100^{*3}	
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.40	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Notes) *1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute.
    *2. Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and Specified loading.
    *3. This characteristics are guaranteed only for L-version.

■CAPACITANCE $(Ta=25°C, \; f=1.0MHz)$

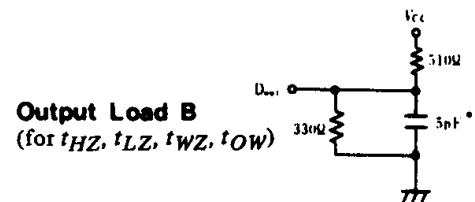| Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	6	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS $(Ta = 0$ to $+70°C, \; V_{CC} = 5V \pm 10\%)$
●AC TEST CONDITIONS

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels: 1.5V (HM6147H-35)
   0.8 to 2.0V (HM6147H-45/55)
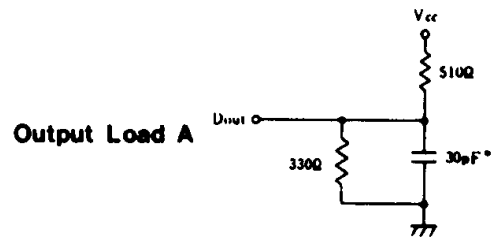
Output Load A

* Including scope & jig capacitance

Output Load B
(for $t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}$)

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● **READ CYCLE**

Parameter	Symbol	HM6147H-35		HM6147H-45		HM6147H-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns	(1)
Address Access Time	t_{AA}	—	35	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	(2), (3), (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	20	ns	

● **TIMING WAVEFORM OF READ CYCLE NO.1** [4] [5]
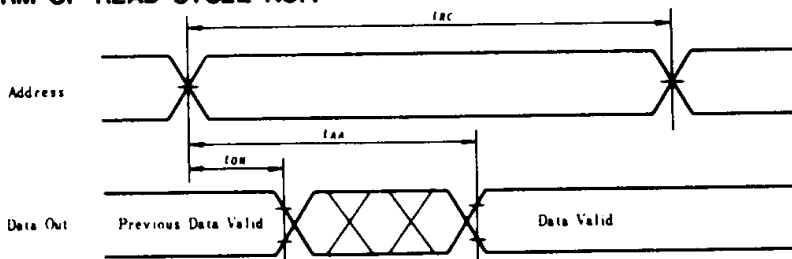

● **TIMING WAVEFORM OF READ CYCLE NO.2** [4] [6]
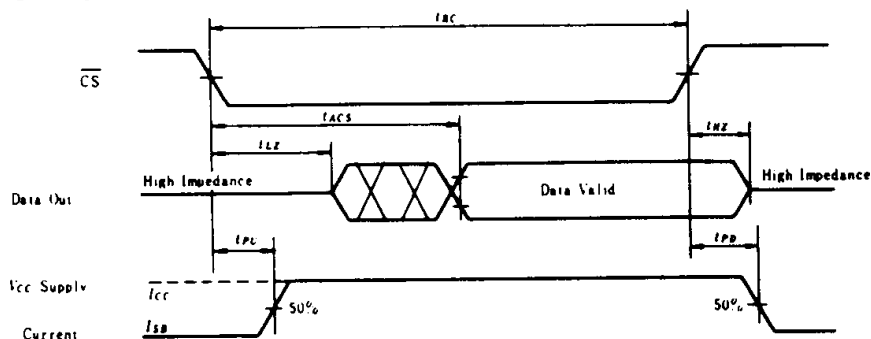
Notes: 1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, $\overline{CS}=V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

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● WRITE CYCLE

Parameter	Symbol	HM6147H-35		HM6147H-45		HM6147H-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns	(2)
Chip Selection to End of Write	t_{CW}	35	—	45	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	10	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	(3), (4)

● TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)
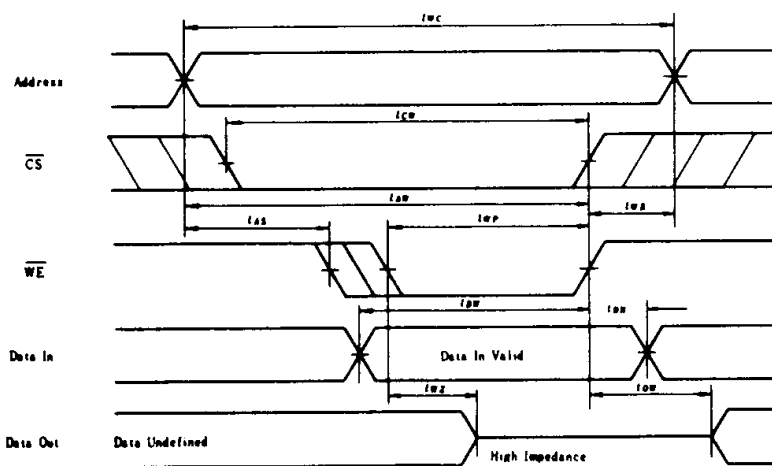
● TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)
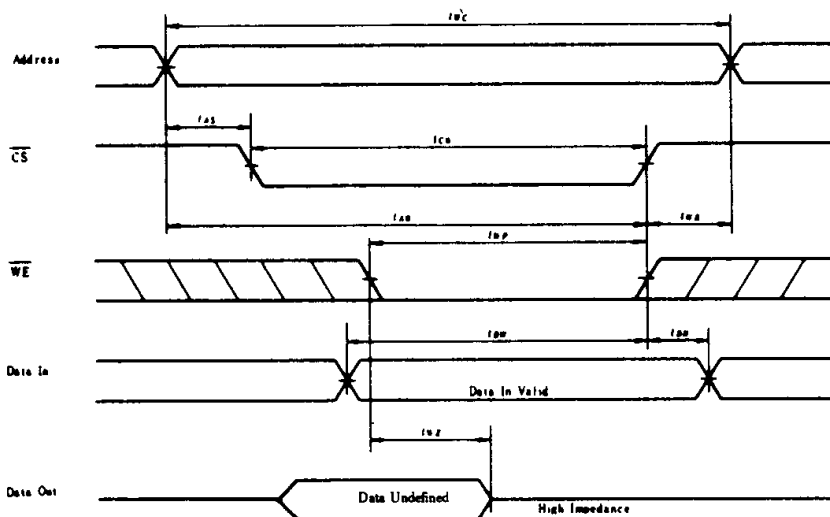
Notes: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.
5. $\overline{CS}$ or $\overline{WE}$ is high for address transition.

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■LOW V$_{cc}$ DATA RETENTION CHARACTERISTICS ($Ta=0℃$ to $+70℃$)

This characteristics are guaranteed only for L-version.

Item	Symbol	Test Condition	min	typ	max	Unit
V$_{cc}$ for Data Retention	V$_{DR}$	$\overline{CS} \geqq V_{cc}-0.2V$ $V_{IN} \geqq V_{cc}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I$_{CCDR}$	$V_{cc}-3.0V$, $\overline{CS} \geqq 2.8V$ $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	50	μA
Chip Deselect to Data Retention Time	t$_{CDR}$	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t$_R$		t_{RC}*1	—	—	ns

Note) *1. t_{RC} = Red Cycle Time.

●LOW V$_{cc}$ DATA RETENTION WAVEFORM
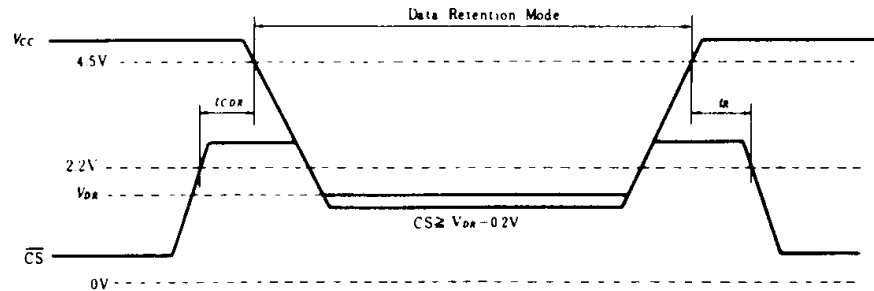
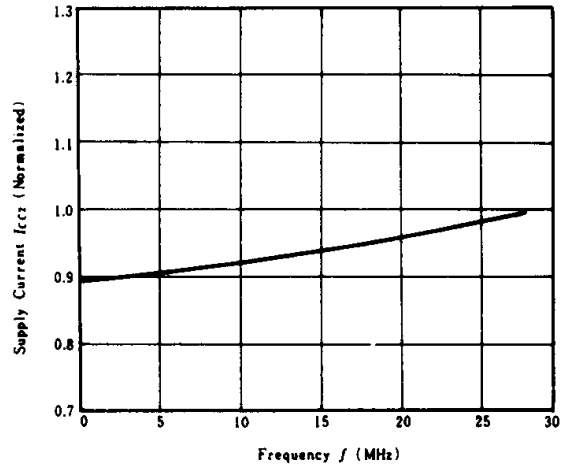## ACCESS TIME VS. SUPPLY VOLTAGE
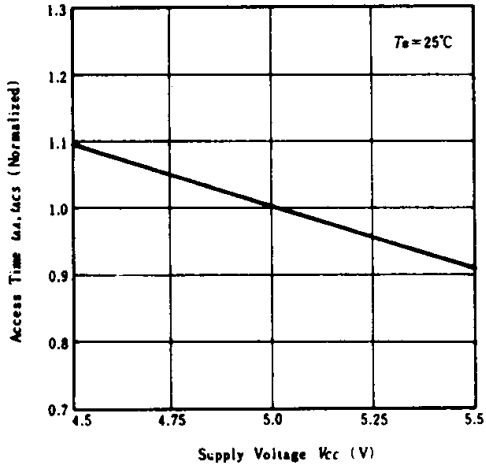
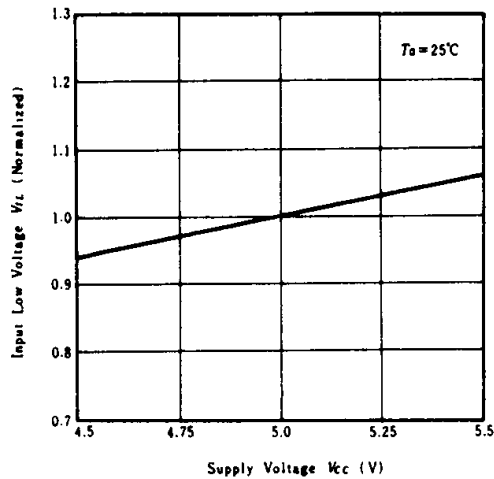## ACCESS TIME VS. AMBIENT TEMPERATURE
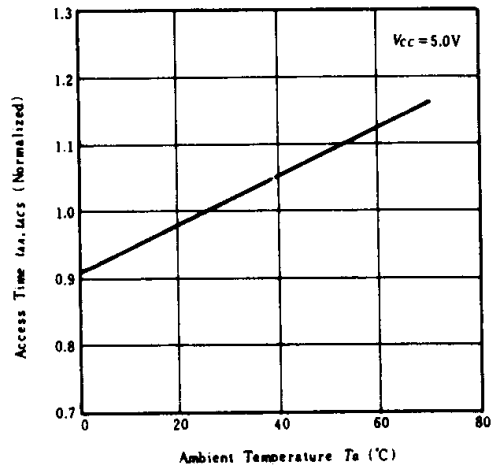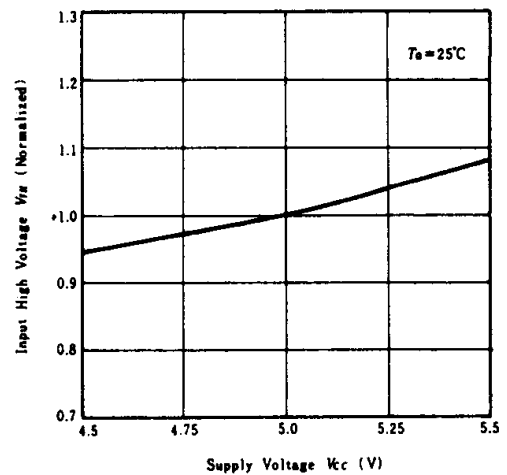

ACCESS TIME VS. LOAD CAPACITANCE
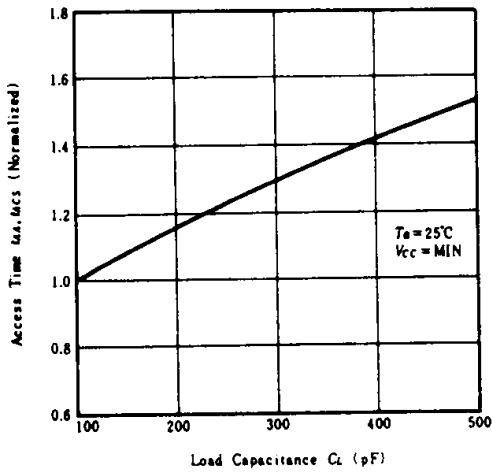
SUPPLY CURRENT VS. FREQUENCY

INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE

INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE

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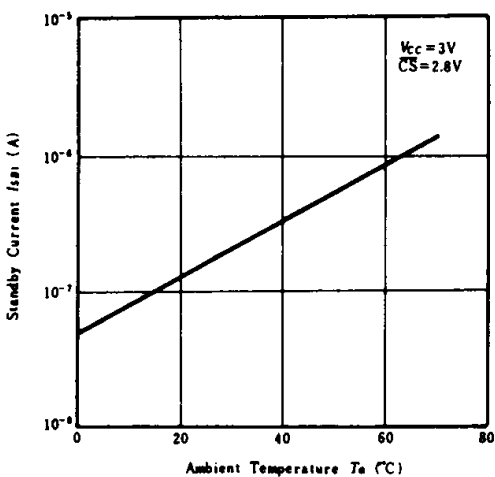Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

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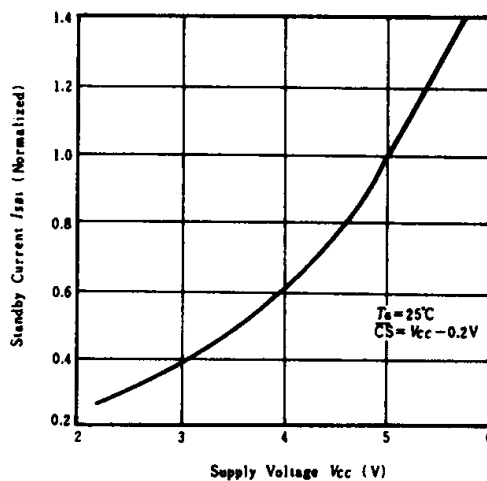## OUTPUT CURRENT VS. OUTPUT VOLTAGE
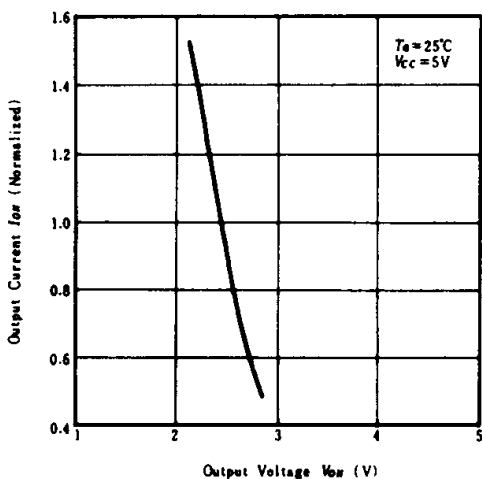
OUTPUT CURRENT VS. OUTPUT VOLTAGE
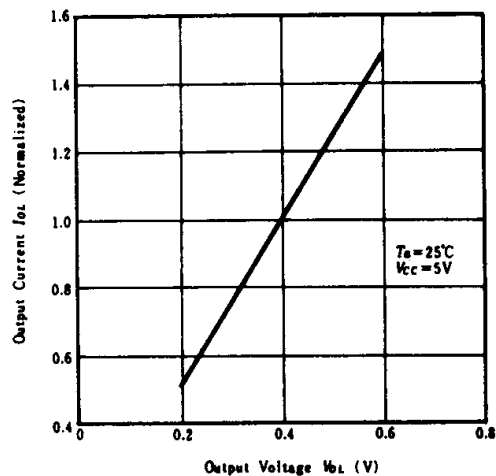
STANDBY CURRENT VS. AMBIENT TEMPERATURE

STANDBY CURRENT VS. SUPPLY VOLTAGE

STANDBY CURRENT VS. INPUT VOLTAGE