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32,768 WORD × 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC55328P/J is a 262,144 bits high speed static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55328P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

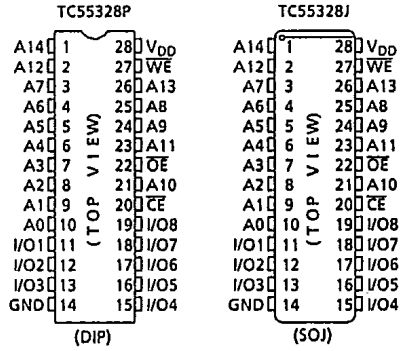
The TC55328P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55328P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time :
  - TC55328P/J-17 17ns(MAX.)
  - TC55328P/J-20 20ns(MAX.)
  - TC55328P/J-25 25ns(MAX.)
  - TC55328P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation : TC55328P/J-17 140mA(MAX.)
  - TC55328P/J-20 140mA(MAX.)
  - TC55328P/J-25 140mA(MAX.)
  - TC55328P/J-35 120mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - −17 : 5V±5%
  - −20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package TC55328P : DIP28−P−300B
  - TC55328J : SOJ28−P−300A

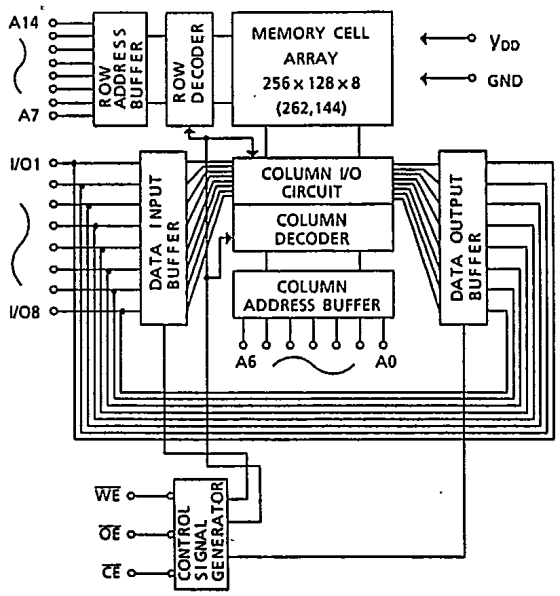
PIN CONNECTION



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



TC55328P/J-17, TC55328P/J-20
TC55328P/J-25, TC55328P/J-35

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MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	−17	4.75	5.0	5.25	V
		−20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		−0.5 *	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, −17 : V_{DD} = 5V ± 5%, −20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}			−	−	±1	μA
I_{DDO}	Operating Current	tcycle = Min cycle	V_{DD} = 5.25V	−17	−	−	140	mA
		$\overline{CE}$ = V_{IL}	V_{DD} = 5.5V	−20	−	−	140	
		Other Input = V_{IH}/V_{IL}		−25	−	−	140	
				−35	−	−	120	
I_{DDS1}	Standby Current	tcycle = Min cycle	V_{DD} = 5.25V	−17	−	−	20	mA
		$\overline{CE}$ = V_{IH}	V_{DD} = 5.5V	−20				
		Other Input = V_{IH}/V_{IL}		−25				
				−35				
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V or 0.2V			−	−	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

TC55328P/J-17, TC55328P/J-20
TC55328P/J-25, TC55328P/J-35

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AC CHARACTERISTICS (Ta = 0~70°C (1), -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55328P/J-17		TC55328P/J-20		TC55328P/J-25		TC55328P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	-	20	-	25	-	35	-	ns
t_{ACC}	Address Access Time	-	17	-	20	-	25	-	35	
t_{CO}	$\overline{CE}$ Access Time	-	17	-	20	-	25	-	35	
t_{OE}	$\overline{OE}$ Access Time	-	9	-	10	-	12	-	15	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	5	-	
t_{COE}	Output Enable Time from $\overline{CE}$	5	-	5	-	5	-	5	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	10	-	10	-	10	-	15	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	0	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	8	-	8	-	10	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	17	-	20	-	25	-	35	

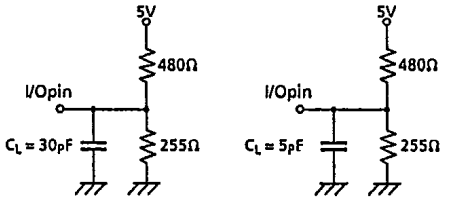
WRITE CYCLE

SYMBOL	PARAMETER	TC55328P/J-17		TC55328P/J-20		TC55328P/J-25		TC55328P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	-	20	-	25	-	35	-	ns
t_{CW}	Chip Enable to End of Write	13	-	13	-	15	-	20	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	13	-	13	-	15	-	20	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	10	-	10	-	12	-	15	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	0		
t_{OEW}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	8	-	8	-	10	-	15	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig.1

Fig.1



(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{ODW})

TC55328P/J-17, TC55328P/J-20
TC55328P/J-25, TC55328P/J-35

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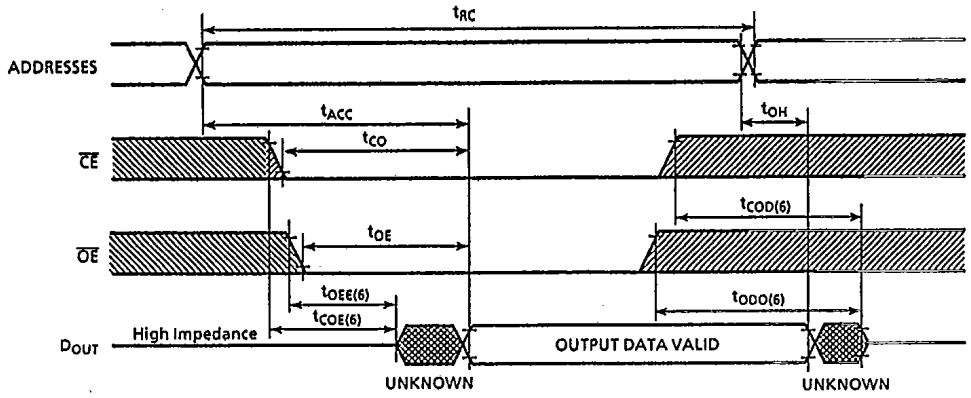
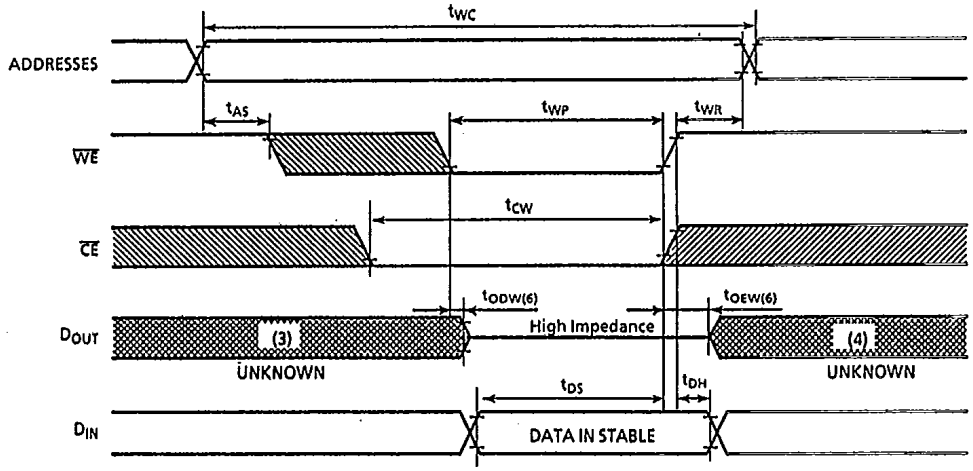
TIMING WAVEFORMS

READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



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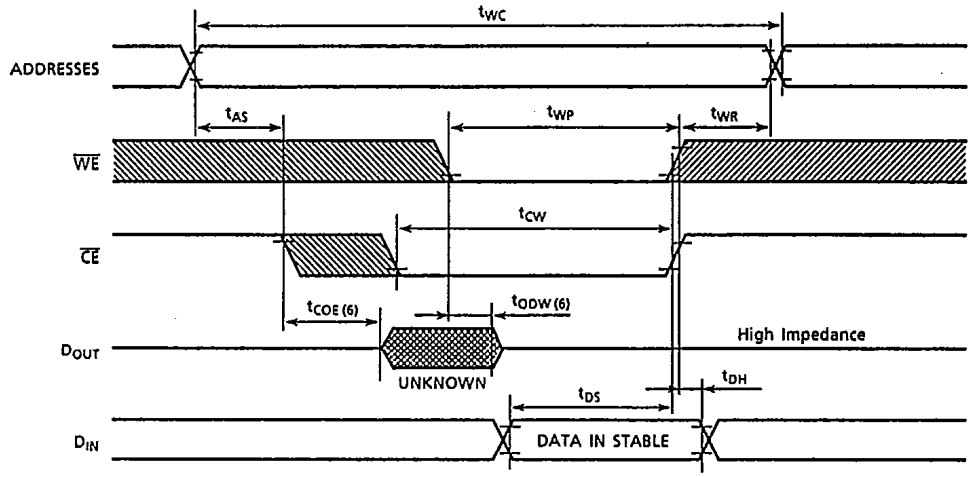
WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

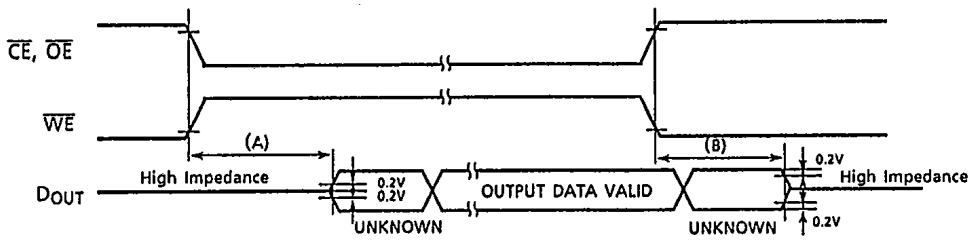
4 Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



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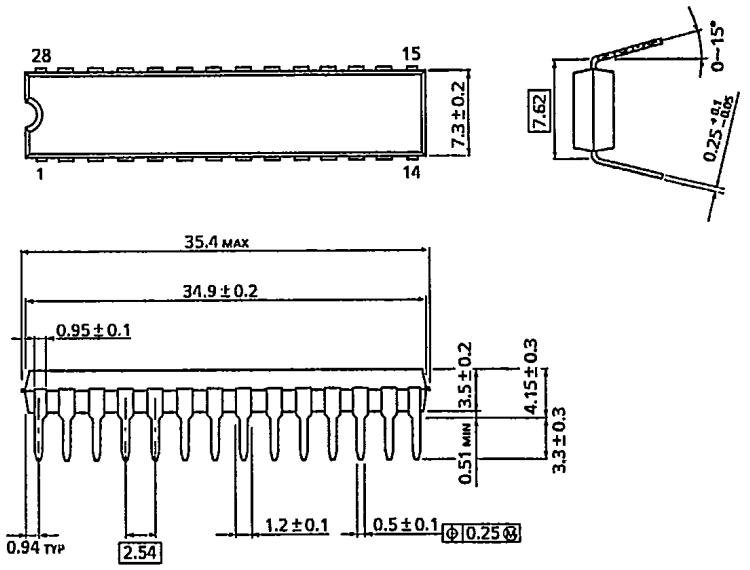
OUTLINE DRAWINGS

Plastic DIP (DIP28 – P – 300B)

UNIT in mm



WEIGHT : 2.03g (Typ.)

TC55328P/J-17, TC55328P/J-20
TC55328P/J-25, TC55328P/J-35

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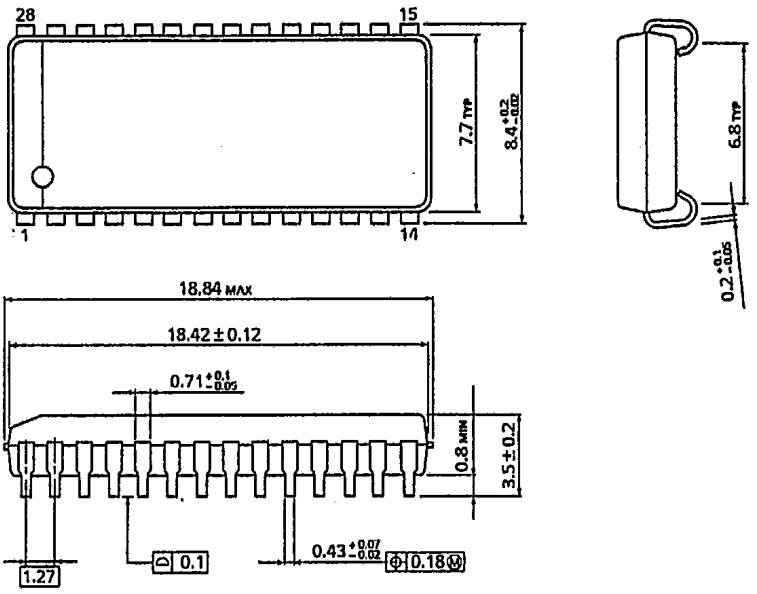
OUTLINE DRAWINGS

Plastic SOJ (SOJ28-P-300A)

UNIT in mm



WEIGHT : 0.83g (Typ.)