HM53051 Series

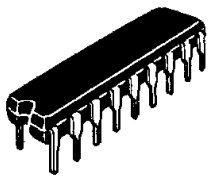
262,144-Word x 4-Bit Frame Memory

■ DESCRIPTION

HM53051P is a 262,144-word x 4-bit frame memory, using the most advanced 1.3 μm CMOS processes. It performs serial access by an internal address generator.

It offers a high-speed cycle time of 45 ns or 60 ns (min). As input data and output data can be written or read in any cycle, synchronized with a system clock, and the delay between data read/write operations is freely settable. Y/C separation and frozen pictures can be realized easily in 4 fsc NTSC digital TV or VCR systems. Also, it enables random access in 32-word x 4-bit data block. With this function, picture in picture or a multiplexed picture can be displayed with ease.

HM53051P Series



3DDP18B

(DP-18B)

■ FEATURES

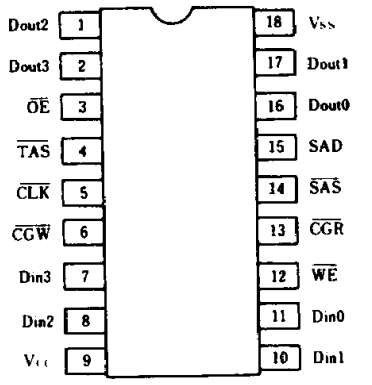
- 262,144-Word x 4-Bit Serial Access Memory
- Organized with Dual Ports
  - Serial Input ..... x 4-Bit
  - Serial Output ..... x 4-Bit
- High Speed
  - Read/Write Cycle Time ..... 45 ns/60 ns (min)
  - Access Time ..... 35 ns/40 ns (max)
- Semi-Synchronous Read/Write Cycle
- Low Power
  - Active: 200 mW (typ)
- Random Access in 32-Word x 4-Bit Blocks
- External Refresh Control is Unnecessary

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53051P-45 HM53051P-60	45 ns 60 ns	300 mil 18-pin Plastic DIP (DP-18B)

■ PIN OUT

HM53051P Series



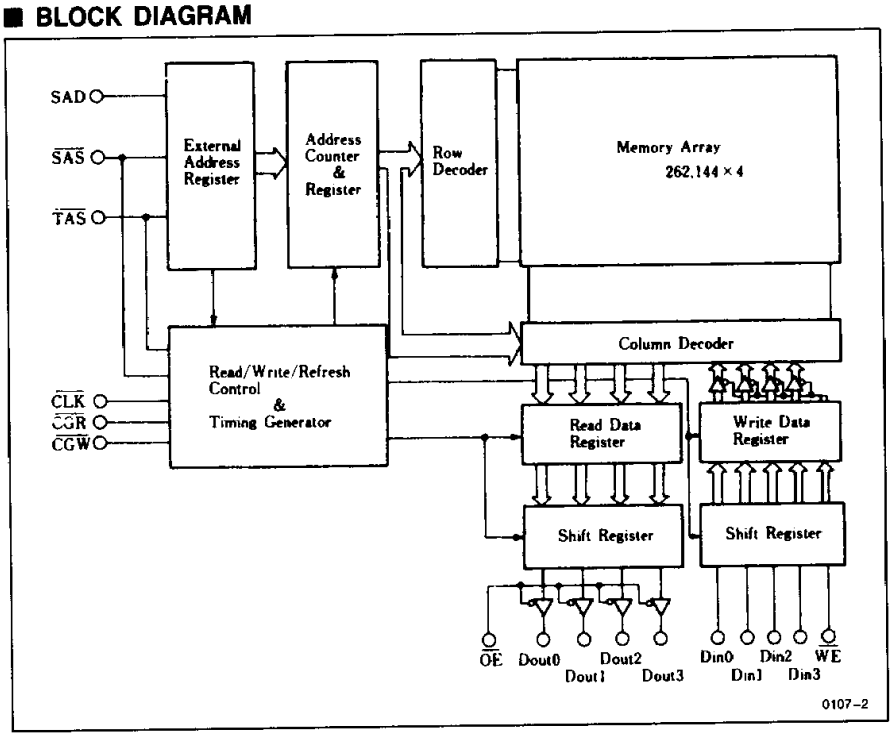
0107-1

(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_{in}	Data Input
D_{out}	Data Output
$\overline{OE}$	Output Enable
$\overline{TAS}$	Transfer Address Strobe
$\overline{CLK}$	System Clock
$\overline{CGW}$	Clock Gate (Write)
$\overline{CGR}$	Clock Gate (Read)
SAD	Serial Address
$\overline{SAS}$	Serial Address Strobe
$\overline{WE}$	Read/Write Enable

■ BLOCK DIAGRAM



0107-2

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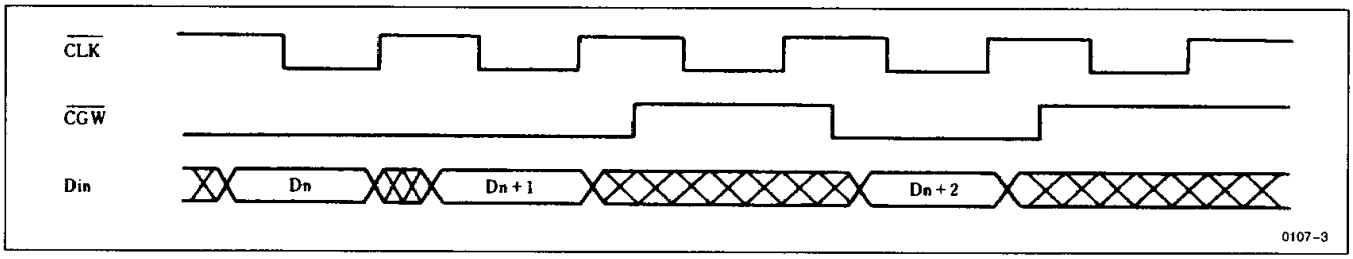
■ FUNCTIONAL DESCRIPTION

• Serial Access Memory with I/O Separated

Read cycle and write cycle of HM53051 can be operated independently synchronized with a system clock. It realizes time compression or expansion for picture in picture in digital TV, for example.

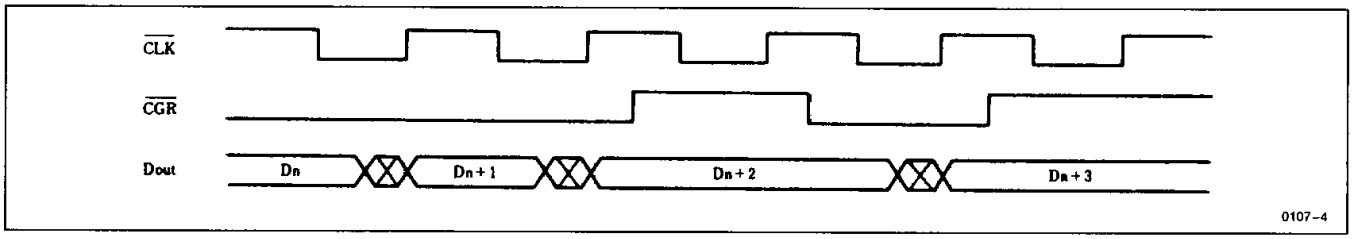
• Write Cycle by $\overline{CGW}$

Write data are taken in at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGW}$ is low. If $\overline{CGW}$ is high, HM53051 does not enter write cycle (cycle time is defined by system clock cycle time). Time is compressed easily with $\overline{CGW}$.



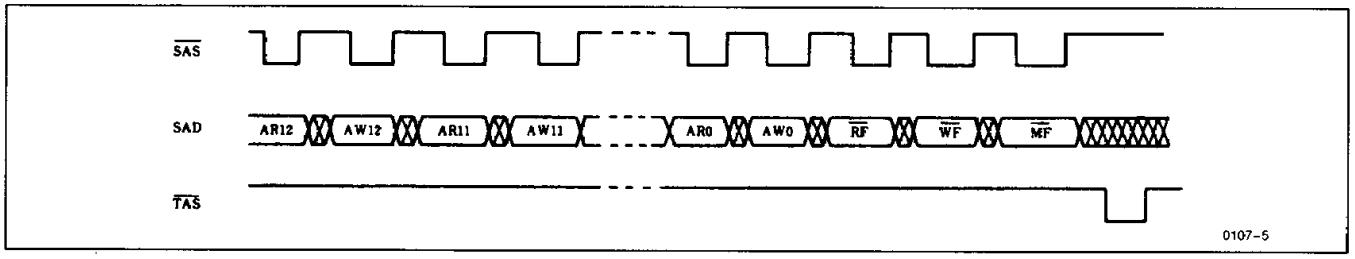
• Read Cycle by $\overline{CGR}$

Read data is output at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGR}$ is low. If $\overline{CGR}$ is high, HM53051 does not enter read cycle (cycle time is defined by system clock time). Time is expanded is realized easily with $\overline{CGR}$.



■ RANDOM ACCESS

The HM53051 is also capable of random access by serial address input, SAD. Random access by the unit of 32-word x 4-bit is performed, when $\overline{TAS}$ is low after read address (AR0–AR12), write address (AW0–AW12) and mode setting flags, $\overline{RF}$ (Read Flag), $\overline{WF}$ (Write Flag) and $\overline{MF}$ (Mode Flag) are read into by $\overline{SAD}$ with synchronous $\overline{SAS}$. In order to output data continuously, the address specified by $\overline{SAD}$ increments automatically.



■ MODE PROGRAMMING

Operation mode in HM53051 is programmed by the combination of SAD 5-bit.

$\overline{MF}$	$\overline{WF}$	$\overline{RF}$	AW0	AR0	Mode
0	0	0	x	x	Write/Read Address Asynchronous Transfer
0	0	1	x	x	Write Address Asynchronous Transfer
0	1	0	x	x	Read Address Asynchronous Transfer
0	1	1	x	x	
1	0	0	x	x	Write/Read Address Synchronous Transfer
1	0	1	x	x	Write Address Synchronous Transfer
1	1	0	x	x	Read Address Synchronous Transfer
1	1	1	1	1	System Reset
1	1	1	0	0	Inhibit
1	1	1	0	1	
1	1	1	1	0	

Note: x means Don't Care.

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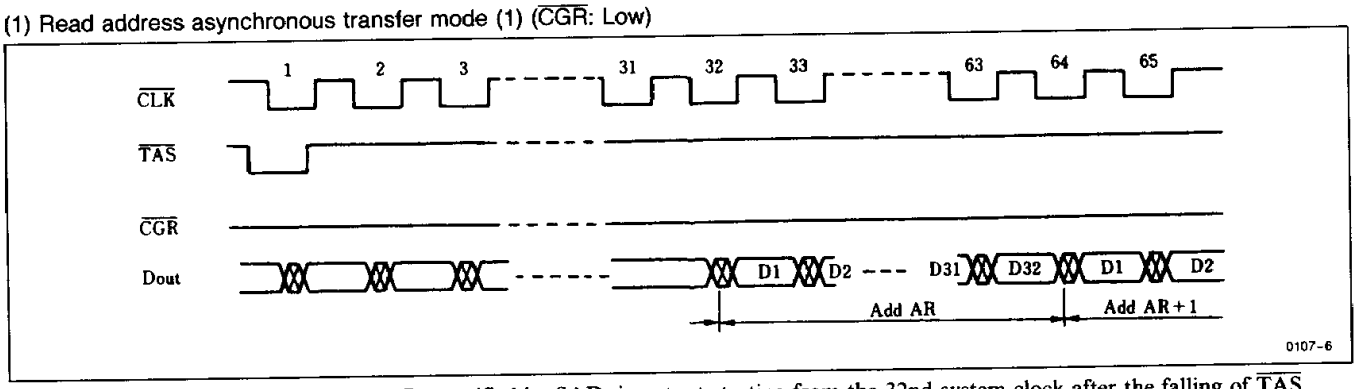
■ READ/WRITE ADDRESS ASYNCHRONOUS TRANSFER MODE

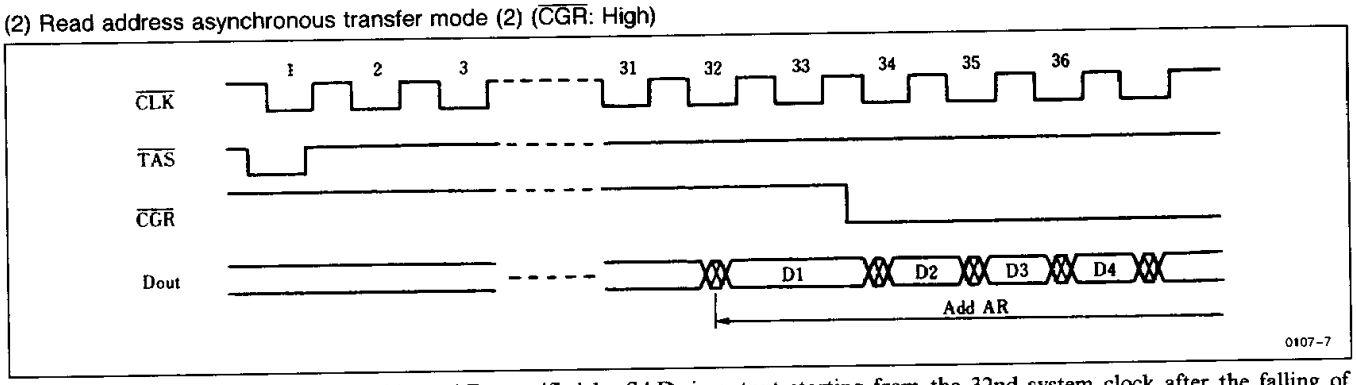
• Read Address Asynchronous Transfer Mode

(1) Read address asynchronous transfer mode (1) ($\overline{CGR}$: Low)



Note: The data block at read address AR, specified by SAD, is output starting from the 32nd system clock after the falling of $\overline{TAS}$.

(2) Read address asynchronous transfer mode (2) ($\overline{CGR}$: High)

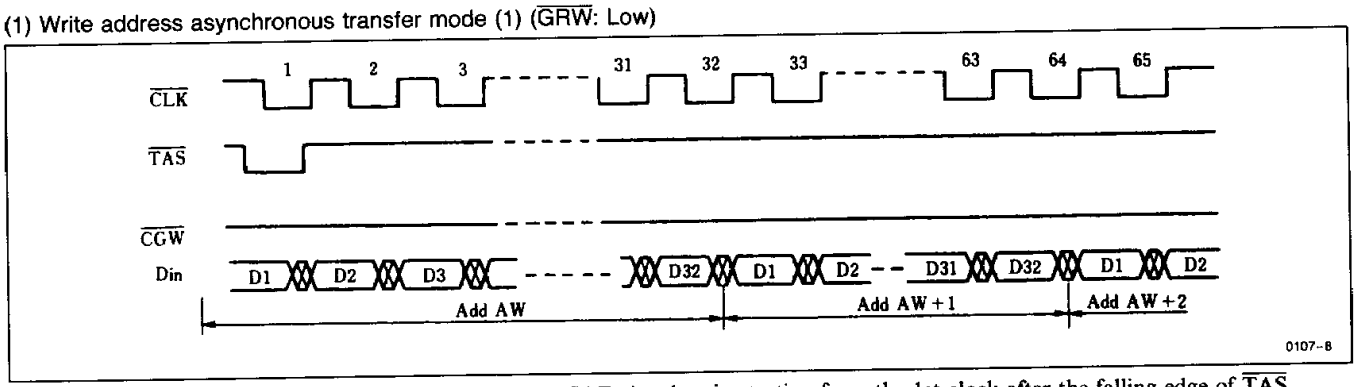


Notes: 1. The data block at read address AR, specified by SAD, is output starting from the 32nd system clock after the falling of $\overline{TAS}$.

2. If $\overline{CGR}$ is turned to low after 33rd clock from falling edge of $\overline{TAS}$, the data at read address AR(D2, D3, D4 . . .) is output with synchronous $\overline{CLK}$ while $\overline{CGR}$ is low.

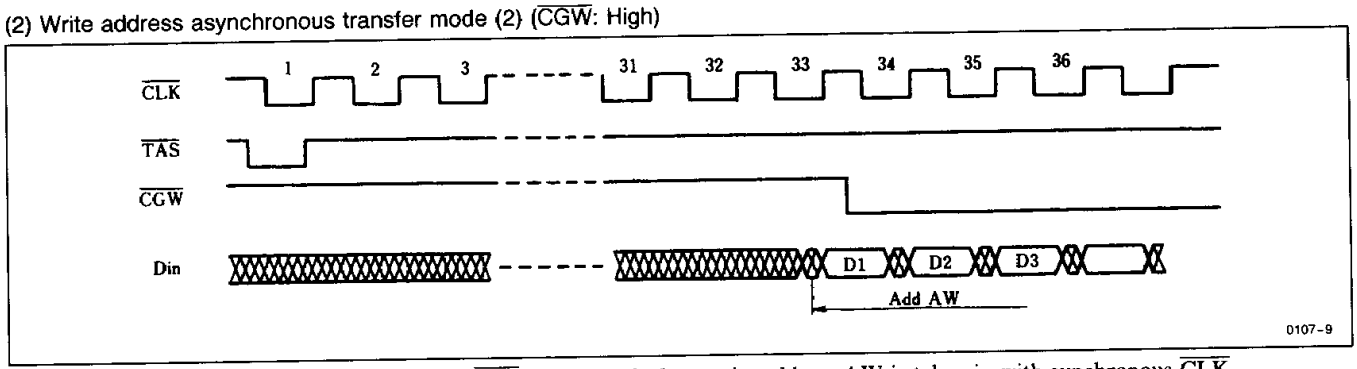
• Write Address Asynchronous Transfer Mode

(1) Write address asynchronous transfer mode (1) ($\overline{GRW}$: Low)



Note: The data block at write address AW, specified by SAD, is taken in starting from the 1st clock after the falling edge of $\overline{TAS}$.

(2) Write address asynchronous transfer mode (2) ($\overline{CGW}$: High)



Note: If $\overline{CGW}$ is turned to low after falling of $\overline{TAS}$, the data block at write address AW is taken in with synchronous $\overline{CLK}$.

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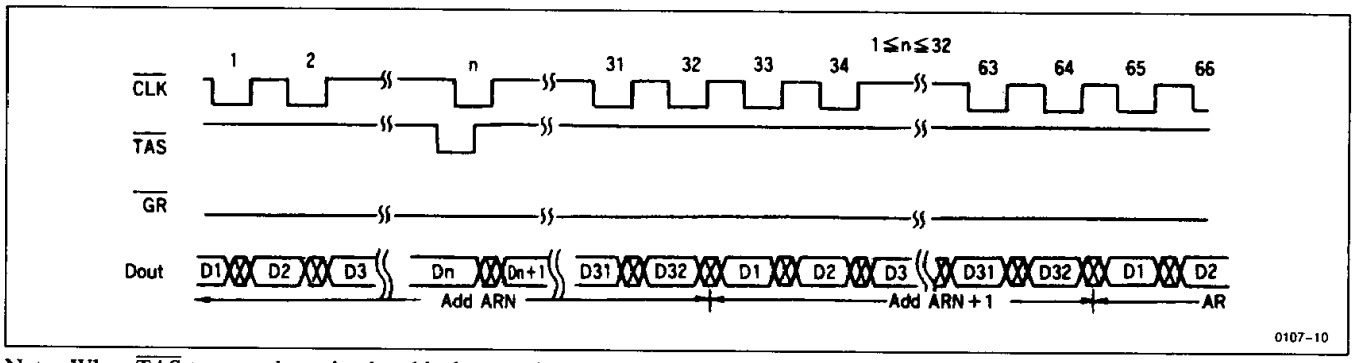
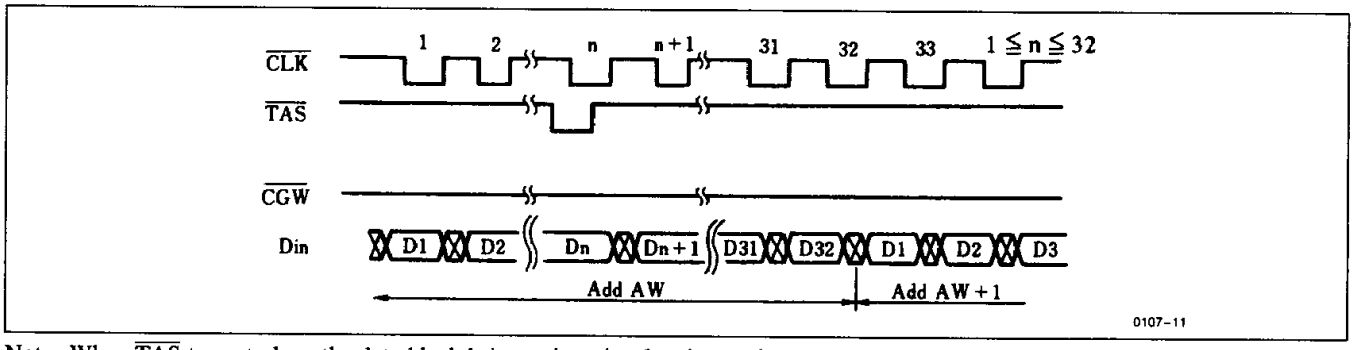
■ READ/WRITE ADDRESS SYNCHRONOUS TRANSFER MODE

• Read Address Synchronous Transfer Mode



Note: When $\overline{TAS}$ turns to low, the data block at read address AR, specified by SAD, is output after the data block at the present read address ARN, and the next address ARN + 1 is put out.

• Write Address Synchronous Transfer Mode



Note: When $\overline{TAS}$ turns to low, the data block being written is taken into write address AW.

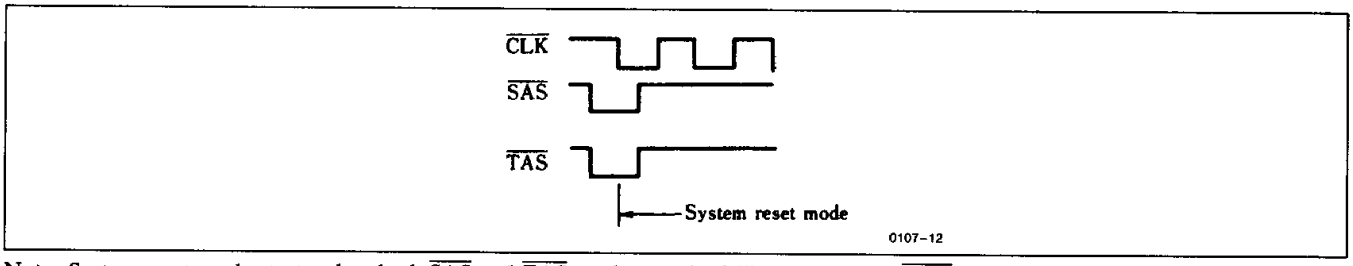
■ SYSTEM RESET MODE

System reset mode is the same as read/write address asynchronous transfer mode except that read/write address are reset to 0.

• System Reset by SAD

Note: System reset mode starts when $\overline{MF}$, $\overline{WF}$, $\overline{RF}$, AW0, and AR0 are all high.

• System Reset by $\overline{SAS}$ and $\overline{TAS}$



Note: System reset mode starts when both $\overline{SAS}$ and $\overline{TAS}$ are low at the falling edge of the $\overline{CLK}$.

• 1 Field Delay

Note: Field-delayed data is output, when $\overline{CGR}$ and $\overline{CGW}$ turn to high before the system reset at the beginning of every field, and turn to low simultaneously after the 33rd clock from the system reset.

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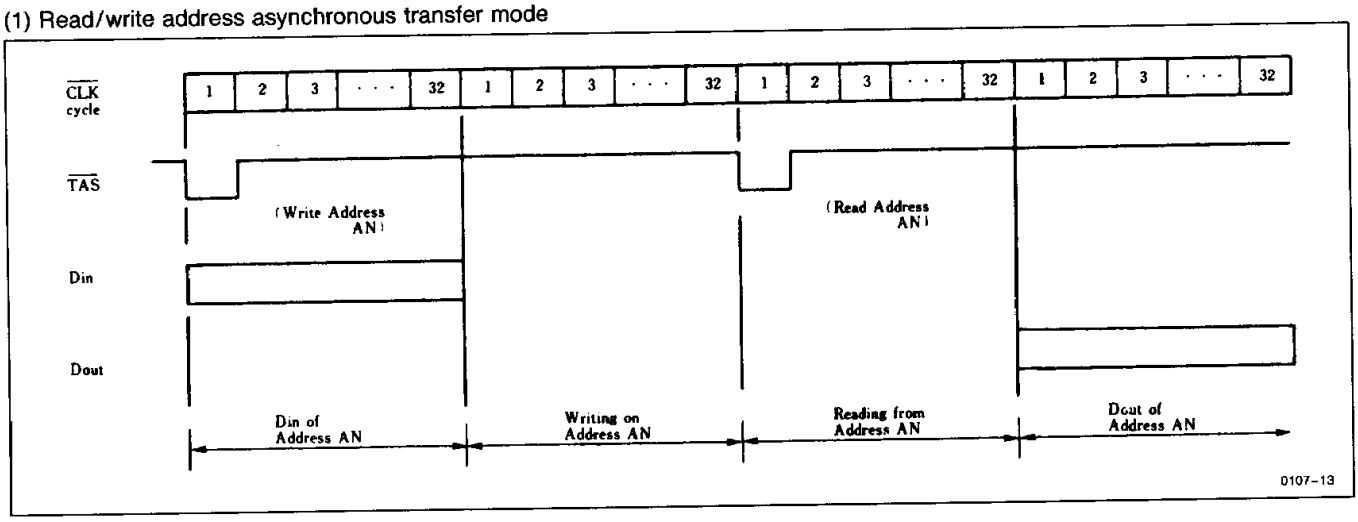
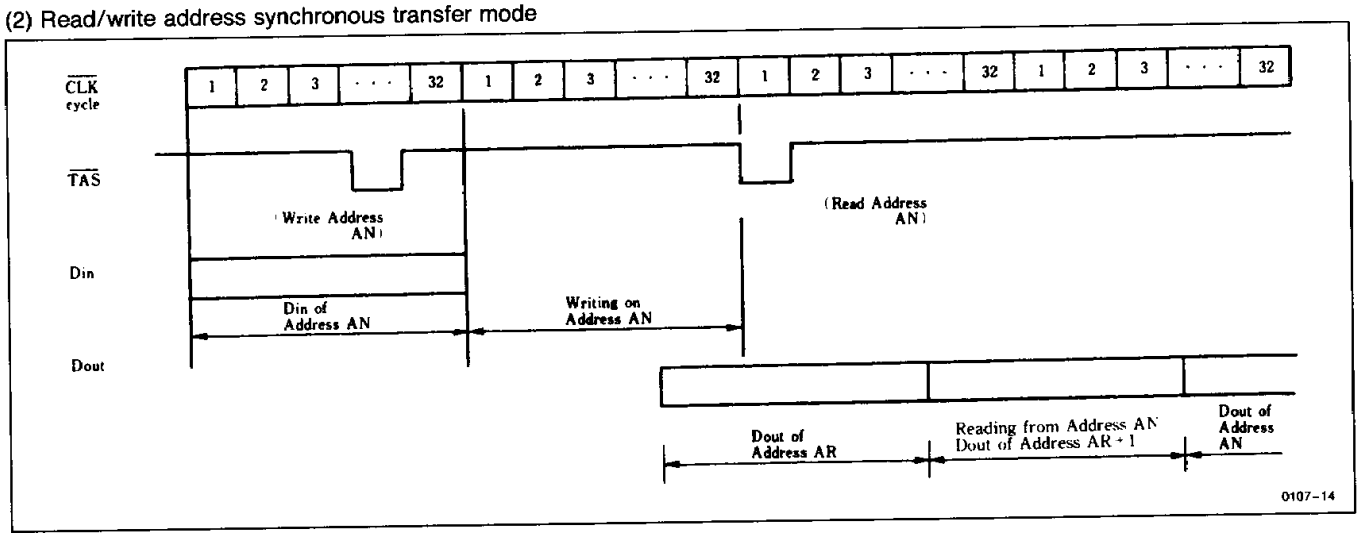
■ NOTES ON USING HM53051

- Input/Output data of 32 words is not written or read in read/write address asynchronous transfer mode or during system reset. The data is written or read out in blocks of 32-word x 4-bit. Input data of less than 32 words is not written in write address asynchronous transfer mode or during system reset. When asynchronous read address transfer mode or system reset mode is activated, output from the current data block will continue. When output data from the current data block is finished, the next data block is not read out if it has less than 32 words.
- Input data is not read out immediately. The data (32 word x 4-bit) is written into the memory array in the next 32 cycles after it is taken in.
  The data can be read out only after writing to the memory array is completed. If read address transfer mode is programmed after the 33 word clock from on input data block, new data can be read out. If this mode is programmed before the 33 word clock, new data or old data is output.

(1) Read/write address asynchronous transfer mode



(2) Read/write address synchronous transfer mode



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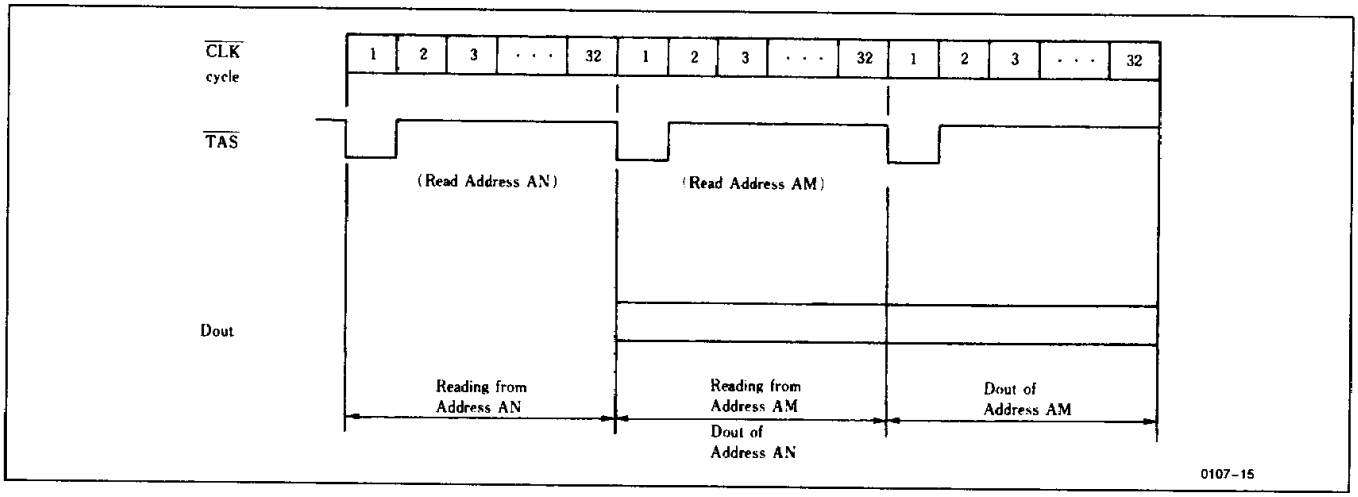
• Mode Programming

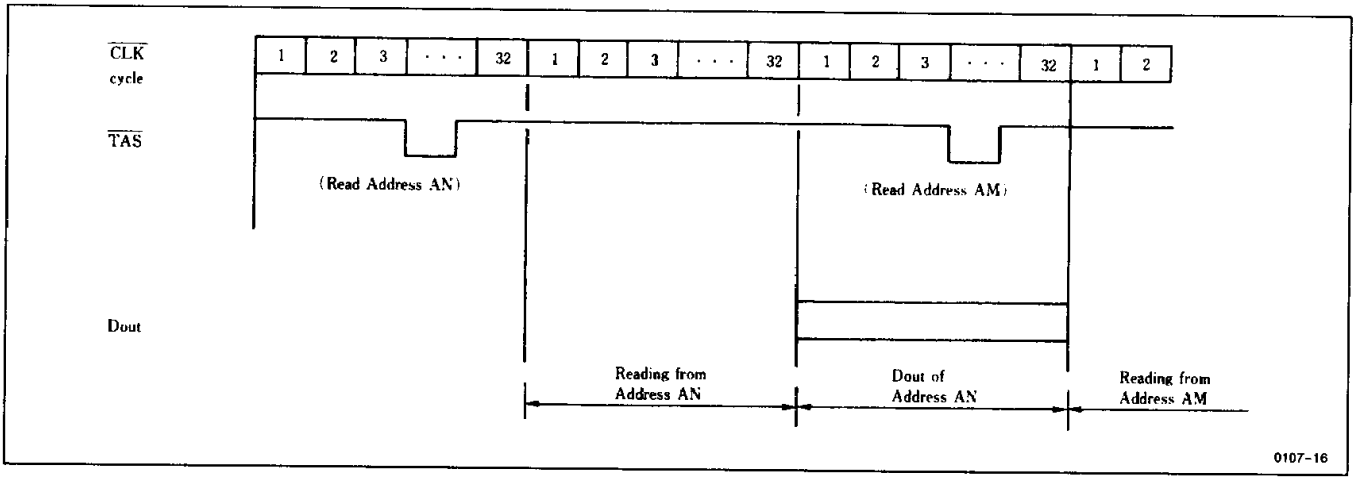
Do not reprogram read address transfer mode before a read operation of the previous read address transfer mode or system reset mode is completed. If it is reprogrammed during a read operation, address becomes invalid, and the device may malfunction.

Do not reprogram write address transfer mode or system reset mode before a write operation of the previous write address transfer mode or system reset mode is completed. If it is reprogrammed during a write operation, address becomes invalid, and the device may malfunction.

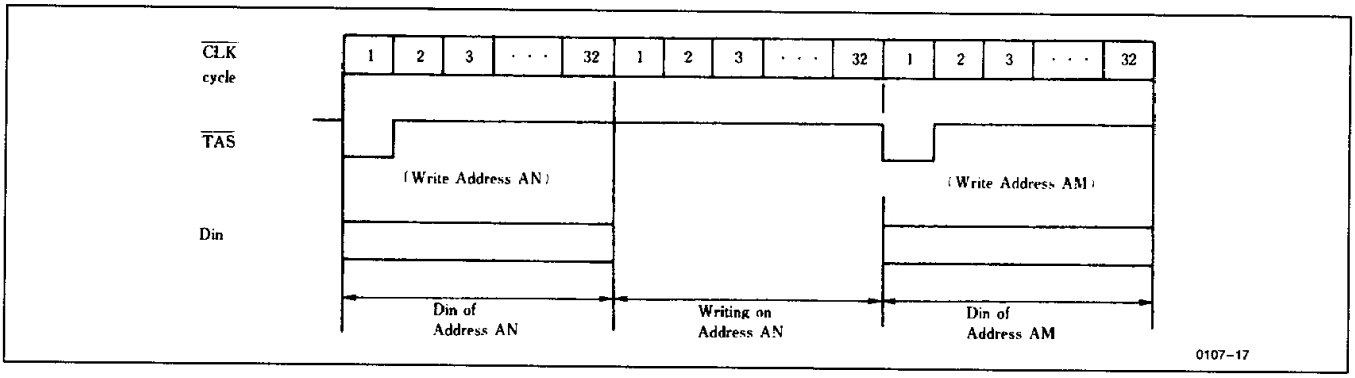
(1) Read address asynchronous transfer mode



(2) Read address synchronous transfer mode



(3) Write address asynchronous transfer mode



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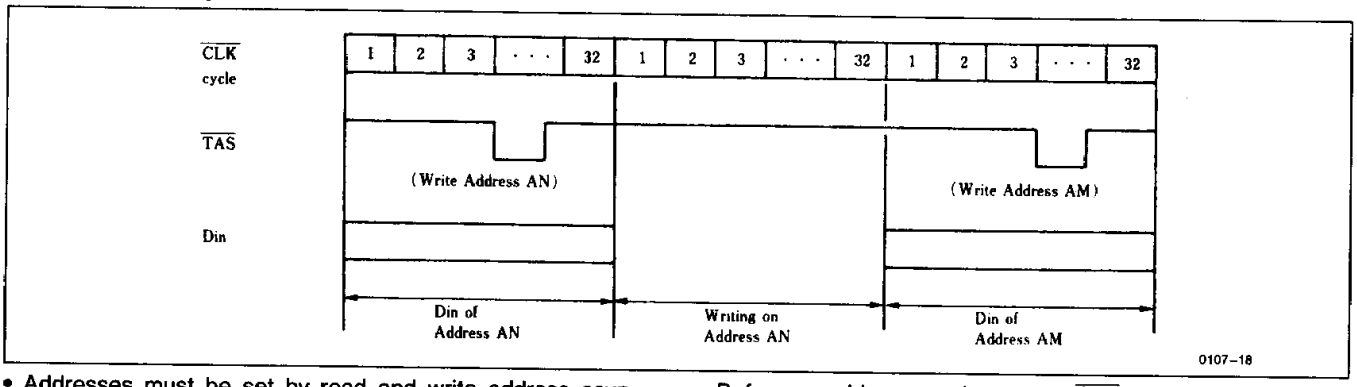
(4) Write address synchronous transfer mode



- Addresses must be set by read and write address asynchronous transfer or system reset 100 μs after power on. Before an address can be set, 32 $\overline{CLK}$ initialization cycles or more are required.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 35 to + 125	°C
Storage Temperature (under Bias)	T_{bias}	− 10 to + 85	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input Voltage	V_{IH}	2.7	—	6.5	V	
	V_{IL}	− 0.5	—	0.8	V	1

Note: 1. − 3.0V for pulse width ≤ 10 ns.

• DC and Operating Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Operating Power Supply Current	I_{CC}	—	40	60	mA	Min. Cycle, I_{out} = 0 mA	
Input Leakage Current	I_{LI}	− 10	—	10	μA	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	I_{LO}	− 10	—	10	μA	$\overline{OE}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.2 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = − 2 mA	

• Capacitance (T_A = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Input Capacitance	C_{in}	—	—	5	pF	V_{in} = 0V	
Output Capacitance	C_{out}	—	—	7	pF	V_{out} = 0V	

Note: This parameter is sampled and not 100% tested.

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• AC Characteristics (V_{CC} = 5V ±10%, T_A = 0 to +70°C)

AC Test Conditions

Input and Output Timing Reference Levels: 1.5V
Input Pulse Levels: V_{SS} to 3V
Input Rise and Fall Times: 5 ns
Output Load: 2 TTL + 50 pF
(Including scope and jig)

Parameter	Symbol	HM53051-45		HM53051-60		Unit
		Min	Max	Min	Max	
System Clock Cycle Time	t_{CC}	45	300	60	300	ns
$\overline{CLK}$ Pulse Width	t_{CL}	15	—	15	—	ns
	t_{CH}	15	—	15	—	ns
Access Time from $\overline{CLK}$	t_{AC}	—	35	—	40	ns
Output Hold Time	t_{OH}	5	—	8	—	ns
Output Enable Access Time	t_{OEA}	—	25	—	30	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	20	0	20	ns
$\overline{CGR}$ Setup Time	t_{GRS}	15	—	15	—	ns
$\overline{CGR}$ Hold Time	t_{GRH}	5	—	5	—	ns
$\overline{CGW}$ Setup Time	t_{GWS}	15	—	15	—	ns
$\overline{CGW}$ Hold Time	t_{GWH}	5	—	5	—	ns
Write Command Setup Time	t_{WCS}	15	—	15	—	ns
Write Command Hold Time	t_{WCH}	5	—	5	—	ns
Data Input Setup Time	t_{DS}	15	—	15	—	ns
Data Input Hold Time	t_{DH}	5	—	5	—	ns
$\overline{SAS}$ Cycle Time	t_{SC}	45	—	60	—	ns
$\overline{SAS}$ Pulse Width	t_{SL}	15	—	15	—	ns
	t_{SH}	15	—	15	—	ns
Serial Address Setup Time	t_{SAS}	15	—	15	—	ns
Serial Address Hold Time	t_{SAH}	5	—	5	—	ns
$\overline{SAS}$ Setup Time during Mode Programming	t_{SSH}	15	—	15	—	ns
$\overline{SAS}$ Hold Time during Mode Programming	t_{SHH}	5	—	5	—	ns
$\overline{TAS}$ Setup Time	t_{TS}	15	—	15	—	ns
$\overline{TAS}$ Hold Time	t_{TH}	5	—	5	—	ns
$\overline{SAS}$ Setup Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SSL}	15	—	15	—	ns
$\overline{SAS}$ Hold Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SHL}	5	—	5	—	ns

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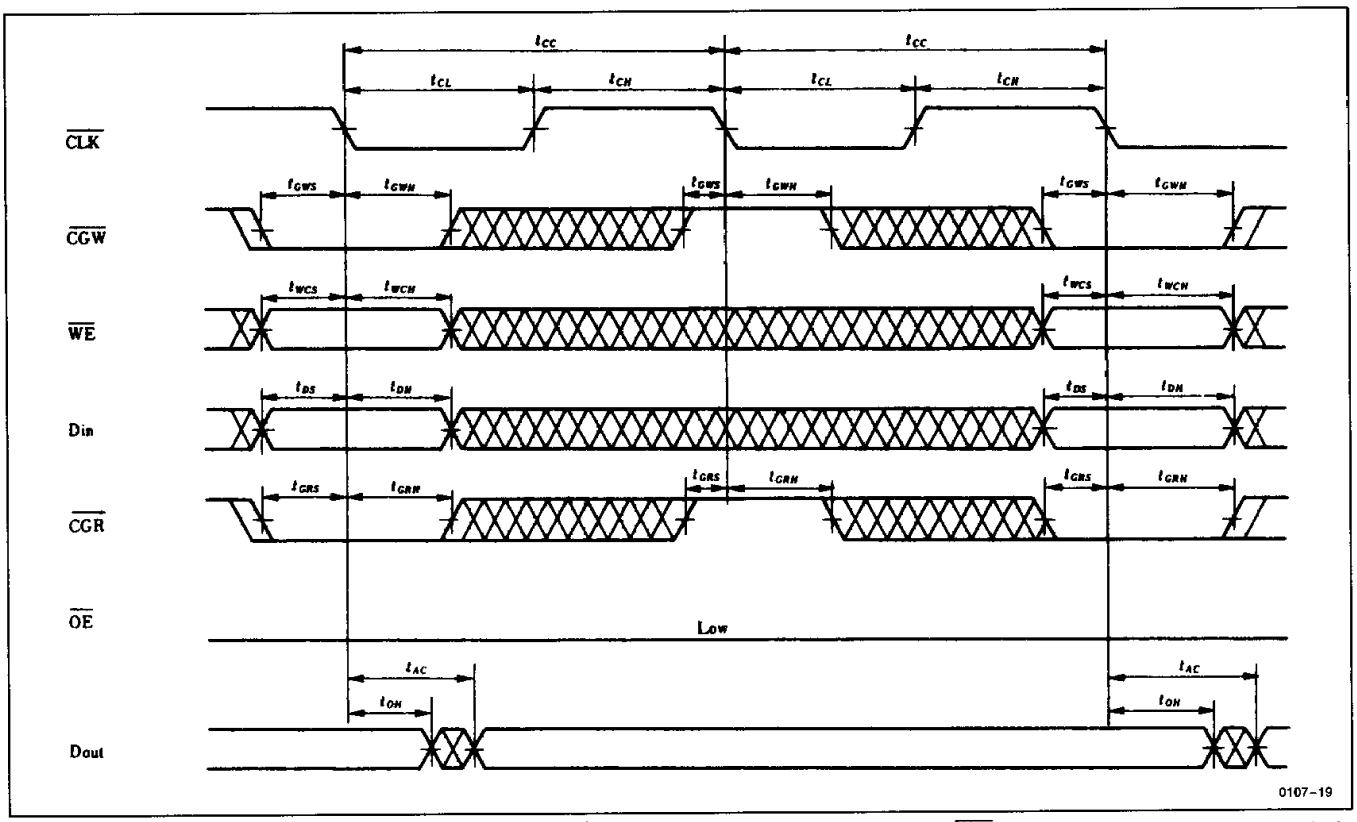
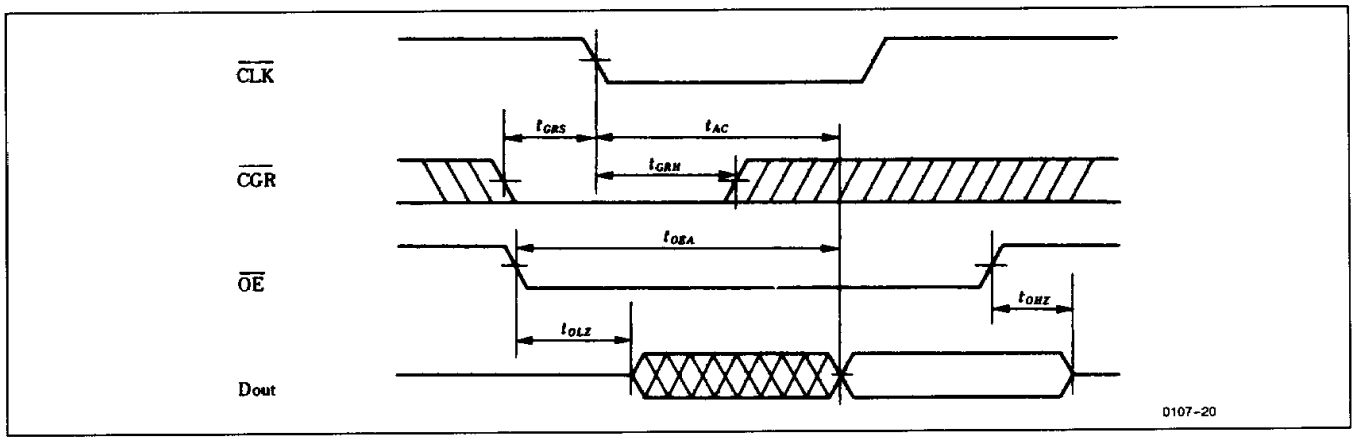
■ TIMING WAVEFORMS

• Read/Write Cycle



Notes: 1. Write cycle starts when $\overline{CGW}$ is low and $\overline{WE}$ is low. Data are not written when $\overline{WE}$ is high. Time-compression mode is realized by controlling $\overline{CGW}$.
2. Read cycle starts when $\overline{CGR}$ is low. Time-expansion mode is realized by controlling $\overline{CGR}$.

• Read Cycle ($\overline{OE}$ Control)



Notes: 1. t_{OHZ} is defined by the time at which the output achieves the open circuit condition.
2. t_{OLZ} and t_{OHZ} are sampled and not 100% tested.

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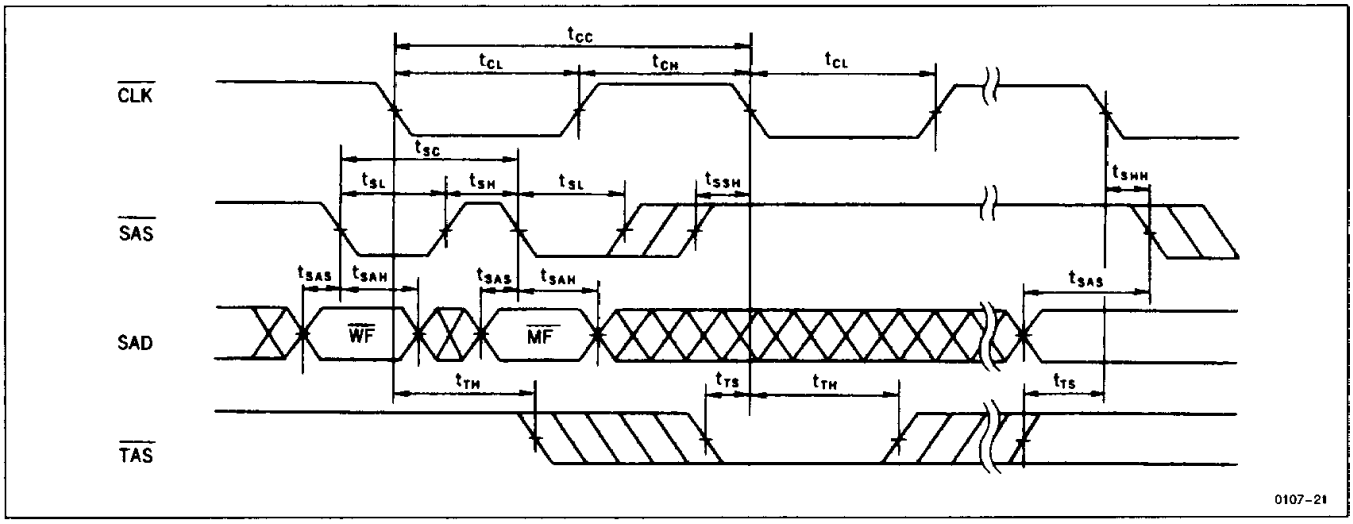
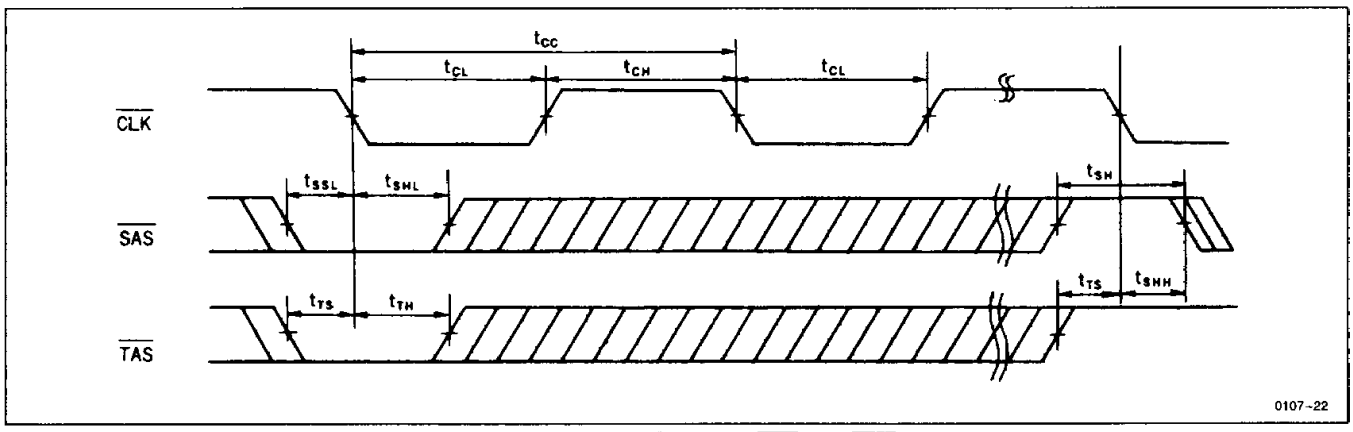
• Mode Selection



Note: $\overline{SAS}$ operates asynchronously with $\overline{CLK}$. When $\overline{TAS}$ is low at the falling edge of the $\overline{CLK}$, the addres transfer cycle starts. $\overline{SAS}$ should be high during the address transfer cycle.

• $\overline{SAS}$, $\overline{TAS}$ Reset Mode



Note: The mode which was selected by SAD before $\overline{SAS}$ and $\overline{TAS}$ reset, if $\overline{SAS}$ and $\overline{TAS}$ are reset, should be changed because SAD is newly taken into by SAS. The mode should be reselected by SAD after $\overline{SAS}$ and $\overline{TAS}$ reset.

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