SONY

CXD2073S

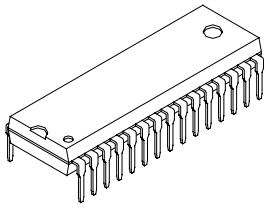
Digital Comb Filter (NTSC)

For the availability of this product, please contact the sales office.

Description

The CXD2073S is an adaptive comb filter compatible with NTSC system, and provide high-precision Y/C separation with a single chip.

30 pin SDIP (Plastic)



Features

- Y/C separation by adaptive processing
- Horizontal aperture compensation circuit
- 8-bit A/D converter (1 channel)
- 8-bit D/A converter (2 channels)
- One 1H delay line
- Clamp circuit

Structure

Silicon gate CMOS IC

Applications

Y/C separation for color TVs and VCRs

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

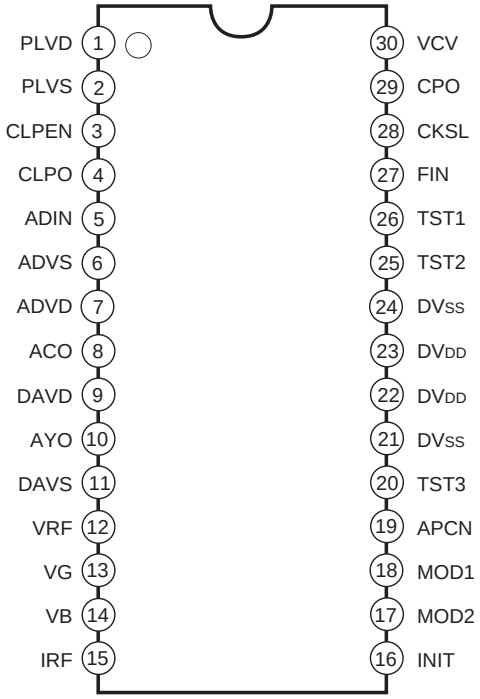
• Supply voltage	DV_{DD}	V_{SS} – 0.5 to +7.0	V
	DAVD	V_{SS} – 0.5 to +7.0	V
	ADVD	V_{SS} – 0.5 to +7.0	V
	PLVD	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} +0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} +0.5	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

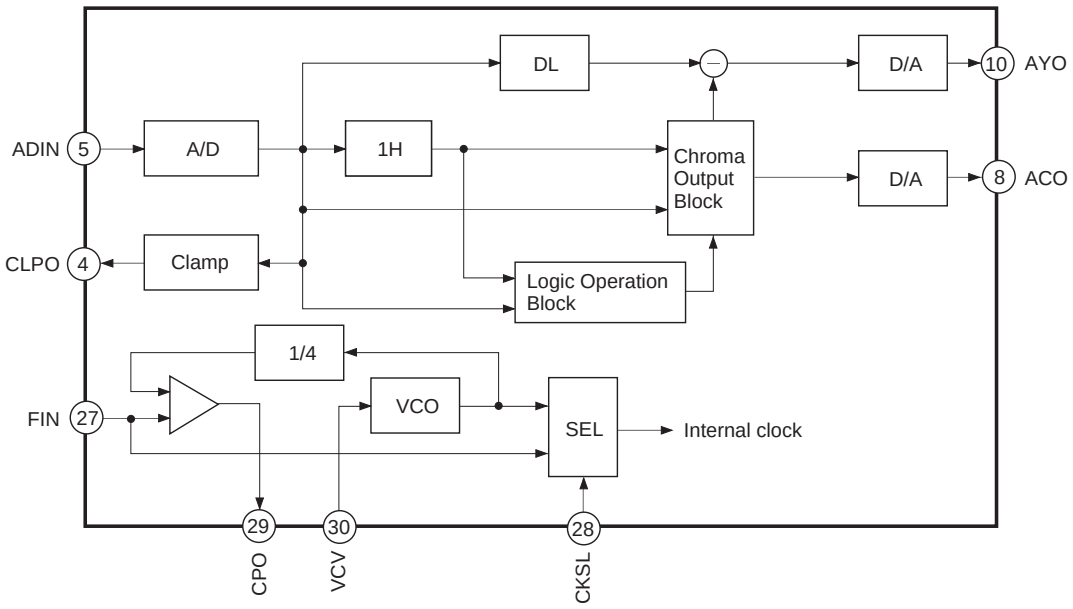
• Supply voltage	DV_{DD}	5.0 ± 0.25	V
	DAVD	5.0 ± 0.25	V
	ADVD	5.0 ± 0.25	V
	PLVD	5.0 ± 0.25	V
• Operating temperature			
	Topr	–20 to +75	°C

E97412B86-PS

Pin Configuration (Top View)



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	PLVD	—	Analog power supply for PLL (+5V)
2	PLVS	—	Analog ground for PLL
3	CLPEN	I	Clamp enable L: Clamp function is enabled. Set to L when the internal clamp is used. H: Clamp function is disabled. Set to H when the internal clamp is not used.
4	CLPO	O	Connect to ADIN when clamp circuit is used. Leave this pin open when clamp circuit is not used.
5	ADIN	I	Comb filter analog input (A/D converter input)
6	ADVS	—	Analog ground for A/D converter
7	ADVD	—	Analog power supply for A/D converter (+5V)
8	ACO	O	Analog chroma signal output
9	DAVD	—	Analog power supply for D/A converter (+5V)
10	AYO	O	Analog luminance signal output
11	DAVS	—	Analog ground for D/A converter
12	VRF	I	D/A converter reference voltage setting. Sets the full-scale value for D/A converter.
13	VG	O	Connect to DAVD via a capacitor of approximately 0.1µF.
14	VB	O	Connect to DAVS via a capacitor of approximately 0.1µF.
15	IRF	O	Connect a resistor of 16 times (16R) that of the output resistor "R" of AYO pin.
16	INIT	I	Test. Normally, fix to Low.
17	MOD2	I	Y/C separation status setting pins MOD2 MOD1 L L Adaptive processing mode L H BPF separation fixed mode H L Y through mode H H Simple comb mode
18	MOD1	I	
19	APCN	I	Aperture compensation switching L: Aperture compensation OFF H: Aperture compensation ON
20	TST3	O	Test. Normally, leave this pin open.
21	DV_{SS}	—	Digital ground
22	DV_{DD}	—	Digital power supply (+5V)
23	DV_{DD}	—	Digital power supply (+5V)
24	DV_{SS}	—	Digital ground
25	TST2	O	Test. Normally, leave this pin open.
26	TST1	I	Test. Normally, fix to Low.
27	FIN	I	Clock input. Input burst-locked clock. Input fsc when the PLL is used. Input 4fsc when the PLL is not used.
28	CKSL	I	PLL control. L: When the PLL is not used. The 4fsc clock input to FIN is supplied internally. H: When the PLL is used. The 4fsc clock from VCO oscillation output is supplied internally.
29	CPO	O	Phase comparison output for the internal PLL. Leave open when the PLL is not used.
30	VCV	I	VCO oscillation control voltage input for the internal PLL. Connect to PLVS when the PLL is not used.

Electrical Characteristics (V_{DD} = 5 ± 0.25V, V_{SS} = 0V, Ta = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	DV_{DD}	—	4.75	5.0	5.25	V
	ADVD					
	DAVD					
	PLVD					
Operating temperature	Topr	—	–20	—	+75	°C
Supply current	I_{DD}	Clock 14MHz	—	55	80	mA
High level input voltage	V_{IH}	CMOS level (Pin 3, 16 to 19, 26, 28)	$V_{DD} \times 0.7$	—	V_{DD}	V
Low level input voltage	V_{IL}		V_{SS}	—	$V_{DD} \times 0.3$	V
High level output voltage	V_{OH}	I_{OH} = –2mA (Pin 20 and 25)	V_{DD} – 0.8	—	V_{DD}	V
Low level output voltage	V_{OL}	I_{OL} = 4mA (Pin 20 and 25)	V_{SS}	—	0.4	V
Logical Vth	LVth	FIN (Pin 27)	—	V_{DD}/2	—	V
Input voltage	V_{IN}		0.5	—	V_{DD}	Vp-p
Feedback resistor	R_{FB}		250k	1M	2.5M	Ω

A/D Converter Characteristics (V_{DD} = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		14.3	—	—	MSPS
Analog input band width	BW	–3dB	—	18	—	MHz
Input bias	BOTTOM		0.48	0.52	0.56	V
	TOP – BOTTOM		1.96	2.08	2.22	V
Differential linearity error	E_D		–1.0	—	+1.0	LSB
Integral linearity error	E_L		–3.0	—	+3.0	LSB

D/A Converter Characteristics (V_{DD} = 5V, V_{RF} = 2V, I_{RF} = 3.3kΩ, R = 200Ω, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax	—	14.3	—	—	MSPS
Differential linearity error	E_D	—	–0.8	—	+0.8	LSB
Integral linearity error	E_L	—	–2.0	—	+2.0	LSB
Output full-scale voltage	V_{FS}	—	1.805	1.90	1.995	V
Output full-scale current	I_{FS}	—	—	9.5	15	mA
Output offset voltage	V_{OS}	—	—	—	1.0	mV
Precision guaranteed output voltage range	V_{OC}	—	1.8	—	2.1	V

Clamp (V_{DD} = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clamp level*1	CLV		—	0.67	—	V

*1 Sync tip clamp

Description of Functions

• Horizontal aperture compensation

Compensates aperture degradation accompanied by D/A conversion.

This compensation is effective for the following modes; adaptive processing, Y through, and simple comb modes.

• Switching of Y/C separation modes

The following four modes can be set; however, the adaptive processing mode or Y through mode is normally used.

(1) Adaptive processing mode

This mode detects interline correlation, switches between comb filter processing and BPF processing, and operates Y/C separation.

(2) Y through mode

The composite video signal input from ADIN (Pin 5) is A/D converted. It is also D/A converted, and then output from AYO (Pin 10).

At this time, the output of ACO (Pin 8) is the same output as that of adaptive processing mode.

(3) BPF mode

C signal is generated by passing composite video signal through BPF.

Y output is a signal in which the C signal generated is subtracted from input composite video signal.

(4) Simple comb mode

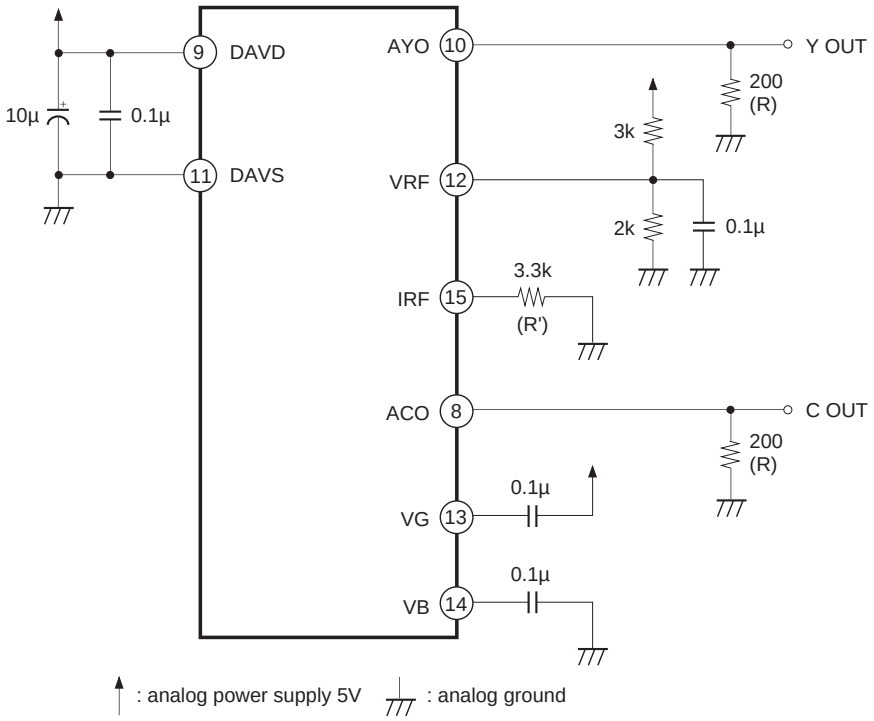
Y/C separation is operated by the comb filter processing forcibly.

Modes	MOD1 (Pin 18)	MOD2 (Pin 17)
Adaptive processing mode	L	L
Y through mode	L	H
BPF mode	H	L
Simple comb mode	H	H

• Selection Pin Setting Table

Pin No.	Symbol	H	L
3	CLPEN	Internal clamp not used	Internal clamp used
17 18	MOD2 MOD1	See the table above.	
19	APCN	Horizontal aperture compensation ON	Horizontal aperture compensation OFF
28	CKSL	Internal 4-multiple PLL used	Internal 4-multiple PLL not used

Application Circuit for D/A Converter



• Method of selecting output resistance

The CXD2073S has a built-in current output-type D/A converter. To obtain the output voltages, connect resistors to AYO and ACO pins.

$$VFS = IFS \times R$$

Here, VFS is output full-scale voltage, IFS is output full-scale current, and R is the output resistance connected to each IO.

In addition, connect a resistance of 16 times the output resistor to the reference current pin IRF. In the case where the value comes to be impractical, use a value of resistance as close to the value calculated as possible. At that time,

$$VFS = VRF \times 16 \times R/R'.$$

R is the output resistance connected to each IO, R' is the resistance connected to IRF, and VRF is the VRF pin voltage. Power consumption can be reduced by using higher resistance values, but then glitch energy and data settling time increase contrastingly. Select optimum resistance values according to the system applications.

In case of the circuit above, VFS = 2 [V] $\times$ 16 $\times$ 0.2k/3.3k $\approx$ 1.93 [V], IFS = 1.93/0.2k $\approx$ 9.65 [mA].

Notes on Operation

• Power supply, ground

Separate the analog and digital systems around the device to reduce noise effect. Both analog and digital V_{DD} are respectively bypassed to V_{SS} as close to these V_{DD} and V_{SS} pins as possible through ceramic capacitors of approximately 0.1µF.

Also, layout the power supply and ground pattern of the board substrate as wide as possible to lower impedance.

• Clock

Use the burst-locked clock. Separate the clock line on the board substrate as far as possible from analog-related pins, analog power supply, and analog ground.

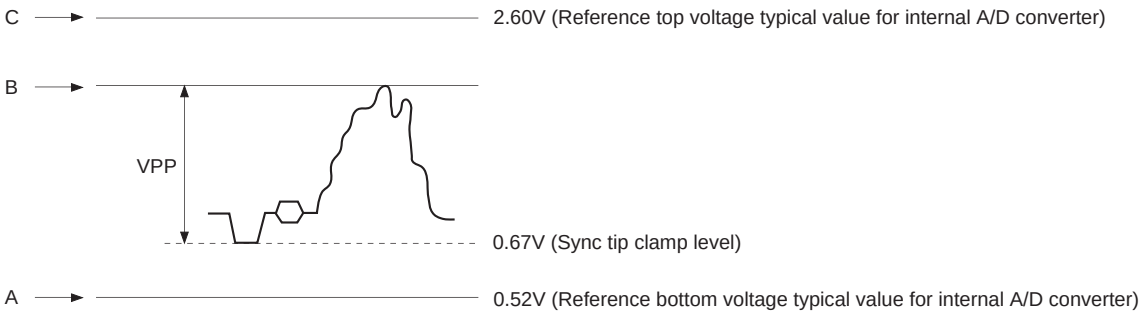
• ADIN (analog input signal)

(1) Low impedance drive

The input signal to ADIN (Pin 5) should be driven at the low impedance and its wiring should be as short as possible.

(2) Input level

Set the input signal peak-to-peak value VPP to 1.75V or less. Additionally, VPP is recommended to be 1.3V or more since the A/D converter input dynamic range should be made as large as possible.



The DC level at the ADIN pin is as shown in the diagram above when the internal sync tip clamp is used.

Labeling the internal D/A converter AYO output full-scale voltage as VFS, the correspondence between the ADIN pin voltage and AYO output pin voltage (DC level) is as follows;

DC voltage at point A → 0 [V]
DC voltage at point B → AYO maximum output voltage [V]
DC voltage at point C → VFS [V]

The VFS is the AYO output voltage generated when the voltage equivalent to the point C is input.

• Internal delay

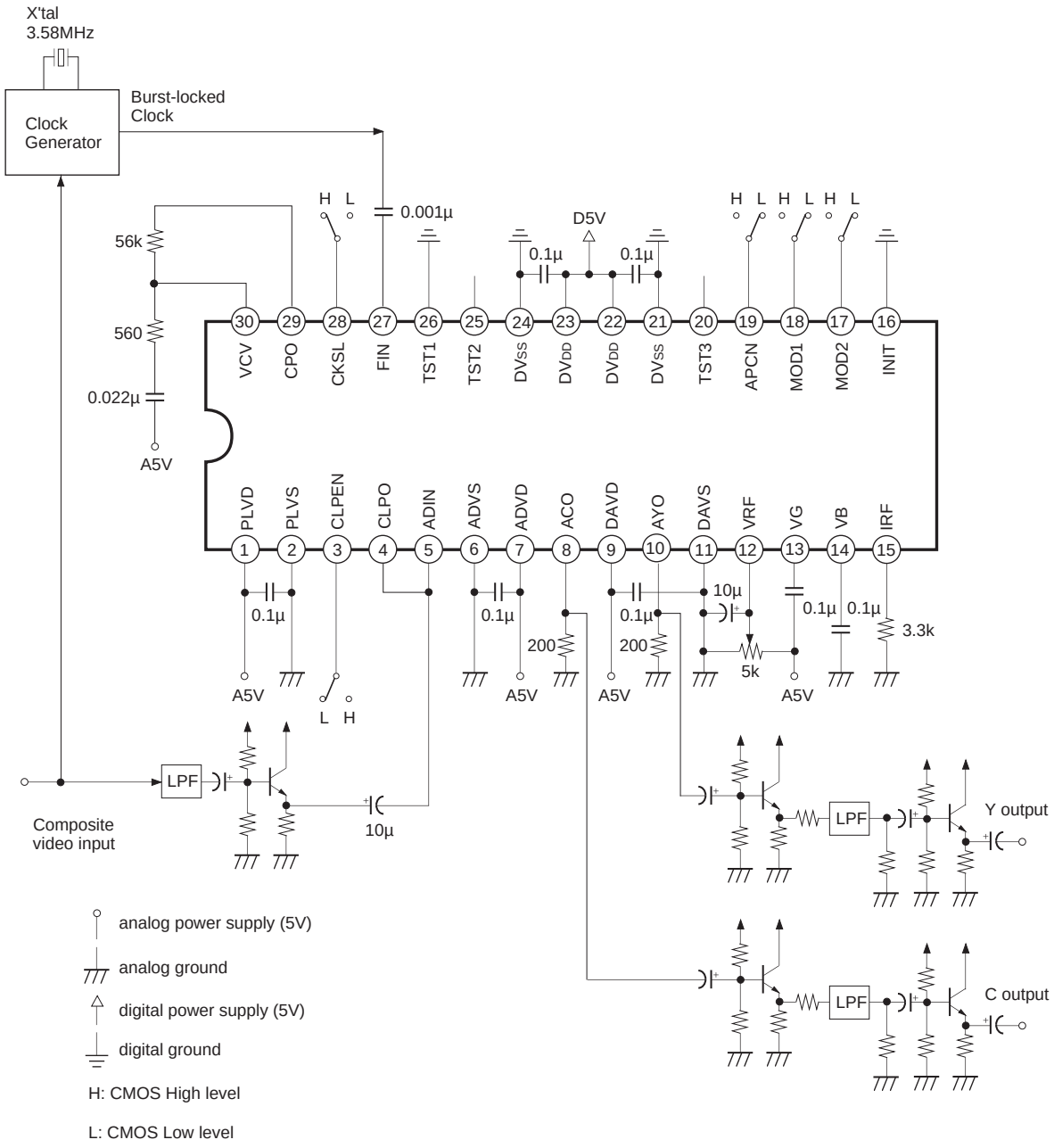
The delay from the internal A/D converter to the D/A converter output is 21.5 clocks + αns (α: D/A converter analog output delay = approximately 20ns).

The 21.5 clocks are the sum of the clocks shown below;

A/D converter: 3.5 clocks (“0.5” is for fetching the data at the fall of the clock.)
Internal logic : 17 clocks
D/A converter: 1 clock

Application Circuit

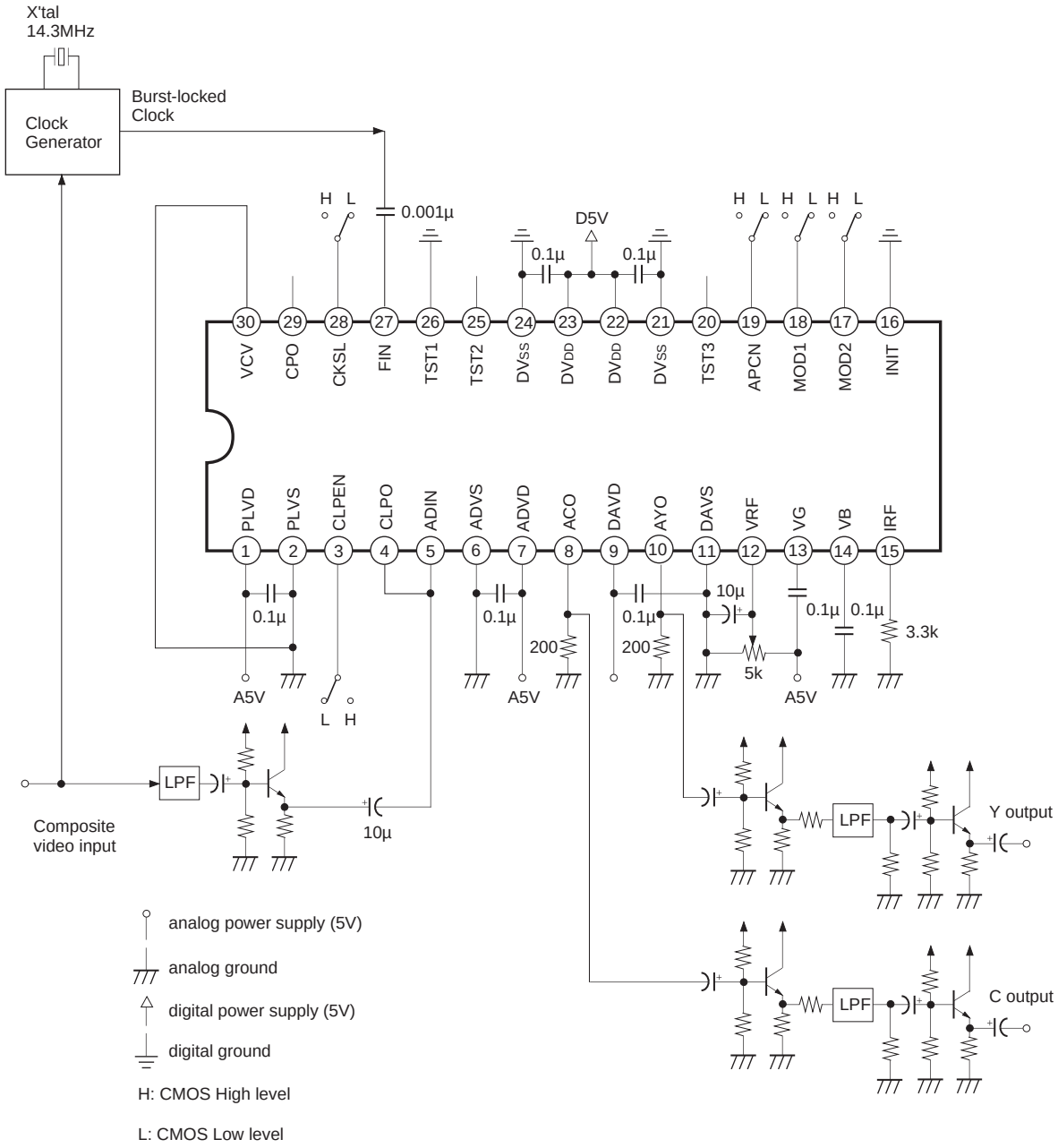
(1) When the fsc clock is used



Recommended LPF: TH327LSJS-2513LCAS (TOKO)
(–3dB at 8MHz)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

(2) When the 4fsc clock is used



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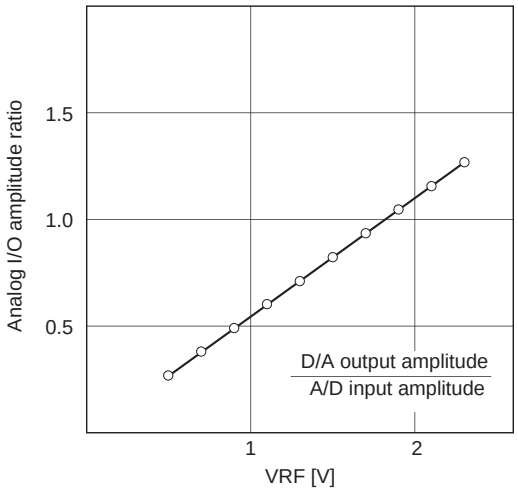
(–3dB at 8MHz)

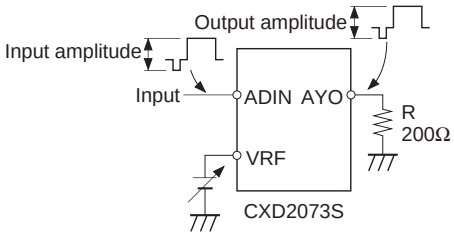
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

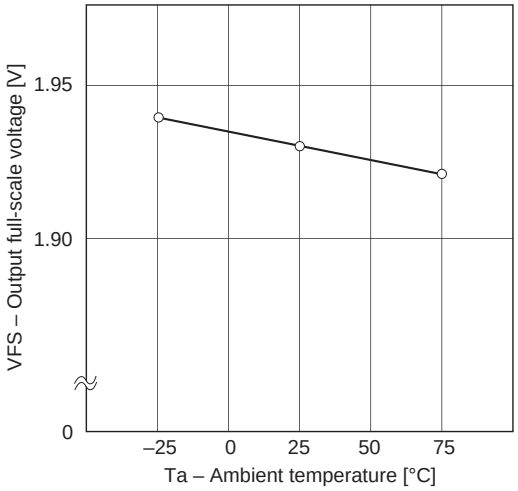
Analog I/O amplitude ratio vs. VRF pin voltage

Input signal peak-to-peak voltage ≤ 1.75V



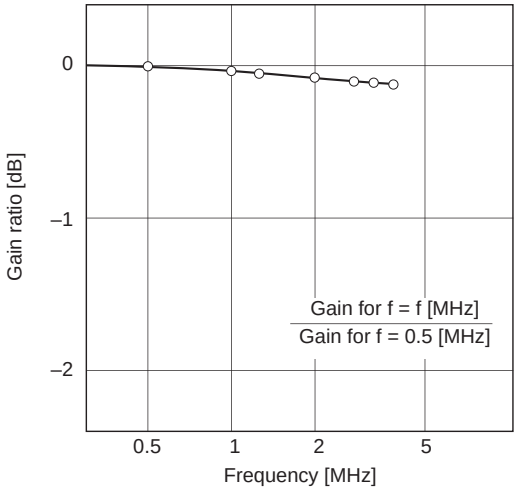


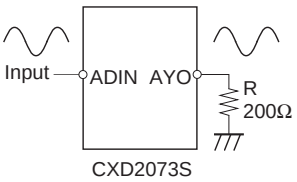
Output full-scale voltage vs. Ambient temperature



V_{DD} = 5V
VRF = 2V
IRF = 3.3kΩ
R = 200Ω

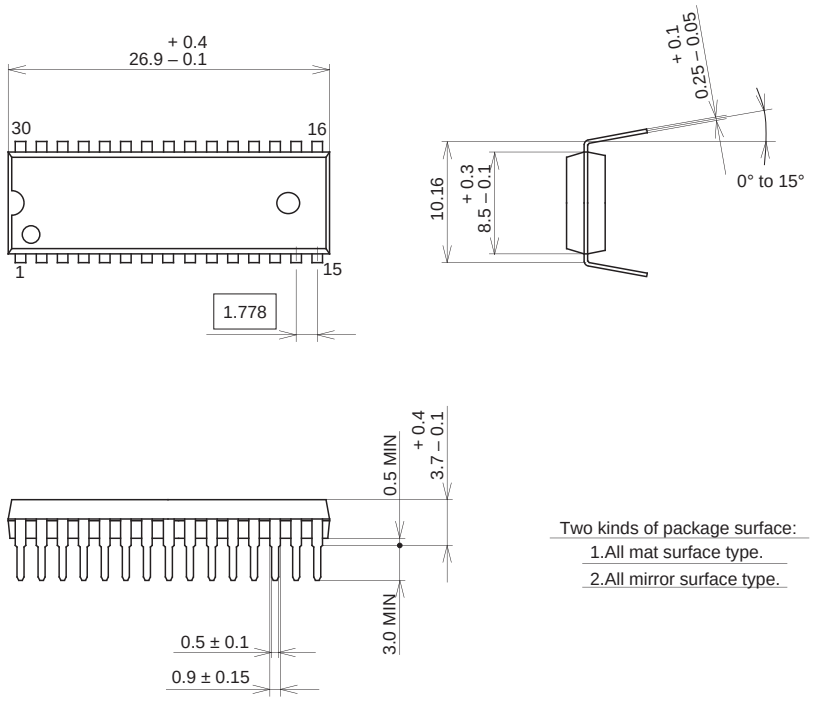
AYO (Y output) frequency response





Package Outline Unit: mm

30PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

SONY CODE	SDIP-30P-01
EIAJ CODE	SDIP030-P-0400
JEDEC CODE	

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g