An Introduction to FETs

Introduction

The basic principle of the field-effect transistor (FET) has been known since J. E. Lilienfeld's patent of 1925. The theoretical description of a FET made by Shockley in 1952 paved the way for development of a classic electronic device which provides the designer the means to accomplish nearly every circuit function. At one time, the field-effect transistor was known as a "unipolar" transistor. The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology, parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

Amplifiers
- Small Signal
- Low Distortion
- High Gain
- Low Noise
- Selectivity
- DC
- High-Frequency

Current Limiters

Voltage-Controlled Resistors

Mixers

Oscillators

Switches
- Chopper-Type
- Analog Gate
- Communicator

Protection Diodes
- Low-leakage

The family tree of FET devices (Figure 1) may be divided into two main branches, Junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, metal-oxide- semiconductor field-effect transistors). Junction FETs are inherently depletion-mode devices, and are available in both n- and p-channel configurations. MOSFETs are available in both enhancement and depletion modes, and also exist as both n- and p-channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

Junction FETs

In its most elementary form, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased pn junction formed along the channel. Implicit in this description is the fundamental difference between JFET and bipolar devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The JFET is a high-input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes. N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

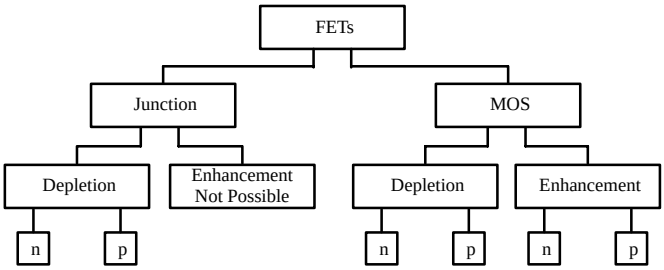

Figure 1. FET Family Tree

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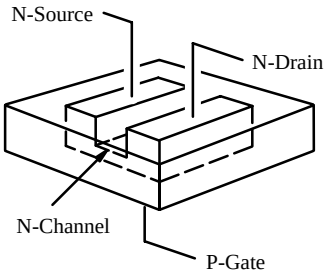
In addition to the channel material, a JFET contains two ohmic (non-rectifying) contacts: the source and the drain. These are shown in Figure 2. Since a symmetrical geometry is shown in the idealized JFET chip, it is immaterial which contact is called the source and which is called the drain; the JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.



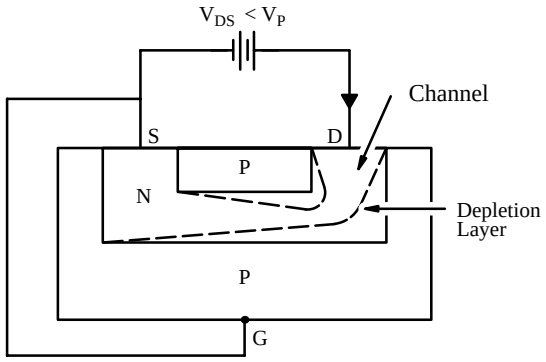
Final form taken by FET with n-type channel embedded in p-type substrate.

Figure 2. Idealized Structure of An N-Channel Junction FET

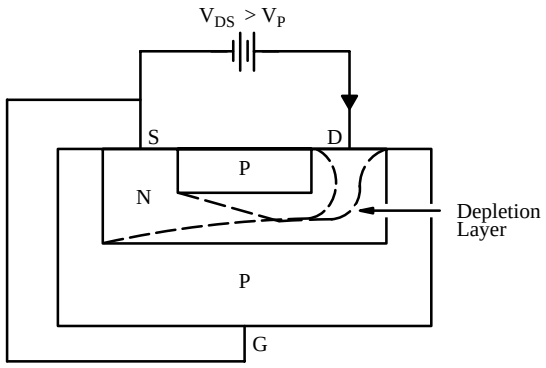
(For certain JFET applications, such as high-frequency amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

Figure 3 shows how the JFET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the pn junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the n-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (Drain-to-Source current with the gate shorted to the source). Figure b shows the almost complete depletion of the channel under these conditions.

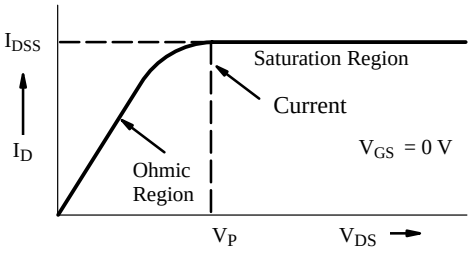
Figure 3c shows the output characteristics of an n-channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be pinched off. The physical meaning of this term leads to one definition of pinch-off voltage, V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.



3a) N-Channel FET Working in the Ohmic Region (V_{GS} = 0 V) (Depletion Shown Only in Channel Region)



3b) N-Channel FET Working in the Current Saturation Region (V_{GS} = 0)



3c) Idealized Output Characteristic for V_{GS} = 0

Figure 3.

In Figure 4, consider the case where V_{DS} = 0 and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for V_{GS} = 0. In fact, at a value of $V_{GS} > V_P$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_P or by $V_{GS(off)}$. V_P has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off.

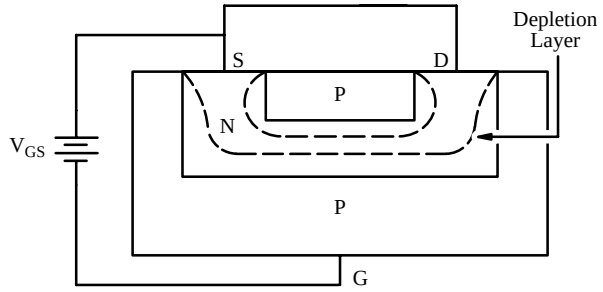


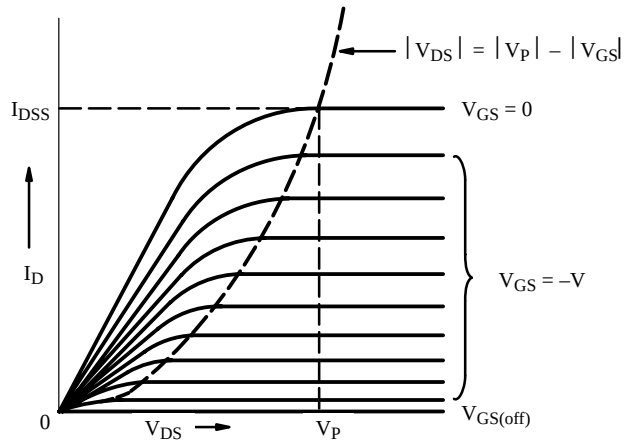
Figure 4. N-Channel FET Showing Depletion Due to Gate-Source Voltage and V_{DS} = 0

The mechanisms of Figures 3 and 4 react together to provide the family of output characteristics shown in Figure 5a. The area below the pinch-off voltage locus is known as the ohmic region: the area above pinch-off is current saturation region. JFETs operating in the current saturation region make excellent amplifiers. Note that in the ohmic region both V_{GS} and V_{DS} control the channel current, while in the current saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.

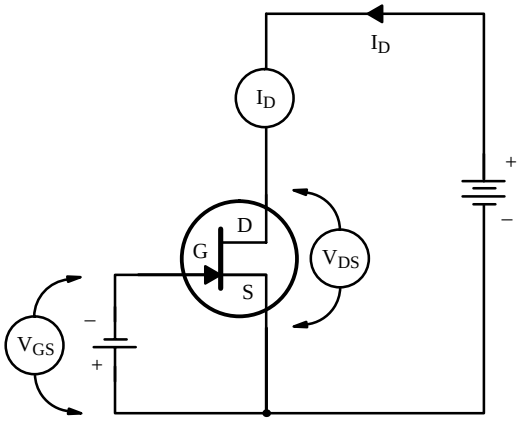
Figure 5b relates the curves in Figure 5a to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.

The p-channel JFET works in precisely the same way as the n-channel JFET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto n-type silicon, and the donor impurity diffused later to form a second n-type region and leave a p-type channel. In the p-channel JFET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_P, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



5a) Family of Output Characteristics for N-Channel FET



5b) Circuit Arrangement for N-Channel FET

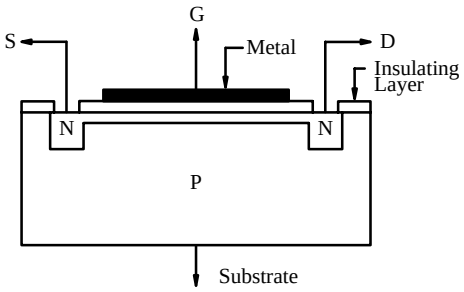
Figure 5.

MOSFETs

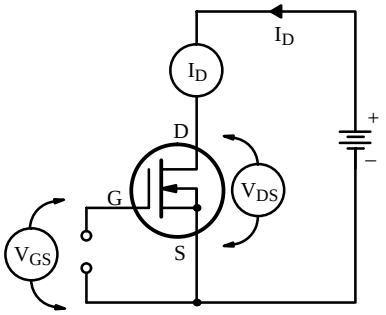
The metal-oxide-semiconductor FET (MOSFET) depends on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET to achieve gate control of the channel current. On a MOSFET, the metallic or polysilicon gate is isolated from the channel by a thin layer of silicon dioxide (Figure 6a). Although the bottom of the insulating layer is in contact with the p-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate in the interface, inverting the p-type material and spontaneously forming an n-type channel. Thus, a conduction path exists between the diffused n-type channel source and drain regions.

There are, however, some fundamental performance differences between MOSFETs and JFETS. JFETs, by nature, operate only in the depletion mode. That is, a reverse gate bias depletes, or pinches off the flow of channel current. A MOSFET, by virtue of its electrically-insulated gate, can be fabricated to perform as either a depletion-mode or enhancement-mode FET. Quite unlike the JFET, a depletion-mode MOSFET will also perform as an enhancement-mode FET.

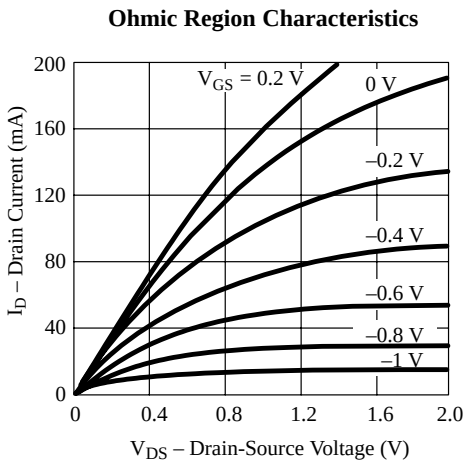
While the great majority of JFETs operate as described in Figures 3 and 4, MOSFETs can assume several forms and operate in either the depletion/enhancement-mode or enhancement-mode only.



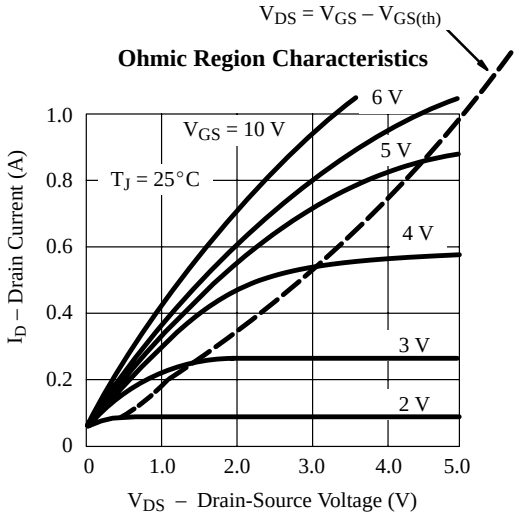
6a) Idealized Cross-Section Through an N-Channel Depletion-Type MOSFET



6b) Circuit Arrangement for N-Channel Depletion MOSFET



6c) Family of Output Characteristics for N-Channel Depletion MOSFET



6d) Family of Output Characteristics for N-Channel Enhancement MOSFET

Figure 6.

There are three types of small-signal MOSFETs. First, we have the planar, lateral MOSFET, similar to that shown in Figure 6a. By virtue of the n-doped channel spanning from source to drain, it performs as an n-channel depletion-mode MOSFET in a fashion not unlike that of the depletion-mode JFET when a voltage of the correct polarity is applied to the gate, as in Figure 6b. However, if we forward-bias the gate (that is, place a gate voltage whose polarity equals the drain voltage polarity) additional electrons will be attracted to the region beneath the gate, further enhancing – and inverting (from p to n) the region. As the channel region thickens, the channel resistance will further decrease, allowing greater channel current to flow beyond that identified as I_{DSS}, as we see in the family of output characteristics in Figure 6c.

MOSFETs can also be constructed for enhancement-mode-only performance, as shown in Figure 7. Unlike the depletion-mode device, the enhancement-mode MOSFET offers no channel between the source and drain. Not until a forward bias on the gate enhances a channel by attracting electrons beneath the gate oxide will current begin to flow (Figure 6d).

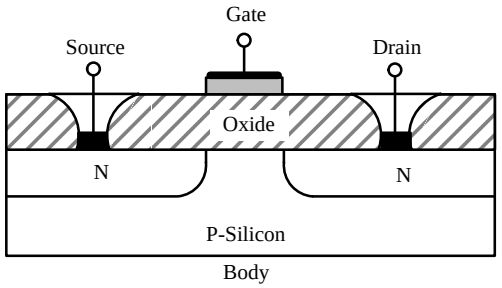


Figure 7. Planar Enhancement-Mode MOS Cross-Section

A newer MOSFET offering superior performance is the lateral double-diffused or DMOS FET. Because of the limitations of photo-lithographic masking, the earlier, older-style MOSFET was severely limited in performance. Some of these former limitations involved switching speeds, channel conductivity (too high an r_{DS}), and current handling in general. The lateral DMOS FET removed these limitations, offering a viable alternative between the JFET and the GaAs FET for video and high-speed switching applications.

The lateral DMOS FET differs radically in its channel construction when compared with the older planar MOSFET. Note the double-diffused source implant into the implanted p-doped channel region, shown in Figure 8. The improved performance of DMOS is a result of both the precisely-defined short channel that results and the "drift region" resulting from the remaining p-doped silicon body and light n-doped ion implant.

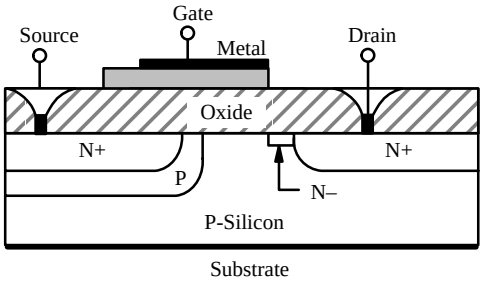


Figure 8. Planar Enhancement-Mode DMOS

Although Figures 7 and 8 illustrate n-channel enhancement-mode DMOS FETs, by reversing the doping sequences, p-channel DMOS FETs can easily be fabricated. Furthermore, by lightly doping across the short channel and drift region, depletion-mode DMOS FETs can be constructed.

As a result of the short channel, the MOSFET is allowed to operate in "velocity saturation" and as a result of the drift region, the MOSFET offers higher operating voltages. Together, the short channel and the drift region offer low on-resistance and low interelectrode capacitances, especially gate-to-drain, V_{GD}.

Velocity saturation coupled with low interelectrode capacitance offers us high-speed and high-frequency performance.

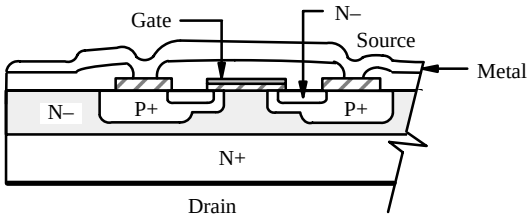


Figure 9. Vertical N-Channel Enhancement-Mode DMOS FET

The novelty of the short-channel DMOS FET led to the evolution of a yet more advanced, higher-voltage, higher-current MOSFET: the Vertical Double-Diffused MOSFET (Figure 9). Where this vertical MOSFET offers improved power-handling capabilities, its fundamental shortcoming is that because of its construction and to a lesser extent because of its size, it fails to challenge the high-speed performance of the lateral DMOS FET. Consequently, the vertical and lateral DMOS FETs complement each other in a wide selection of applications.