

## 64K x 4 Static RAM

### Features

- High speed
  - 12 ns
- Output enable ( $\overline{OE}$ ) feature (7C195 and 7C196)
- CMOS for optimum speed/power
- Low active power
  - 880 mW
- Low standby power
  - 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

### Functional Description

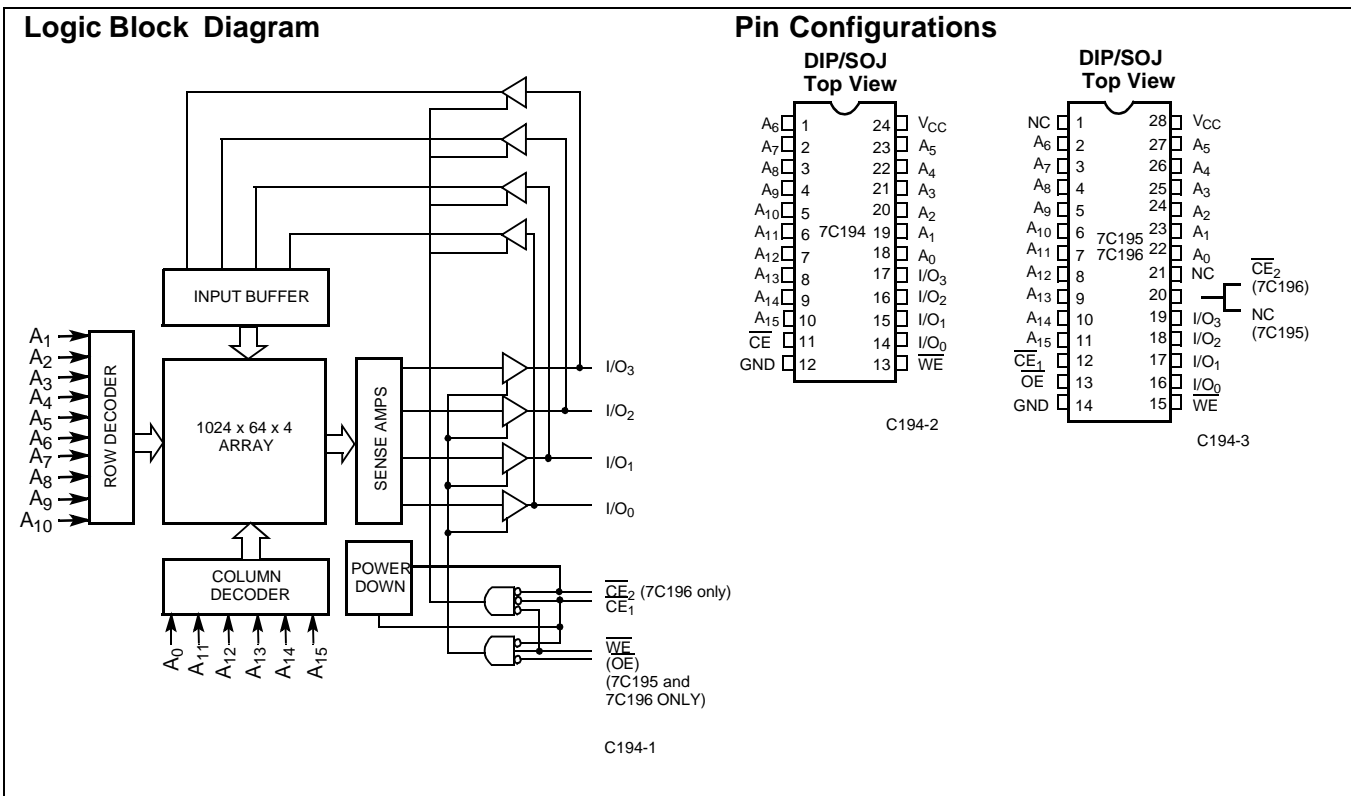
The CY7C194, CY7C195, and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW Chip En-

able(s) ( $\overline{CE}$  on the CY7C194 and CY7C195,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the Chip Enable(s) ( $\overline{CE}$  on the CY7C194 and CY7C195,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) and Write Enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location, specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking the Chip Enable(s) ( $\overline{CE}$  on the CY7C194 and CY7C195,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) LOW, while Write Enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

A die coat is used to ensure alpha immunity.



### Selection Guide

	7C194-12 7C195-12 7C196-12	7C194-15 7C195-15 7C196-15	7C194-20 7C195-20 7C196-20	7C194-25 7C195-25 7C196-25	7C194-35 7C195-35 7C196-35	7C194-45 7C196-45
Maximum Access Time (ns)	12	15	20	25	35	45
Maximum Operating Current (mA)	155	145	135	115	115	
Maximum Standby Current (mA)	30	30	30	30	30	30

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

### Operating Range

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
$V_{IL}^{[1]}$	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	µA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	µA
$I_{OS}$	Output Short Circuit Current <sup>[3]</sup>	$V_{CC} = \text{Max.},$ $V_{OUT} = GND$		-300		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		155		145	mA
$I_{SB1}$	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs <sup>[4]</sup>	Max. $V_{CC}, \overline{CE}_{1,2} \geq V_{IH},$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		30		30	mA
$I_{SB2}$	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs <sup>[4]</sup>	Max. $V_{CC}, \overline{CE}_{1,2} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$		10		10	mA

#### Notes:

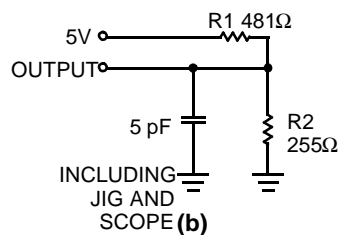
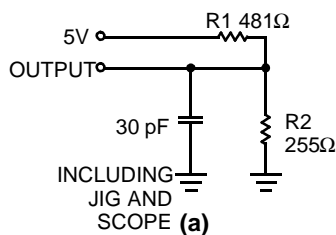
- Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to  $V_{CC}$  on the  $\overline{CE}$  input is required to keep the device deselected during  $V_{CC}$  power-up, otherwise  $I_{SB}$  will exceed values given.

**Electrical Characteristics** Over the Operating Range (continued)

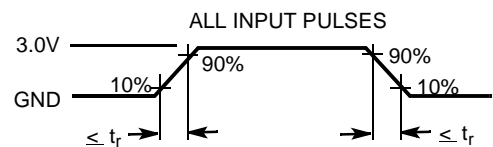
Parameter	Description	Test Conditions	7C194-20 7C195-20 7C196-20		7C194-25, 35, 45 7C195-25, 35 7C196-25, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>oZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		135		115	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs <sup>[4]</sup>	Max. V <sub>CC</sub> , $\overline{CE}_{1,2} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		30	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs <sup>[4]</sup>	Max. V <sub>CC</sub> , $\overline{CE}_{1,2} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		15		15	mA

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**AC Test Loads and Waveforms<sup>[6]</sup>**


C194-4



C194-5

Equivalent to: **THÉVENIN EQUIVALENT**  
 $167\Omega$   
 OUTPUT  $\text{---} \text{---} \text{---} 1.73V$

**Notes:**

5. Tested initially and after any design or process changes that may affect these parameters.
6.  $t_r \leq 3$  ns for the -12 and -15 speeds.  $T_r \leq 5$  ns for the -20 and slower speeds.

**Switching Characteristics** Over the Operating Range<sup>[7]</sup>

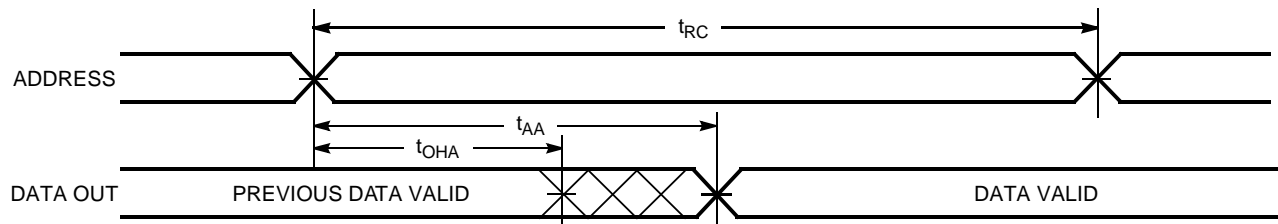
Parameter	Description	7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		7C194-20 7C195-20 7C196-20		7C194-25 7C195-25 7C196-25		7C194-35 7C195-35 7C196-35		7C194-45 7C196-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>														
t <sub>RC</sub>	Read Cycle Time	12		15		20		25		35		45		ns
t <sub>AA</sub>	Address to Data Valid		12		15		20		25		35		45	ns
t <sub>OHA</sub>	Output Hold from Address Change	3		3		3		3		3		3		ns
t <sub>ACE1</sub> , t <sub>ACE2</sub>	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		7		9		10		16		16	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z		0		0		0		3		3		3	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[8]</sup>		5		7		9		11		15		15	ns
t <sub>LZCE1</sub> , t <sub>LZCE2</sub>	$\overline{CE}$ LOW to Low Z <sup>[8]</sup>	3		3		3		3		3		3		ns
t <sub>HZCE1</sub> , t <sub>HZCE2</sub>	$\overline{CE}$ HIGH to High Z <sup>[8,8]</sup>		5		7		9		11		15		15	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35		45	ns
<b>WRITE CYCLE<sup>[10]</sup></b>														
t <sub>WC</sub>	Write Cycle Time	12		15		20		25		35		45		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	9		10		15		18		22		22		ns
t <sub>AW</sub>	Address Set-Up to Write End	9		10		15		20		25		35		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		9		15		18		22		22		ns
t <sub>SD</sub>	Data Set-Up to Write End	8		9		10		10		15		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	3		3		3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[8,9]</sup>		7		7		10		13		15		20	ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  LOW, and  $\overline{WE}$  LOW. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

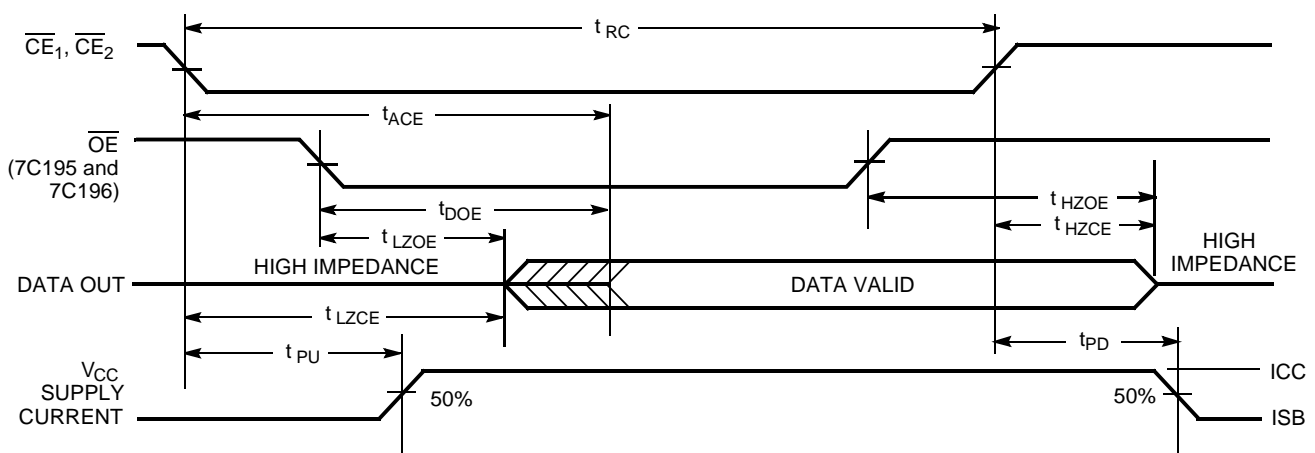
## Switching Waveforms

### Read Cycle No. 1 [11, 12]



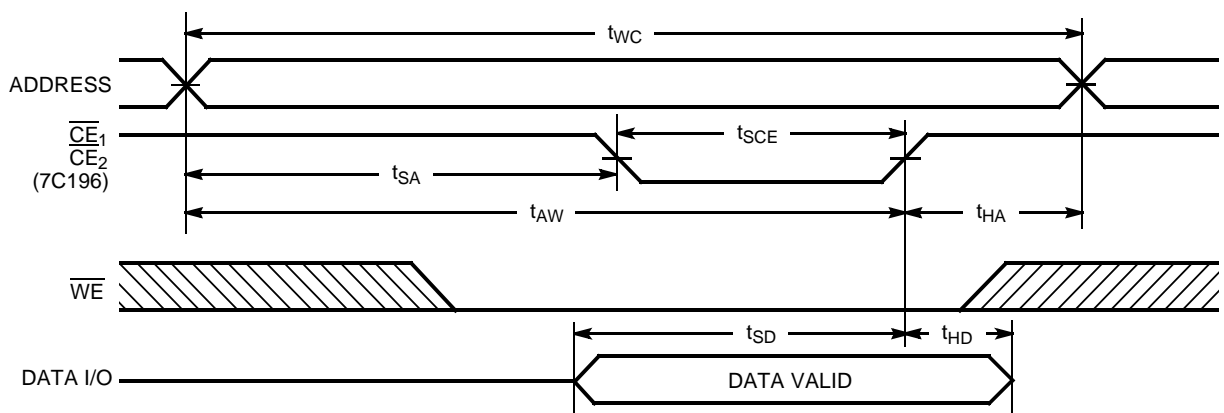
C194-8

### Read Cycle No. 2 [11, 13]



C194-6

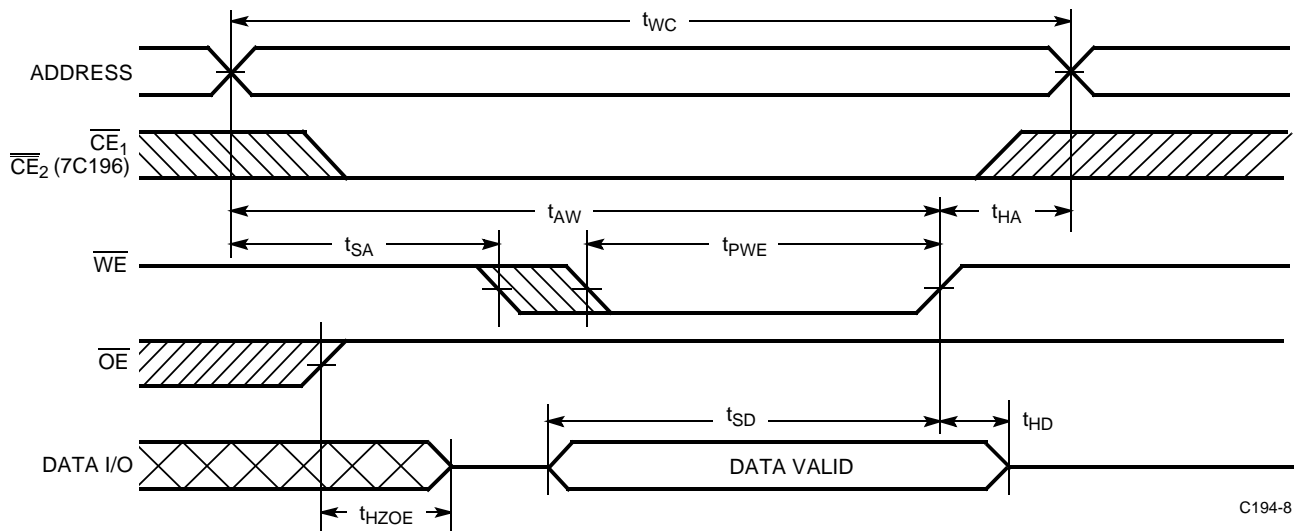
### Write Cycle No. 1 (CE Controlled) [10, 14, 15]



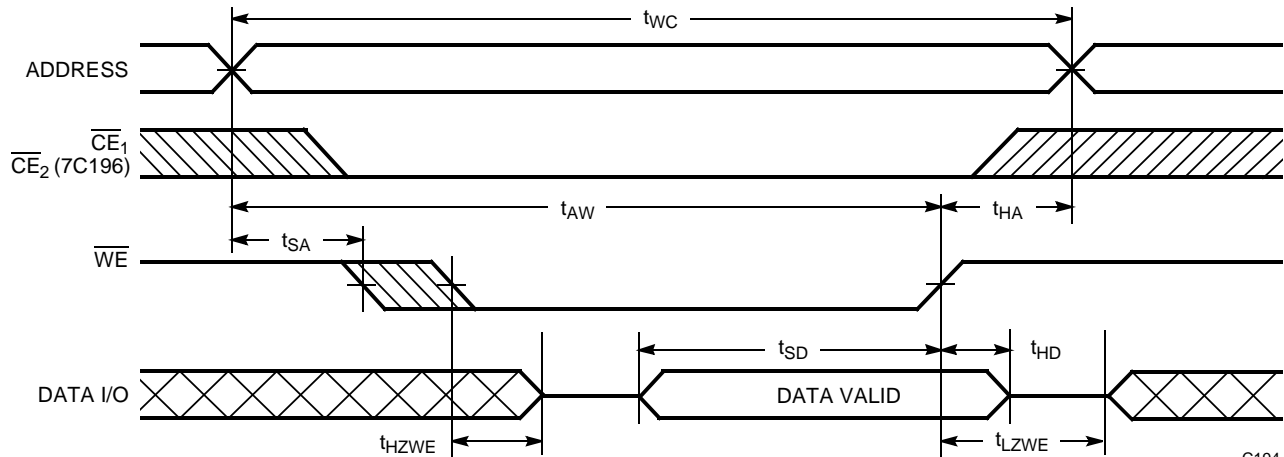
C194-7

#### Notes:

11.  $\overline{WE}$  is HIGH for read cycle.
12. Device is continuously selected:  $\overline{CE}_1 = V_{IL}$ ,  $\overline{CE}_2 = V_{IL}$  (7C196), and  $\overline{OE} = V_{IL}$  (7C195 and 7C196).
13. Address valid prior to or coincident with  $\overline{CE}_1$  and  $\overline{CE}_2$  transition LOW.
14. Data I/O will be high impedance if  $\overline{OE} = V_{IH}$  (7C195 and 7C196).
15. If any CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write for 7C195 and 7C196 only)** <sup>[10, 14, 15]</sup>


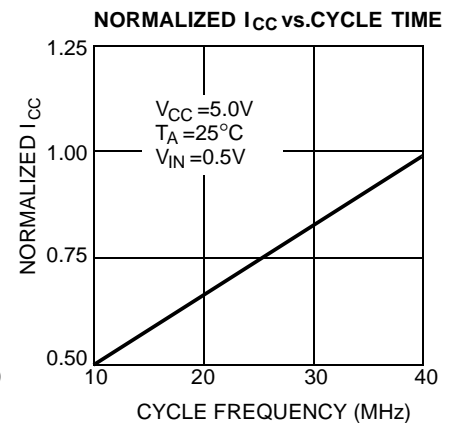
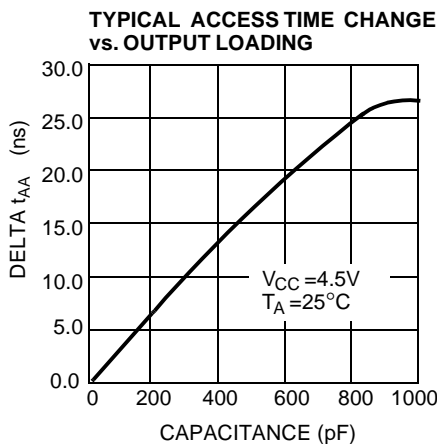
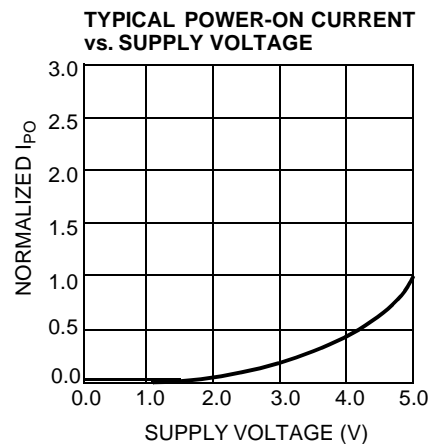
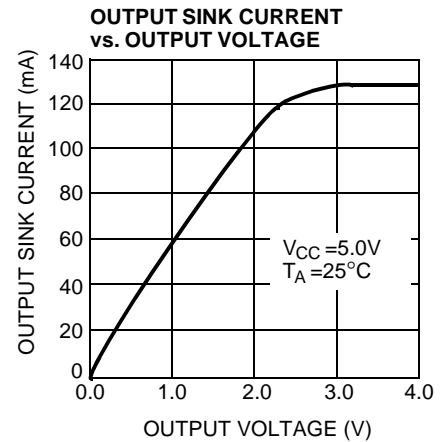
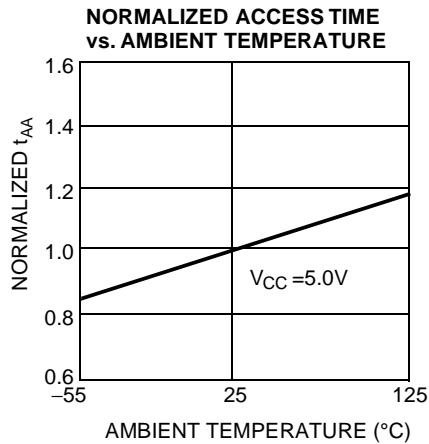
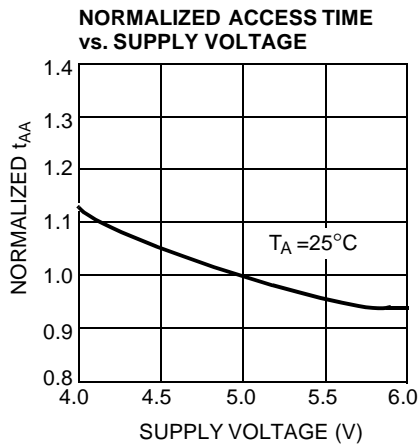
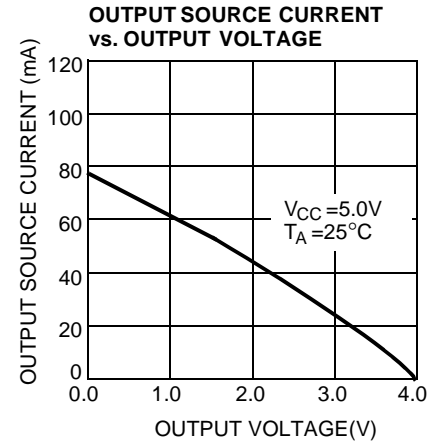
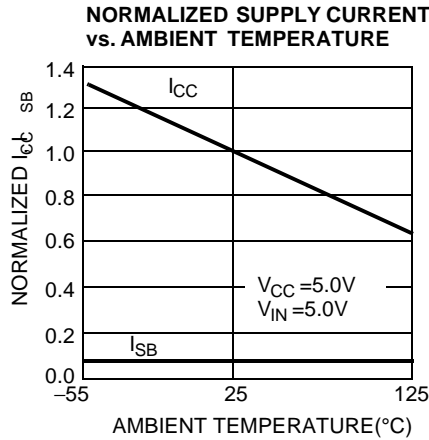
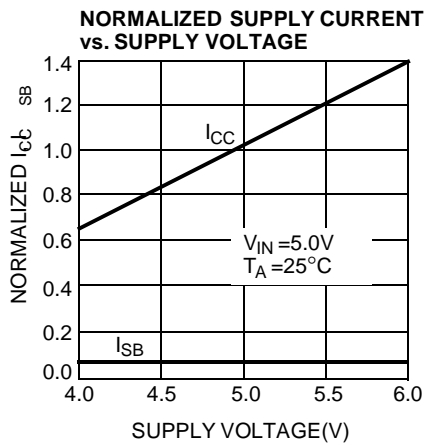
C194-8

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** <sup>[15, 16]</sup>


C194-9

**Note:**

 16. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Typical DC and AC Characteristics**


**7C194 Truth Table**

<b>CE</b>	<b>WE</b>	<b>Data I/O</b>	<b>Mode</b>	<b>Power</b>
H	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	Data Out	Read	Active ( $I_{CC}$ )
L	L	Data In	Write	Active ( $I_{CC}$ )

**7C195 Truth Table**

<b>CE<sub>1</sub></b>	<b>WE</b>	<b>OE</b>	<b>Data I/O</b>	<b>Mode</b>	<b>Power</b>
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect	Active ( $I_{CC}$ )

**7C196 Truth Table**

<b>CE<sub>1</sub></b>	<b>CE<sub>2</sub></b>	<b>WE</b>	<b>OE</b>	<b>Data I/O</b>	<b>Mode</b>	<b>Power</b>
H	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	H	X	X			
L	L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	L	H	H	High Z	Deselect	Active ( $I_{CC}$ )



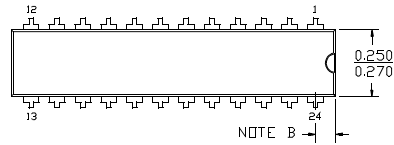
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C194-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-12VC	V13	24-Lead Molded SOJ	
15	CY7C194-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-15VC	V13	24-Lead Molded SOJ	
20	CY7C194-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-20VC	V13	24-Lead Molded SOJ	
25	CY7C194-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-25VC	V13	24-Lead Molded SOJ	
35	CY7C194-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-35VC	V13	24-Lead Molded SOJ	
45	CY7C194-45PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-45VC	V13	24-Lead Molded SOJ	

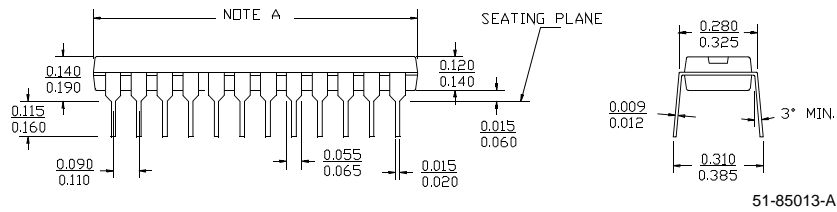
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C195-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-12VC	V21	28-Lead Molded SOJ	
15	CY7C195-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-15VC	V21	28-Lead Molded SOJ	
20	CY7C195-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-20VC	V21	28-Lead Molded SOJ	
25	CY7C195-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-25VC	V21	28-Lead Molded SOJ	
35	CY7C195-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-35VC	V21	28-Lead Molded SOJ	
45	CY7C195-45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-45VC	V21	28-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C196-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-12VC	V21	28-Lead Molded SOJ	
15	CY7C196-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-15VC	V21	28-Lead Molded SOJ	
20	CY7C196-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-20VC	V21	28-Lead Molded SOJ	
25	CY7C196-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-25VC	V21	28-Lead Molded SOJ	
35	CY7C196-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-35VC	V21	28-Lead Molded SOJ	

**Package Diagrams**
**24-Lead (300-Mil) Molded DIP P13/P13A**

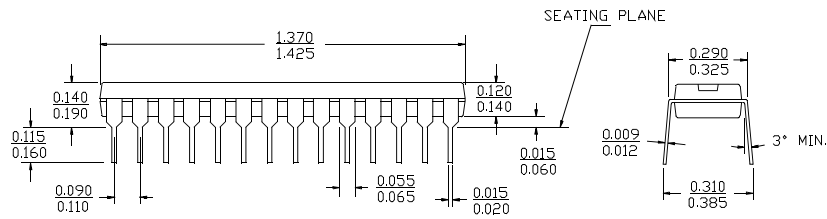
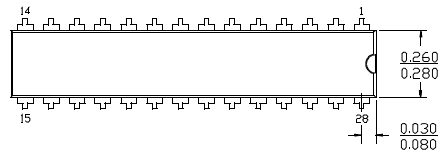
 DIMENSIONS IN INCHES MIN.  
MAX.


	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080



51-85013-A

**28-Lead (300-Mil) Molded DIP P21**

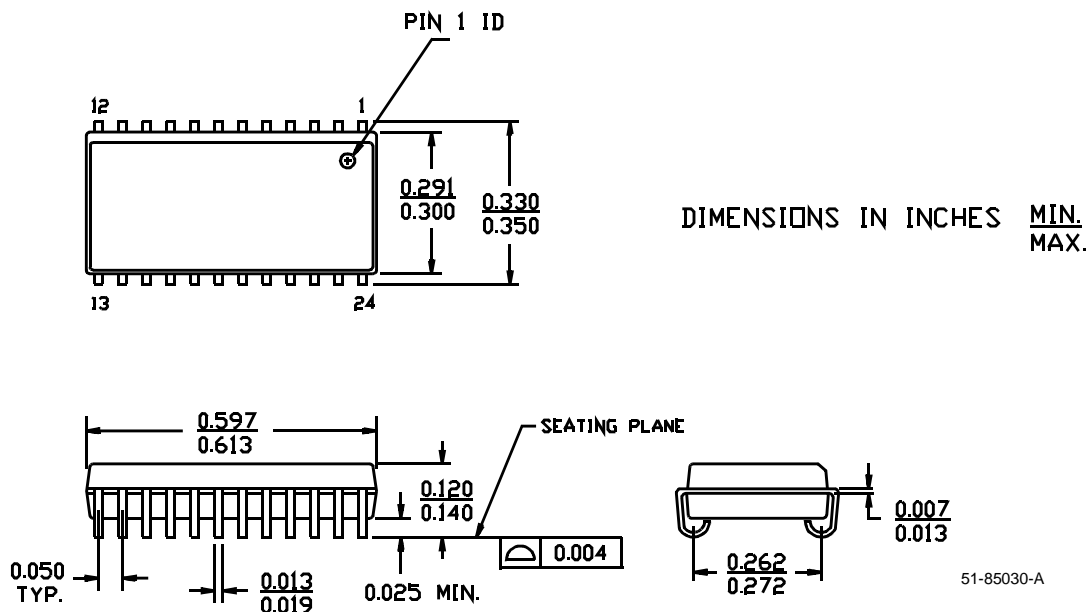
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MAX.


51-85014-B

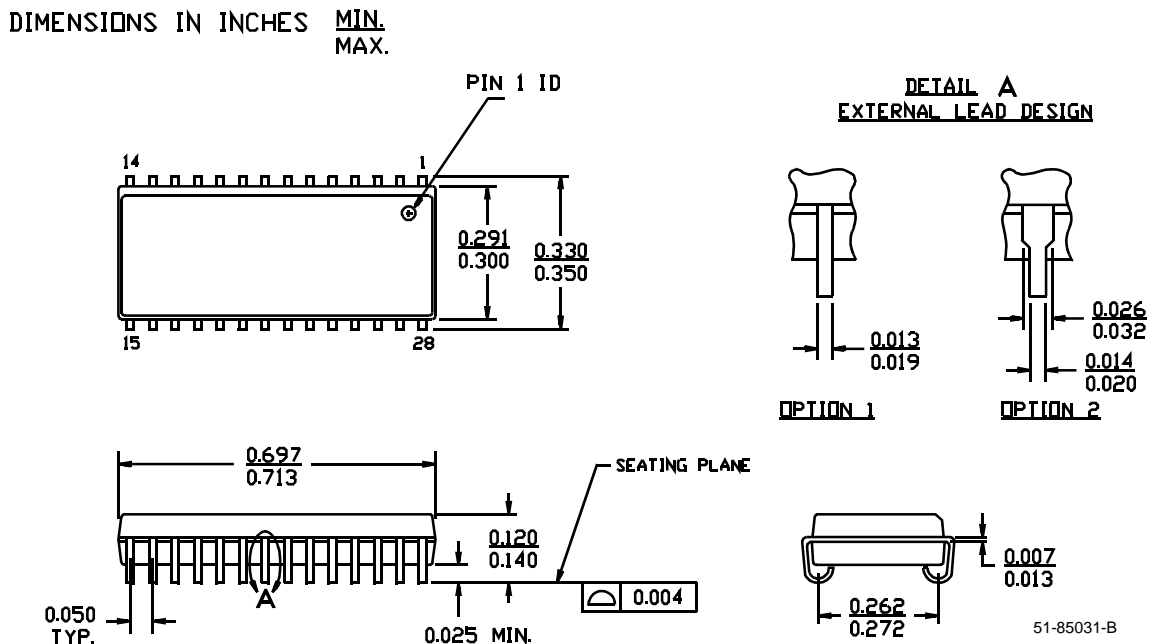


Package Diagrams (continued)

24-Lead (300-Mil) Molded SOJ V13



28-Lead (300-Mil) Molded SOJ V21





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