M66305AP/AFP

TOGGLE LINE BUFFER

DESCRIPTION

M66305A Toggle Line Buffer has two 5,120-bit line buffer memories. It takes in serial data that arrives synchronously with clock pulses and outputs it in serial at a rate of up to 10 Mbits per second synchronously with external clock pulses. This buffer employs the double buffer system: While data is being output, data on the next line can be written on the other line buffer memory.

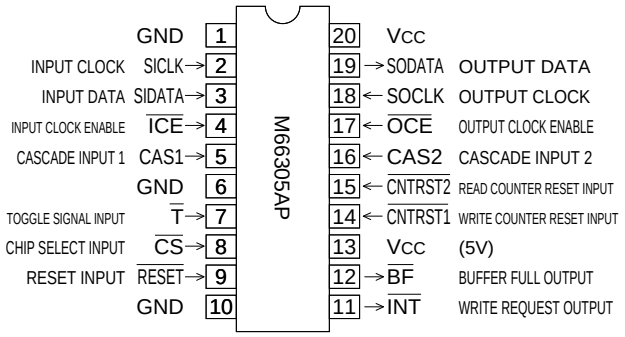
FEATURES

- 5,120 × 1bit serial input-serial output line buffer memories
- Data transmission at 10 megabits/second maximum
- Two line buffer memories can be alternated by external toggle signal.
- Memory capacity can be doubled by cascade connection.
- Because of cascade input pin (CAS1), output potential after completion of output can be set to either H or L.
- Low noise and high fan-out output (I_O = ±24mA guaranteed)
- Every input pin has built-in Schmidt trigger circuit.
- Read counter and write counter can be reset independently.
- $\overline{RESET}$, $\overline{T}$, $\overline{CNTRST1}$ and $\overline{CNTRST2}$ are equipped with negative noise reduction circuit.

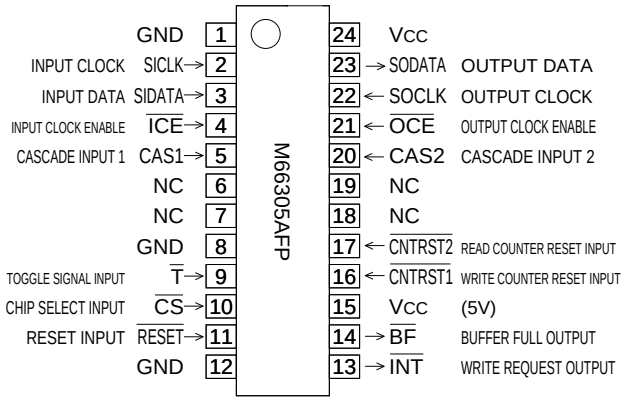
APPLICATION

Data buffer between industrial or home-use image data processing system and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



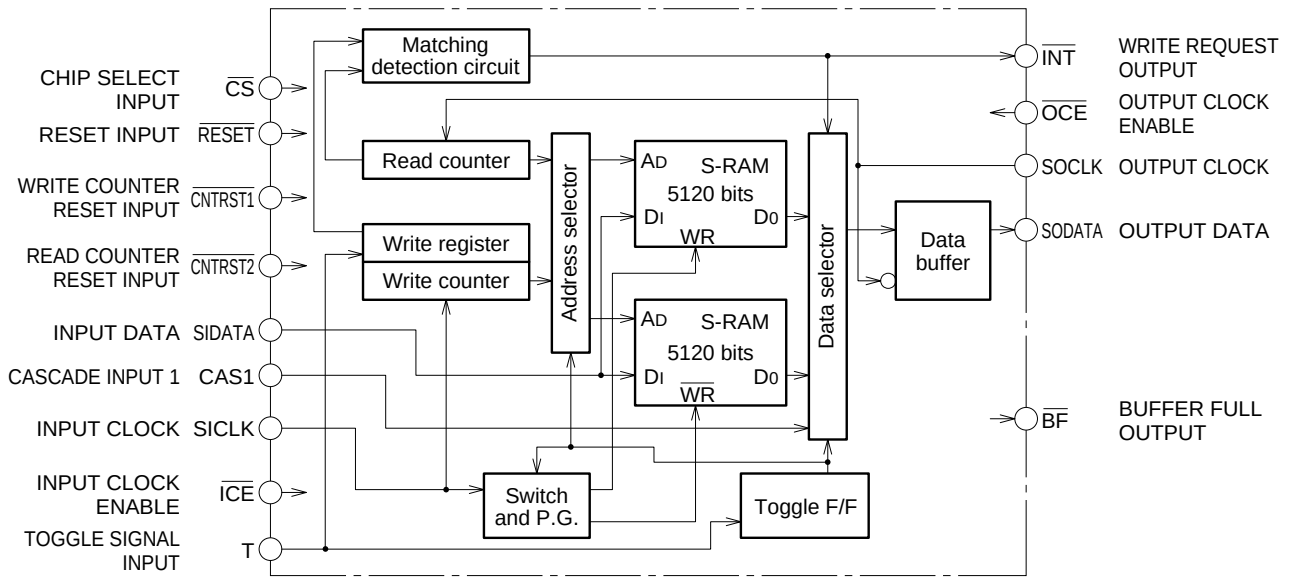
Outline 20P4



Outline 24P2W-A

NC: No Connection

BLOCK DIAGRAM



FUNCTION

When the status of input clock enable ($\overline{ICE}$) is "L", input data (SIDATA) is taken in (written) synchronously with input clock (SICLK) rise edge. When output clock enable ($\overline{OCE}$) is "L", output data (SODATA) is output (read) synchronously with output clock (SOCLK) fall edge. The double buffer system makes independent read and write operation possible.

When one-line write and one-line read are completed, toggle signal ($\overline{T}$) is required to be changed to "L", With input of toggle signal, the line buffer memory which has completed write operation is switched to read mode, and the line buffer which has completed output is switched to write mode, enabling next write and read operations.

To rewrite data during write operation, use write counter reset input ($\overline{CNTRST1}$). To repeat output during output operation, use read counter reset ($\overline{CNTRST2}$).

These operations are possible only when the status of chip select ($\overline{CS}$) is "L".

FUNCTION TABLE

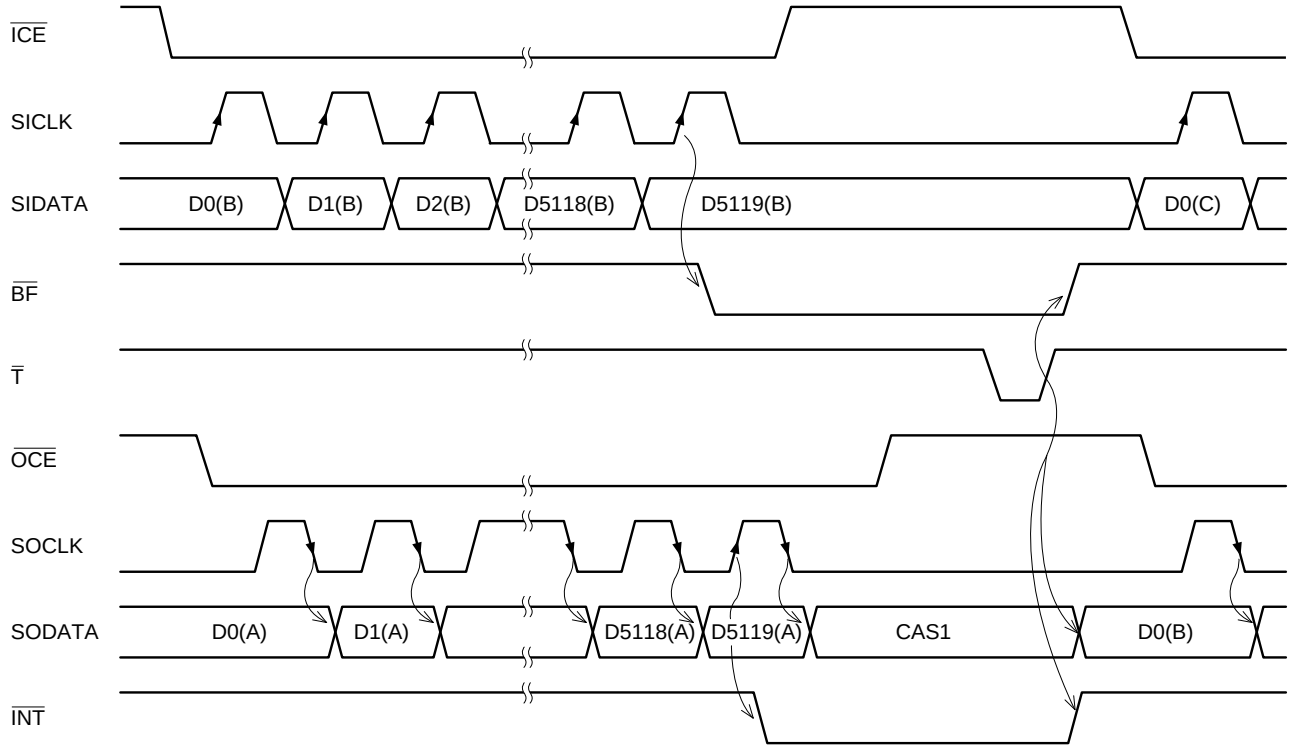
Input									Output			Remarks
$\overline{RES}$	$\overline{CS}$	$\overline{ICE}$	SIC	$\overline{OCE}$	SOC	$\overline{T}$	$\overline{CR1}$	$\overline{CR2}$	SOD	$\overline{INT}$	$\overline{BF}$	
L	X	X	X	X	X	X	X	X	L	H	H	Initialization
H	H	X	X	X	X	X	X	X	Q^0	Q^0	Q^0	No internal change, no output change
H	L	H	X	H	X	H	H	H	Q^0	Q^0	Q^0	No internal change, no output change
H	L	L	⎍	H	X	H	H	H	Q^0	Q^0	*1	With rise of SICLK, data is written on line buffer memory.
H	L	H	X	L	⎍	H	H	H	*2	*3	Q^0	With fall of SOCLK, data is output.
H	L	L	⎍	L	⎍	H	H	H	*2	*3	*1	Write and read
H	L	L	L	X	L	⎍	H	H	*4	H	H	With rise of $\overline{T}$: 1) Line buffer memory in read mode is switched to write mode and the other in write mode is switched to read mode. 2) $\overline{BF}$ and $\overline{INT}$ are canceled.
H	L	H	X	X	L	⎍	H	H				
H	L	L	L	X	X	H	⎍	H	*5	*5	H	With $\overline{CNTRST1}$ input, internal write counter is reset, enabling rewriting.
H	L	H	X	X	X	H	⎍	H				
H	L	X	X	L	L	H	H	⎍	*6	H	*6	With $\overline{CNTRST2}$ input, internal read counter is reset, enabling retrial of output.
H	L	X	X	H	X	H	H	⎍				

Q^0 : No change
x : "H" or "L"
*1 : $\overline{BF}$ changes from "H" to "L" with rise of SICLK for write of 5120th bit.
*2 : With fall of SOCLK, data written before toggle signal input is output in order.
*3 : $\overline{INT}$ changes from "H" to "L" when the status of SOCLK rises after output of final bit of written before toggle signal inputs.
*4 : Outputs the first bit of written data (D_0).
*5 : Output operation can be performed irrespective of $\overline{CNTRST1}$.
*6 : SODATA changes to the first bit of written data (D_0). Write operation can be performed irrespective of $\overline{CNTRST2}$.

PIN DESCRIPTION

Pin	Name	Functions
$\overline{\text{RESET}}$	Reset input	Initializes integrated circuit. (SODATA ="L", $\overline{\text{BF}}$ ="H", $\overline{\text{INT}}$ = "H")
$\overline{\text{CS}}$	Chip select input	"L": Chip select "H": Non-select (Inputs other than $\overline{\text{RESET}}$ have no effects on circuit inside.)
$\overline{\text{ICE}}$	Input clock enable	"L": Input clock (SICLK) enable "H": Input clock (SICLK) disable
SICLK	Input clock	With rise of SICLK, SIDATA is written on line buffer memory.
SIDATA	Input data	
$\overline{\text{OCE}}$	Output clock enable	"L": Output clock (SOCLK) enable "H": Output clock (SOCLK) disable
SOCLK	Output clock	With fall of SOCLK, SODATA is output. Because buffer is provided between memory and output, each piece of data is propagated at a constant rate, irrespective of internal memory read access time.
SODATA	Output data	
$\overline{\text{T}}$	Toggle signal input	The line buffer memory in write mode is switched to read mode, and the other in read mode is switched to write mode.
$\overline{\text{BF}}$	Buffer full output	Output when SICLK rises for input of 5,120th bit, indicating no more writing is possible. When $\overline{\text{BF}}$ is "L", circuit inside is automatically set to "input disable". $\overline{\text{BF}}$ is canceled with rise of toggle signal ($\overline{\text{T}}$) status.
$\overline{\text{INT}}$	Write request output	Output when SOCLK rises after output of final bit of written data. When $\overline{\text{INT}}$ is "L", circuit inside is automatically set to "output disable". $\overline{\text{INT}}$ is canceled with rise of toggle signal ($\overline{\text{T}}$) status.
$\overline{\text{CNTRST1}}$	Write counter reset input	Used to rewrite data during write operation when $\overline{\text{CS}}$ is "L".
$\overline{\text{CNTRST2}}$	Read counter reset input	Used to undo data output halfway or to retry output when $\overline{\text{CS}}$ is "L".
CAS1	Cascade input 1	Output when SOCLK falls after output of final bit of written data. When cascade connection is not used, be sure to connect this pin to V_{CC} or GND.
CAS2	Cascade input 2	Up to 2 cascade connections are possible. Connect the CA2 pin of master IC to V_{CC}, and the CA2 pin of slave IC to GND. Refer to APPLICATION EXAMPLE for details.
NC	No Connection	Non-connected pin provided only for M66305AFP. This pin can be used for wiring.

BASIC TIMING DIAGRAM

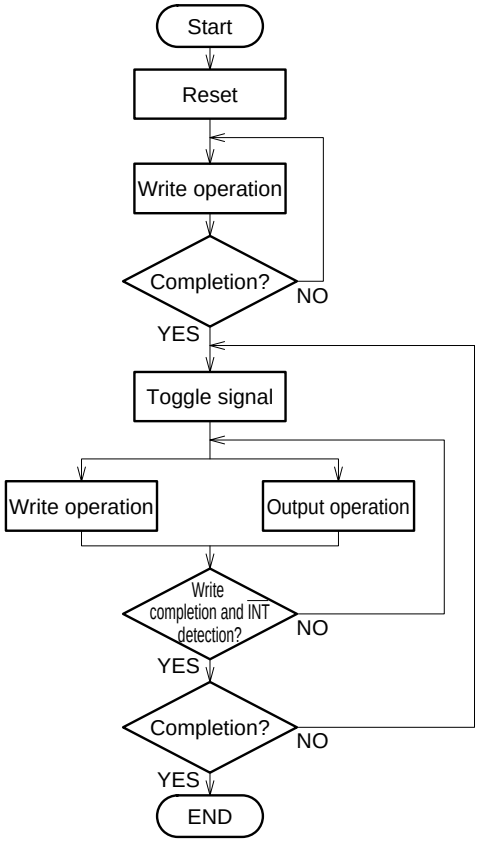


* Circuit operates as shown in this timing chart in case one line length 5,120. If the line length is shorter than this, $\overline{BF}$ stays "H" status.

OPERATION FLOWCHART

During the first cycle of operation after reset, write operation is possible but read operation is impossible. Input toggle signal ($\overline{T}$) after the one-line data is written.

During the second and following cycles, the previous written data can be output or new data can be written in parallel. After one-line data is written and output is completed ($\overline{INT}$ output), input toggle signal ($\overline{T}$).



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
P_d	Power dissipation	mounted	700	mW
T_{stg}	Storage temperature		–65 ~ 150	°C

RECOMMENDED OPERATIONAL CONDITIONS (T_a = –10˚C ~ 70°C unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
GND	Supply voltage			0.0		V
V_I	Input voltage		0.0		V_{CC}	V
V_O	Output voltage		0.0		V_{CC}	V
T_{opr}	Operating ambient temperature		–10		70	°C

ELECTRICAL CHARACTERISTICS (T_a = –10˚C ~ 70°C, V_{CC} = 5V±10% and GND = 0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{T+}	Positive threshold voltage	All input			2.4	V
V_{T-}	Negative threshold voltage		0.6			V
V_{T+} - V_{T-}	Hysteresis width			0.4		V
V_{OH}	“H” output voltage	I_{OH}=–24mA	V_{CC} – 0.8	V_{CC}–0.35*		V
				V_{CC}–0.4**		
V_{OL}	“L” output voltage	I_{OL}=+24mA		0.25*	0.53	V
				0.30**		
I_{CC}	Quiescent supply current	V_I=V_{CC} or GND		55*	130	mA
				45**	110**	
I_{IH}	“H” input current	V_I=5.5V			+1.0	µA
I_{IL}	“L” input current	V_I=0V			–1.0	µA
C_I	Input capacitance				10	pF

The current flowing into the IC is positive current.
*Ta=25˚C
**Ta=70˚C

TIMING CONDITIONS (T_a = –10˚C ~ 70°C, V_{CC} = 5V±10% and GND = 0V unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w\pm}$(SIC)	Input clock pulse width (Note 2)	30			ns
$t_{w\pm}$(SOC)	Output clock pulse width (Note 2)	43*			ns
		50			
$t_{w}(\overline{T})$	Toggle signal input pulse width	150			ns
$t_{w}(\overline{RES})$	Reset input pulse width	100			ns
$t_{w}(\overline{CR1})$	Write counter reset input pulse width	100			ns
$t_{w}(\overline{CR2})$	Read counter reset input pulse width	100			ns
t_{su}(SID-SIC)	Input data setup time before input clock	25			ns
t_{h}(SIC-SID)	Input data hold time after input clock	0			ns
$t_{su}(\overline{ICE}$-SIC)	Input clock enable setup time before input clock	25			ns
t_{h}(SIC-$\overline{ICE}$)	Input clock enable hold time after input clock	0			ns
$t_{su}(\overline{CS}$-SIC)	Chip select setup time before input clock	150			ns
t_{h}(SIC-$\overline{CS}$)	Chip select hold time after input clock	100			ns
$t_{su}(\overline{OCE}$-SOC)	Output clock enable setup time before output clock	25			ns
t_{h}(SOC-$\overline{OCE}$)	Output clock enable hold time after output clock	0			ns
$t_{su}(\overline{CS}$-SOC)	Chip select setup time before output clock	150			ns
t_{h}(SOC-$\overline{CS}$)	Chip select hold time after output clock	100			ns
$t_{su}(\overline{CS}$-$\overline{T})$	Chip select setup time before toggle signal input	100			ns
$t_{h}(\overline{T}$-$\overline{CS})$	Chip select hold time after toggle signal input	100			ns
t_{h}(SIC-$\overline{T}$)	Toggle signal hold time after input clock	100			ns
$t_{rec}(\overline{T}$-SIC)	Input clock recovery time after toggle signal input	150			ns
t_{h}(SOC-$\overline{T}$)	Toggle signal hold time after output clock	100			ns
$t_{rec}(\overline{T}$-SOC)	Output clock recovery time after toggle signal input	150			ns
$t_{su}(\overline{CS}$-$\overline{CR1})$	Chip select setup time before write counter reset	100			ns
$t_{h}(\overline{CR1}$-$\overline{CS})$	Chip select hold time after write counter reset	100			ns
$t_{su}(\overline{CS}$-$\overline{CR2})$	Chip select setup time before read counter reset	100			ns
$t_{h}(\overline{CR2}$-$\overline{CS})$	Chip select hold time after read counter reset	100			ns
$t_{rec}(\overline{R}$-SIC/SOC)	Input and output clock recovery time after reset	100			ns
$t_{rec}(\overline{CR1}$-SIC)	Input clock recovery time after write counter reset	150			ns
$t_{rec}(\overline{CR2}$-SOC)	Output clock recovery time after read counter reset	150			ns

Note 2 To satisfy switching characteristic f_{max} = 10 MHz (frequency: 100ns), the condition shown below should be met: 100 ns ≤ (t_{W+}) + (t_{W-}) *: Ta=25˚C

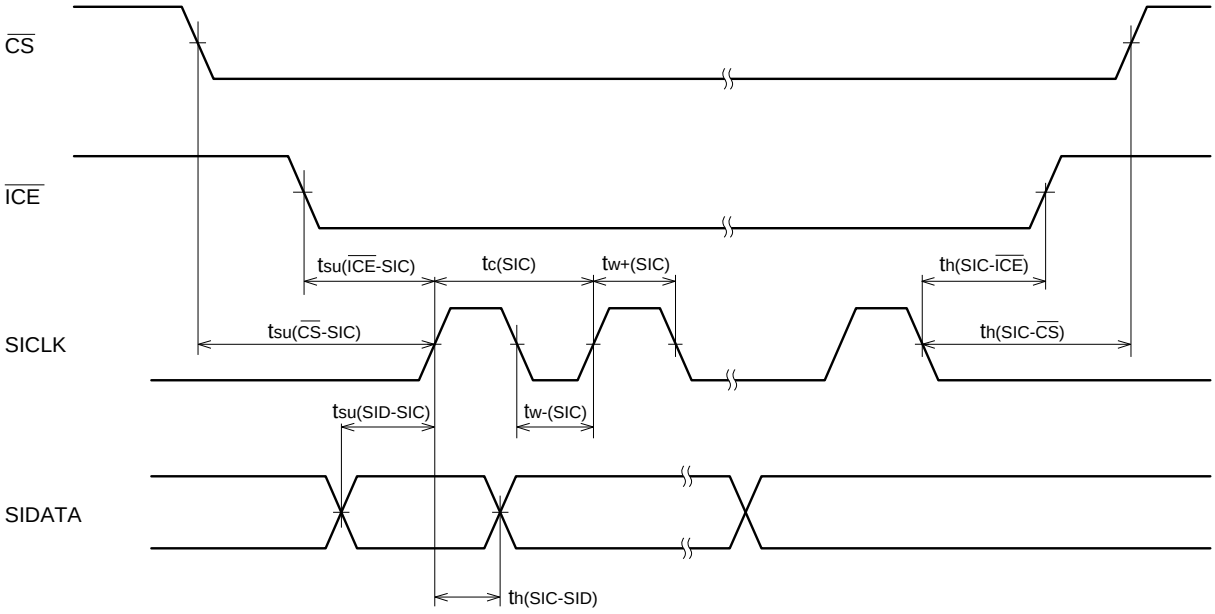
SWITCHING CHARACTERISTICS (T_a = –10˚C ~ 70°C, V_{CC} = 5V±10% and GND = 0V)

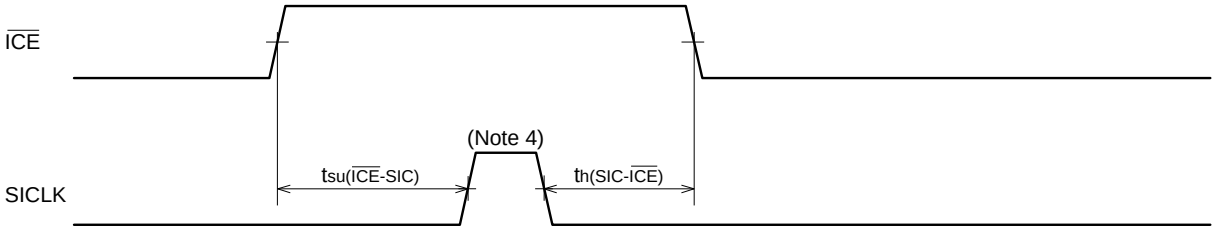
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_C(SIC)	Input clock cycle time		100			ns
t_C(SOC)	Output clock cycle time		100			ns
t_{PLH}(SOC-SOD)	Propagation time between input clock and output data	C_L=50pF			36	ns
		C_L=150pF			40	
t_{PHL}(SOC-SOD)		C_L=50pF			36	ns
		C_L=150pF			40	
t_{PHL}(SIC-$\overline{BF}$)	Propagation time between input clock and $\overline{BF}$	C_L=50pF			75	ns
		C_L=150pF			85	
t_{PHL}(SOC-$\overline{INT}$)	Propagation time between output clock and $\overline{INT}$	C_L=50pF			75	ns
		C_L=150pF			85	
$t_{PLH}(\overline{T}$-$\overline{BF})$	Propagation time between toggle signal input and $\overline{BF}$	C_L=150pF			100	ns
$t_{PLH}(\overline{T}$-$\overline{INT})$	Propagation time between toggle signal input and $\overline{INT}$				100	ns
$t_{PLH}(\overline{R}$-$\overline{BF})$	Propagation time between reset input and $\overline{BF}$				100	ns
$t_{PLH}(\overline{R}$-$\overline{INT})$	Propagation time between reset input and $\overline{INT}$				100	ns
$t_{PHL}(\overline{CR1}$-$\overline{BF})$	Propagation time between write counter reset and $\overline{BF}$				100	ns
$t_{PLH}(\overline{CR2}$-$\overline{INT})$	Propagation time between read counter reset and $\overline{INT}$				100	ns

Note 3 AC test waveform ;
Input pulse level: 0V ~ 3V Input pulse fall time: 6ns
Input pulse rise time: 6ns

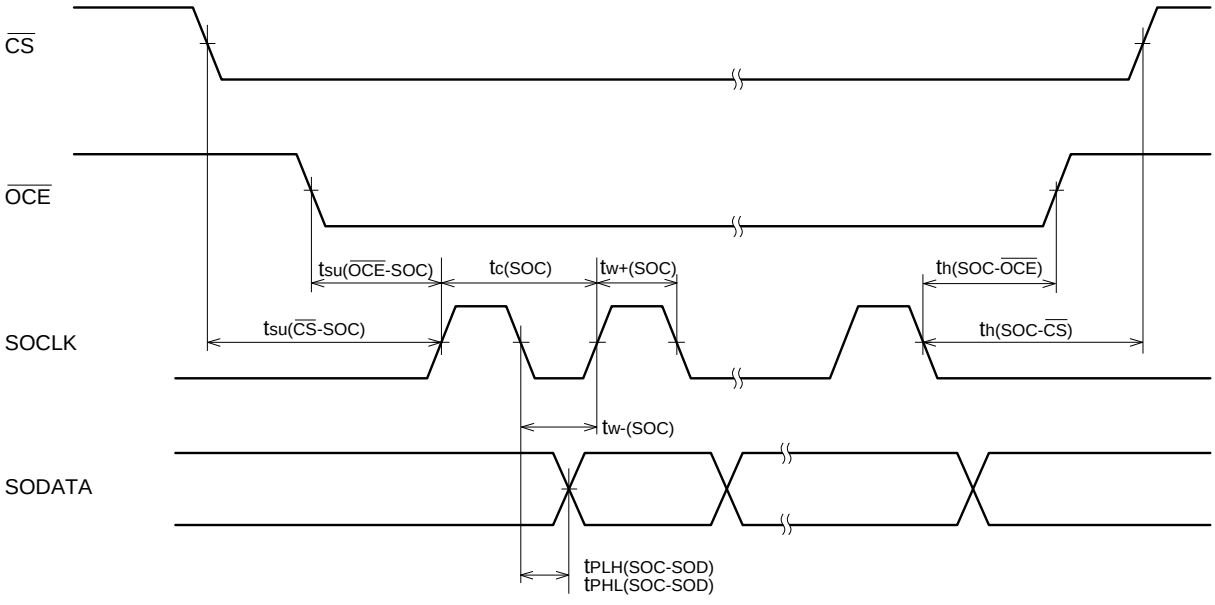
Test voltage ;
Input voltage: 1.3V
Output voltage: 1.3V

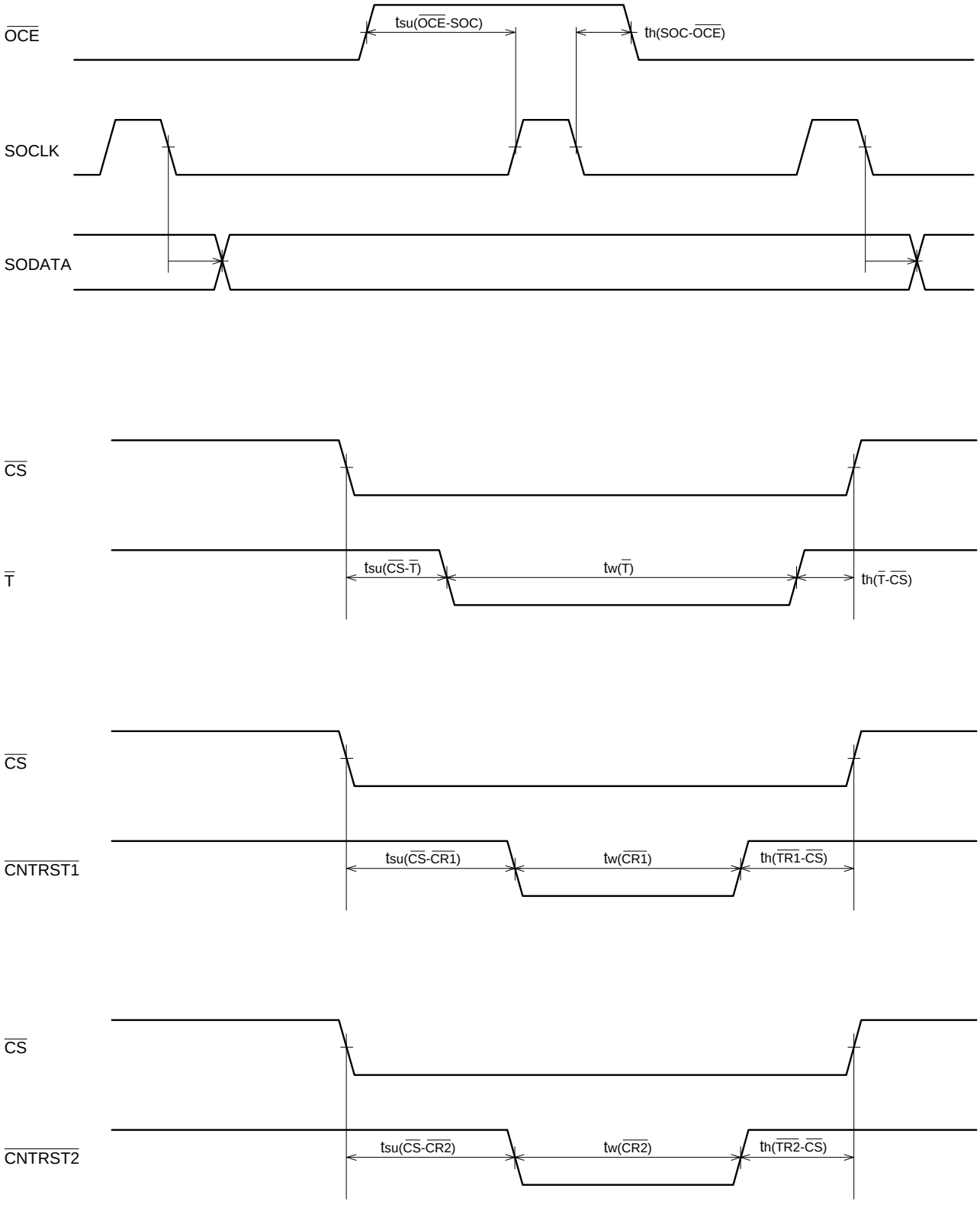
TIMING CHARTS

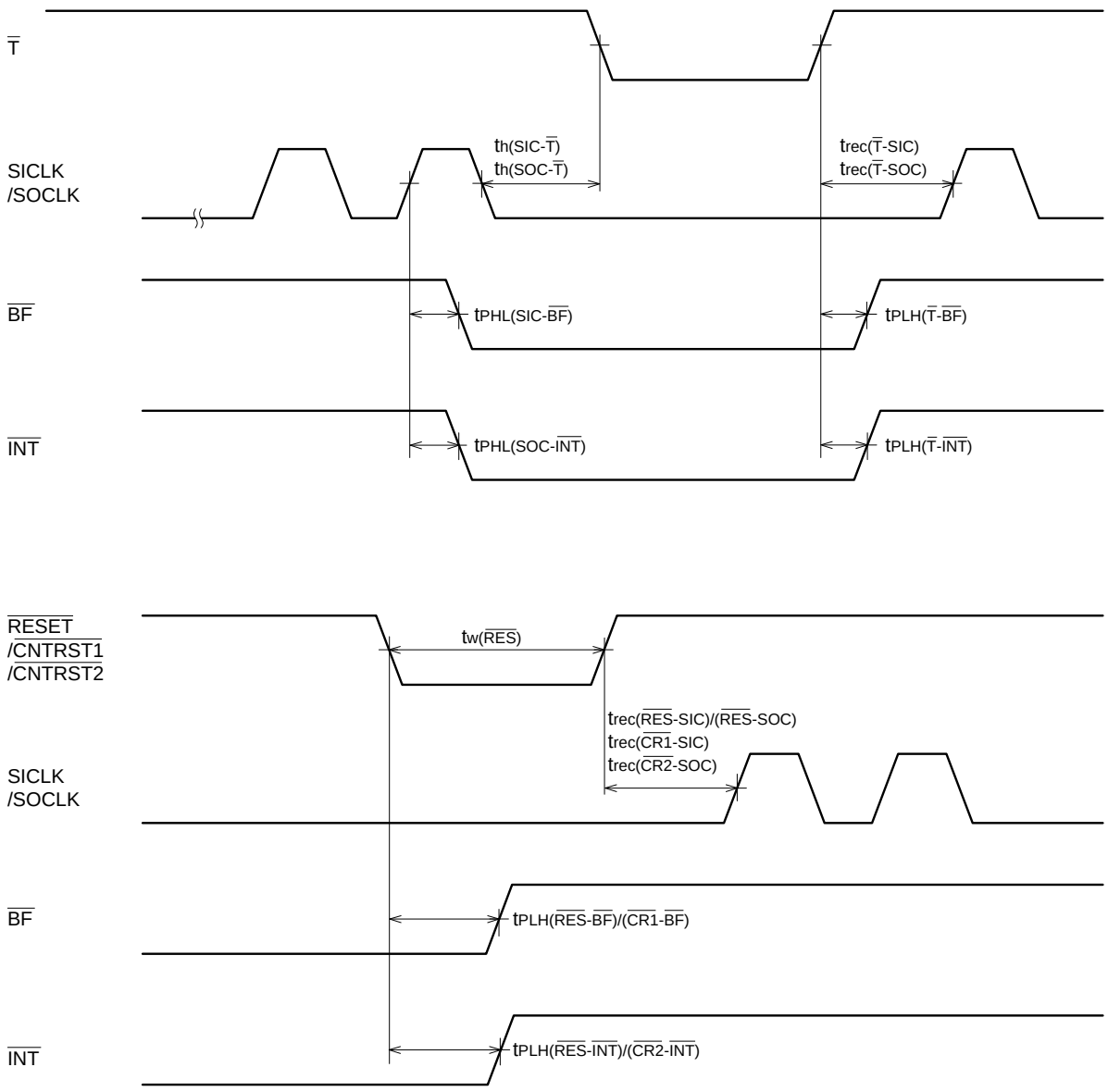




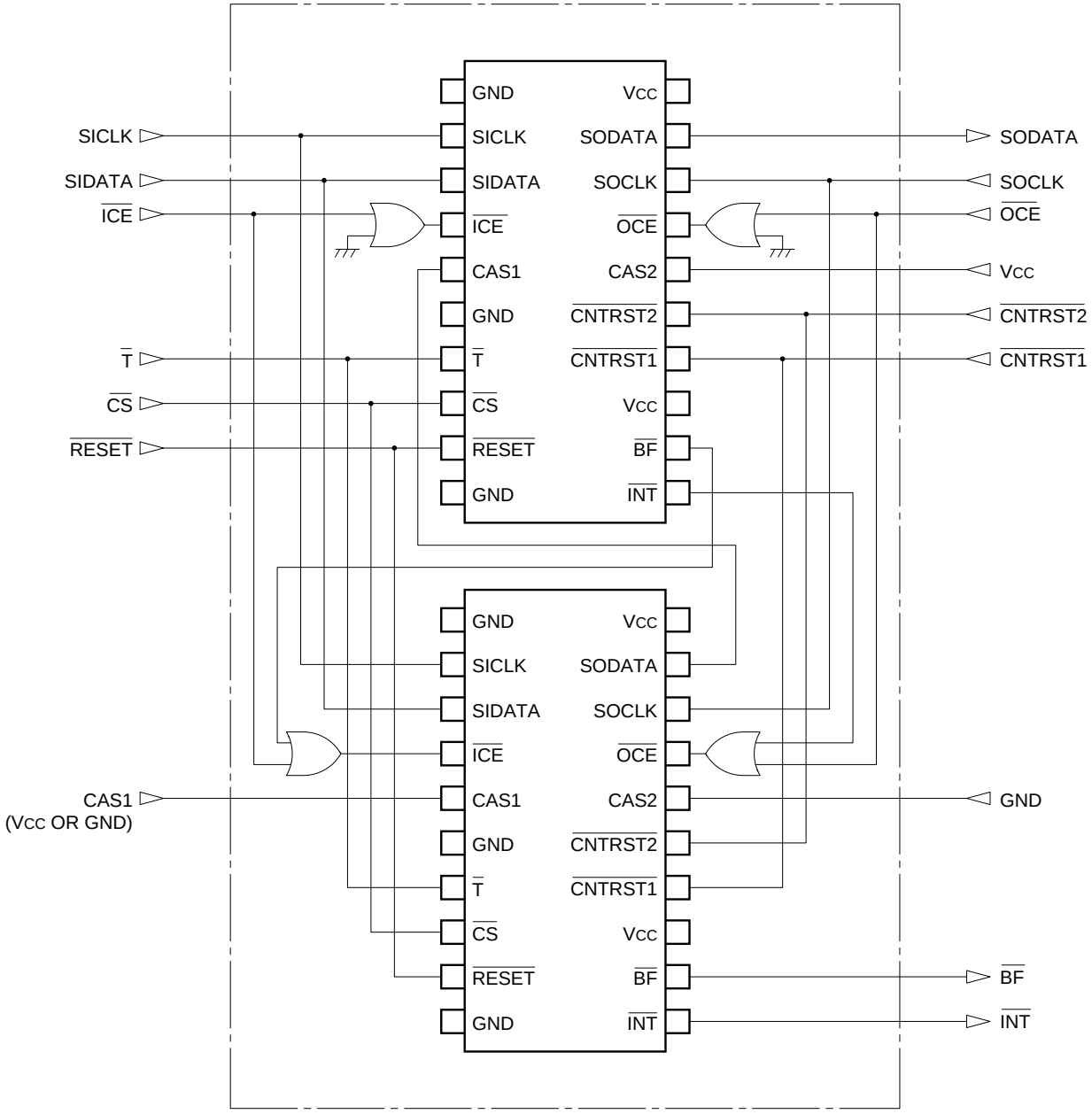
Note 4. Timing to invalidate the clock.




OCE
tsu(OCE-SOC)
th(SOC-OCE)
SOCLK
SODATA
CS
T
tsu(CS-T)
tw(T)
th(T-CS)
CS
CNTRST1
tsu(CS-CR1)
tw(CR1)
th(TR1-CS)
CS
CNTRST2
tsu(CS-CR2)
tw(CR2)
th(TR2-CS)


T
SICLK
/SOCLK
th(SIC-T)
th(SOC-T)
trec(T-SIC)
trec(T-SOC)
BF
tPHL(SIC-BF)
tPLH(T-BF)
INT
tPHL(SOC-INT)
tPLH(T-INT)
RESET
/CNTRST1
/CNTRST2
tw(RES)
trec(RES-SIC)/(RES-SOC)
trec(CR1-SIC)
trec(CR2-SOC)
SICLK
/SOCLK
BF
tPLH(RES-BF)/(CR1-BF)
INT
tPLH(RES-INT)/(CR2-INT)

APPLICATION EXAMPLE



Note 5.
Output clock recovery time after toggle signal input [$t_{re(\overline{T}\text{-SOC})}$:
1) When one line length is 5,125 bits (5,120 +5) or less, $t_{rec(\overline{T}\text{-SOC})}$ is required to be 500 ns or more.
2) When one line length is 5,126 bits (5,120 +6) or more, $t_{rec(\overline{T}\text{-SOC})}$ is required to be 150 ns or more.

Note 6.
ICs used in this example connection:
M66305A: 2pcs.
M74HC32: 1pc.