

M63823P/FP/GP

7-UNIT 500mA DARLINGTON TRANSISTOR-ARRAY WITH CLAMP DIODE

DESCRIPTION

M63823P, M63823FP and M63823GP are seven-circuit Darlington transistor arrays with clamping diodes. The circuits are made of NPN transistors. Both the semi-conductor integrated circuits perform high-current driving with extremely low input-current supply.

Production lineup has been newly expanded with the addition of 225mil (GP) package.

M63823P and M63823FP have the same pin connection as M54523P and M54523FP. (Compatible with M54523P and M54523FP) More over, the features of M63823P and M63823FP are equal or superior to those of M54523P and M54523FP.

FEATURES

- Three package configurations (P, FP and GP)
- Pin connection Compatible with M54523P and M54523FP
- High breakdown voltage ($BV_{CEO} \geq 50V$)
- High-current driving ($I_{C(max)} = 500mA$)
- With clamping diodes
- PMOS Compatible input
- Wide operating temperature range ($T_a = -40$ to $+85^\circ C$)

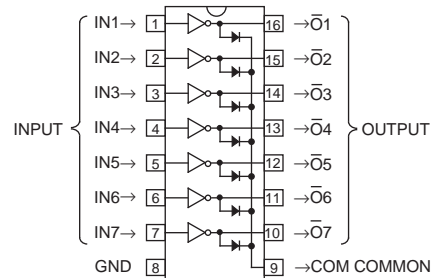
APPLICATION

Drives of relays and printers, digit drives of indication elements (LEDs and lamps), and MOS-bipolar logic IC interfaces

FUNCTION

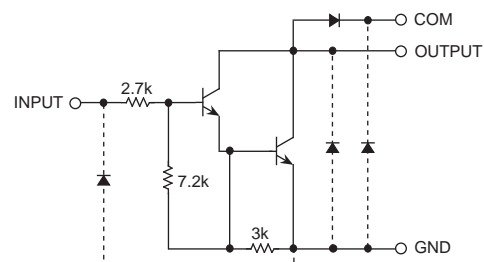
The M63823P, M63823FP and M63823GP each have seven circuits consisting of NPN Darlington transistors. These ICs have resistance of $2.7k\Omega$ between input transistor bases and input pins. A spike-killer clamping diode is provided between each output pin (collector) and COM pin (pin 9). The output transistor emitters are all connected to the GND pin (pin 8). The collector current is 500mA maximum. Collector-emitter supply voltage is 50V maximum. The M63823FP and M63823GP is enclosed in molded small flat package, enabling space-saving design.

PIN CONFIGURATION



16P4(P)
16P2N-A(FP)
Package type 16P2S-A(GP)

CIRCUIT DIAGRAM



The seven circuits share the COM and GND
The diode, indicated with the dotted line, is parasitic, and cannot be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_a = -40 \sim +85^\circ C$)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Collector-emitter voltage	Output, H	$-0.5 \sim +50$	V
I_C	Collector current	Current per circuit output, L	500	mA
V_i	Input voltage		$-0.5 \sim +30$	V
I_F	Clamping diode forward current		500	mA
V_R	Clamping diode reverse voltage		50	V
P_d	Power dissipation	$T_a = 25^\circ C$, when mounted on board	1.47(P)/1.00(FP)/0.80(GP)	W
T_{opr}	Operating temperature		$-40 \sim +85$	$^\circ C$
T_{stg}	Storage temperature		$-55 \sim +125$	$^\circ C$

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RECOMMENDED OPERATING CONDITIONS (Unless otherwise noted, Ta = -40 ~ +85°C)

Symbol	Parameter	Limits			Unit	
		min	typ	max		
V _O	Output voltage	0	—	50	V	
I _C	Collector current (Current per 1 circuit when 7 circuits are coming on simultaneously)	Duty Cycle P : no more than 8% FP : no more than 5% GP : no more than 4%	0	—	400	mA
		Duty Cycle P : no more than 30% FP : no more than 20% GP : no more than 15%	0	—	200	
V _{IH}	"H" input voltage	I _C ≤ 400mA	3.85	—	25	V
V _{IL}	"L" input voltage	I _C ≤ 200mA	3.4	—	25	V
			0	—	0.6	

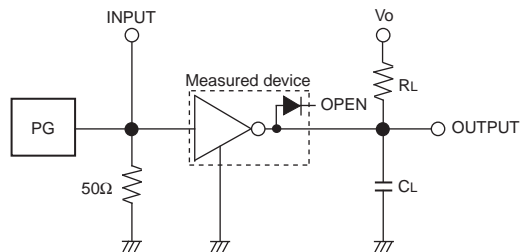
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
V (BR) CEO	Collector-emitter breakdown voltage	I _{CEO} = 100μA	50	—	—	V
V _{CE(sat)}	Collector-emitter saturation voltage	I _I = 500μA, I _C = 350mA	—	1.2	1.6	V
		I _I = 350μA, I _C = 200mA	—	1.0	1.3	
		I _I = 250μA, I _C = 100mA	—	0.9	1.1	
I _I	Input current	V _I = 3.85V	—	0.9	1.4	mA
V _F	Clamping diode forward voltage	I _F = 350mA	—	1.4	2.0	V
I _R	Clamping diode reverse current	V _R = 50V	—	—	100	μA
h _{FE}	DC amplification factor	V _{CE} = 4V, I _C = 350mA	1000	2000	—	—

SWITCHING CHARACTERISTICS (Unless otherwise noted, Ta = 25°C)

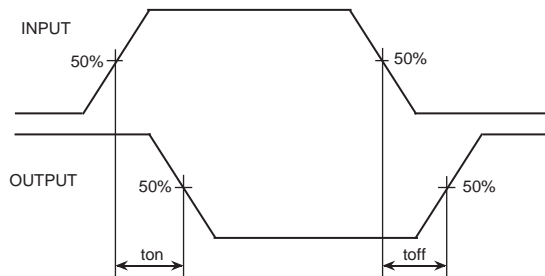
Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
t _{on}	Turn-on time	C _L = 15pF (note 1)	—	15	—	ns
t _{off}	Turn-off time		—	350	—	ns

NOTE 1 TEST CIRCUIT



- (1) Pulse generator (PG) characteristics : PRR=1kHz,
t_w = 10μs, t_r = 6ns, t_f = 6ns, Z_o = 50Ω
V_P = 3.85V_{P-P}
- (2) Input-output conditions : R_L = 25Ω, V_O = 10V
- (3) Electrostatic capacity C_L includes floating capacitance at connections and input capacitance at probes

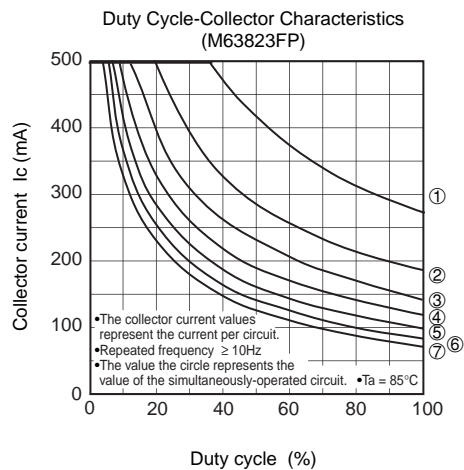
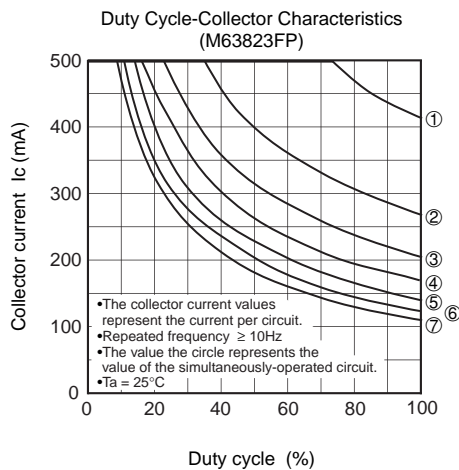
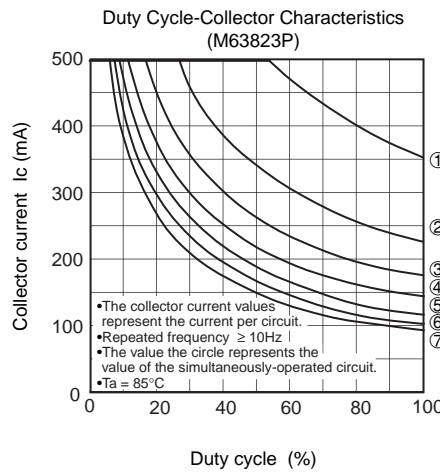
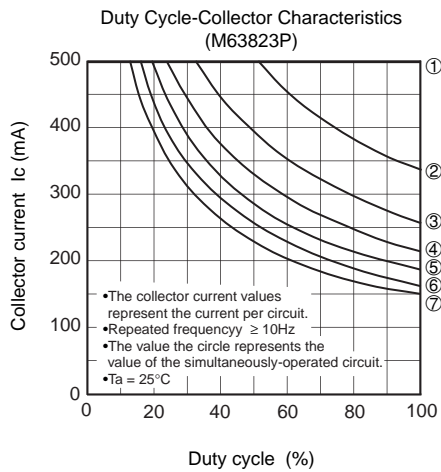
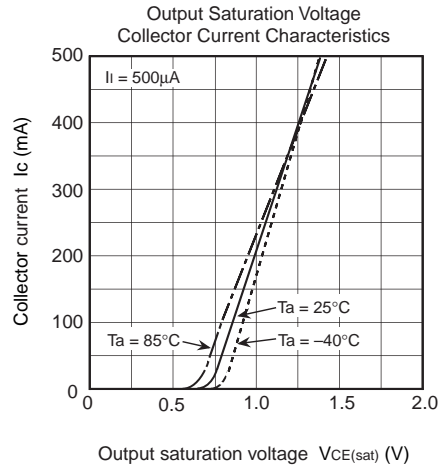
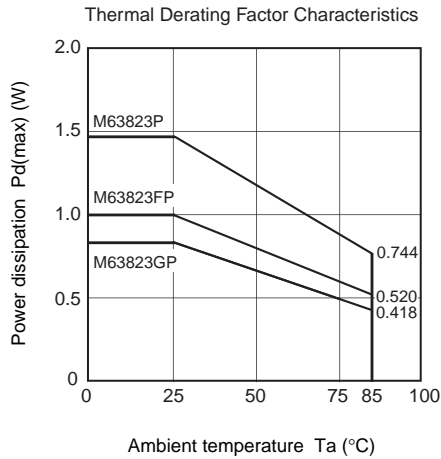
TIMING DIAGRAM



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TYPICAL CHARACTERISTICS



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