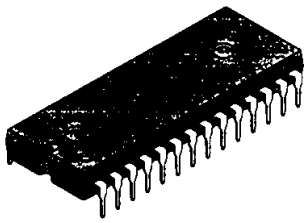
# SONY CXK5864BP/BSP/BM -70L/10L/12L/ -70LL/10LL/12LL

## 8,192-word × 8-bit High Speed CMOS Static RAM *Maintenance Only*

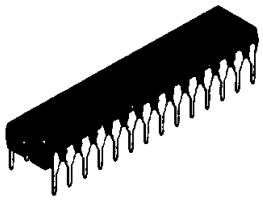
### Description

CXK5864BP/BSP/BM are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8 bits and operates from a single 5V supply. These IC are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

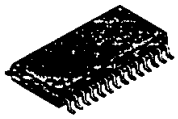
CXK5864BP
28 pin DIP (Plastic)



CXK5864BSP
28 pin DIP (Plastic)



CXK5864BM
28 pin SOP (Plastic)



### Features

- Fast access time (Access time)
  CXK5864BP/BSP/BM-70L, 70LL 70ns(Max.)
  CXK5864BP/BSP/BM-10L, 10LL 100ns(Max.)
  CXK5864BP/BSP/BM-12L, 12LL 120ns(Max.)
- Low power operation :
  CXK5864BP/BSP/BM-70LL, 10LL, 12LL ;
  Standby/Operation : 5 μW (Typ.) /40mW (Typ.)
  CXK5864BP/BSP/BM-70L, 10L, 12L ;
  Standby/Operation : 10 μW (Typ.) /40mW (Typ.)
- Single power supply 5V : +5V ± 10%
- Fully static memory ··· No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs
- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

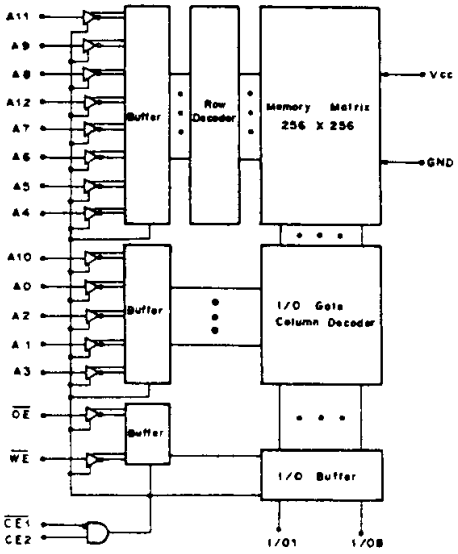
### Function

8,192-word × 8-bit static RAM

### Structure

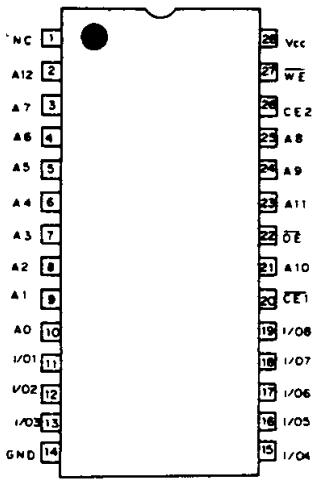
Silicon gate CMOS IC

### Block Diagram




### Pin Configuration

(Top View)




### Pin Description

| Symbol | Description |
|---|---|
| A0 to A12 | Address input |
| I/O1 to I/O8 | Data input output |
| $\overline{CE1}$, CE2 | Chip enable 1, 2 input |
| $\overline{WE}$ | Write enable input |
| $\overline{OE}$ | Output enable input |
| Vcc | +5V Power supply |
| GND | Ground |
| NC | No connection |

E89720B0Y – ST

## Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

| Item | Symbol | | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | − 0.5 to + 7.0 | V |
| Input voltage | $V_{IN}$ | | − 0.5* to $V_{CC}$ + 0.5 | V |
| Input and output voltage | $V_{I/O}$ | | − 0.5* to $V_{CC}$ + 0.5 | V |
| Allowable power dissipation | $P_D$ | CXK5864BP/BSP | 1.0 | W |
| | | CXK5864BM | 0.7 | |
| Operating temperature | Topr | | 0 to + 70 | ℃ |
| Storage temperature | Tstg | | − 55 to + 150 | ℃ |
| Soldering temperature • time | Tsolder | | 260 • 10 | ℃ • sec |

* $V_{IN}$, $V_{I/O}$ = − 3.0V Min. for pulse width less than 50ns.

## Truth Table

| $\overline{CE1}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | Mode | I/O1 to I/O8 | $V_{CC}$ Current |
|---|---|---|---|---|---|---|
| H | X | X | X | Not selected | High Z | $I_{SB1}$, $I_{SB2}$ |
| X | L | X | X | Not selected | High Z | $I_{SB1}$, $I_{SB2}$ |
| L | H | H | H | Output disable | High Z | $I_{CC1}$, $I_{CC2}$ |
| L | H | L | H | Read | Data out | $I_{CC1}$, $I_{CC2}$ |
| L | H | X | L | Write | Data in | $I_{CC1}$, $I_{CC2}$ |

X : "H" or "L"

## DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input high voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | − 0.3* | — | 0.8 | V |

* $V_{IL}$ = − 3.0V Min. for pulse width less than 50ns.

5

## Electrical Characteristics

### • DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

| Item | Symbol | Test conditions | | −70L/10L/12L −70LL/10LL/12LL | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.* | Max. | |
| Input leak current | $I_{LI}$ | $V_{IN}$ = GND to Vcc | | −500 | — | 500 | nA |
| Output leak current | $I_{LO}$ | $V_{I/O}$ = GND to Vcc<br>$\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ or<br>$\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ | | −500 | — | 500 | nA |
| Operating supply current | $I_{CC1}$ | $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$,<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$,<br>$I_{OUT}$ = 0mA | | — | 8 | 15 | mA |
| Average operating current | $I_{CC2}$ | Min. cycle<br>Duty = 100%, $I_{OUT}$ = 0mA | | — | 30 | 50 | mA |
| Standby current | $I_{SB1}$ | CE2 ≦ 0.2V<br>or $\overline{CE1}$ ≧ Vcc − 0.2V<br>CE2 ≧ Vcc − 0.2V | − L | — | 2 | 60 | µA |
| | | | − LL | — | 1 | 30 | |
| | $I_{SB2}$ | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ | | — | 0.1 | 2 | mA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = −1.0mA | | 2.4 | — | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2.1mA | | — | — | 0.4 | V |

* Vcc = 5V, Ta = 25°C

### Pin capacitance

(Ta = 25°C, f = 1MHz)

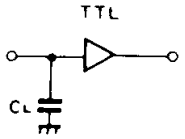
| Item | Symbol | Test conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0V | — | 7 | pF |
| Input/Output capacitance | $C_{I/O}$ | $V_{I/O}$ = 0V | — | 7 | pF |

**Note**) This parameter is sampled and is not 100% tested.

### AC characteristics

### • AC test conditions (Vcc = 5V ± 10%, Ta = 0 to +70°C)

| Item | | Conditions |
|---|---|---|
| Input pulse high level | | $V_{IH}$ = 2.2V |
| Input pulse low level | | $V_{IL}$ = 0.8V |
| Input rise time | | tr = 5ns |
| Input fall time | | tf = 5ns |
| Input and output reference level | | 1.5V |
| Output load conditions | 10L/10LL/12L/12LL | $C_L$* = 100pF, 1TTL |
| | 70L/70LL | $C_L$* = 30pF, 1TTL |




* $C_L$ includes scope and jig capacitances.

## ● Read cycle

| Item | Symbol | −70L/70LL | | −10L/10LL | | −12L/12LL | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read cycle time | $t_{RC}$ | 70 | — | 100 | — | 120 | — | ns |
| Address access time | $t_{AA}$ | — | 70 | — | 100 | — | 120 | ns |
| Chip enable access time ($\overline{CE1}$, CE2) | $t_{CO1}$<br>$t_{CO2}$ | — | 70 | — | 100 | — | 120 | ns |
| Output enable to output valid | $t_{OE}$ | — | 35 | — | 50 | — | 60 | ns |
| Output hold from address change | $t_{OH}$ | 10 | — | 10 | — | 10 | — | ns |
| Chip enable to output in low Z ($\overline{CE1}$, CE2) | $t_{LZ1}$<br>$t_{LZ2}$ | 10 | — | 10 | — | 10 | — | ns |
| Output enable to output in low Z ($\overline{OE}$) | $t_{OLZ}$ | 5 | — | 5 | — | 5 | — | ns |
| Chip disable to output in high Z ($\overline{CE1}$, CE2) | $t_{HZ1}$ *<br>$t_{HZ2}$ * | 0 | 30 | 0 | 35 | 0 | 45 | ns |
| Output disable to output in high Z ($\overline{OE}$) | $t_{OHZ}$ * | 0 | 30 | 0 | 35 | 0 | 45 | ns |

* $t_{HZ1}$, $t_{HZ2}$ and $t_{OHZ}$ are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

## ● Write cycle

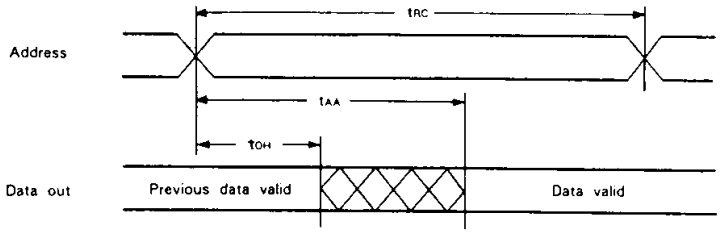
| Item | Symbol | −70L/70LL | | −10L/10LL | | −12L/12LL | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write cycle time | $t_{WC}$ | 70 | — | 100 | — | 120 | — | ns |
| Address valid to end of write | $t_{AW}$ | 60 | — | 80 | — | 85 | — | ns |
| Chip enable to end of write | $t_{CW}$ | 60 | — | 80 | — | 85 | — | ns |
| Data to write time overlap | $t_{DW}$ | 30 | — | 35 | — | 50 | — | ns |
| Data hold from write time | $t_{DH}$ | 0 | — | 0 | — | 0 | — | ns |
| Write pulse width | $t_{WP}$ | 40 | — | 60 | — | 70 | — | ns |
| Address setup time | $t_{AS}$ | 0 | — | 0 | — | 0 | — | ns |
| Write recovery time ($\overline{WE}$) | $t_{WR}$ | 0 | — | 0 | — | 0 | — | ns |
| Write recovery time ($\overline{CE1}$, CE2) | $t_{WR1}$ | 0 | — | 0 | — | 0 | — | ns |
| Output active from end of write | $t_{OW}$ | 5 | — | 5 | — | 5 | — | ns |
| Write to output in high Z | $t_{WHZ}$ * | 0 | 30 | 0 | 35 | 0 | 45 | ns |

* $t_{WHZ}$ is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

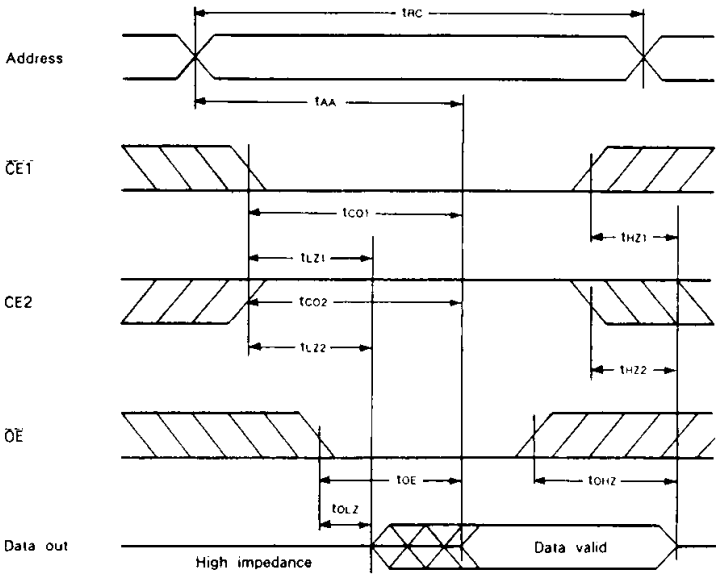
5

## Timing Waveform

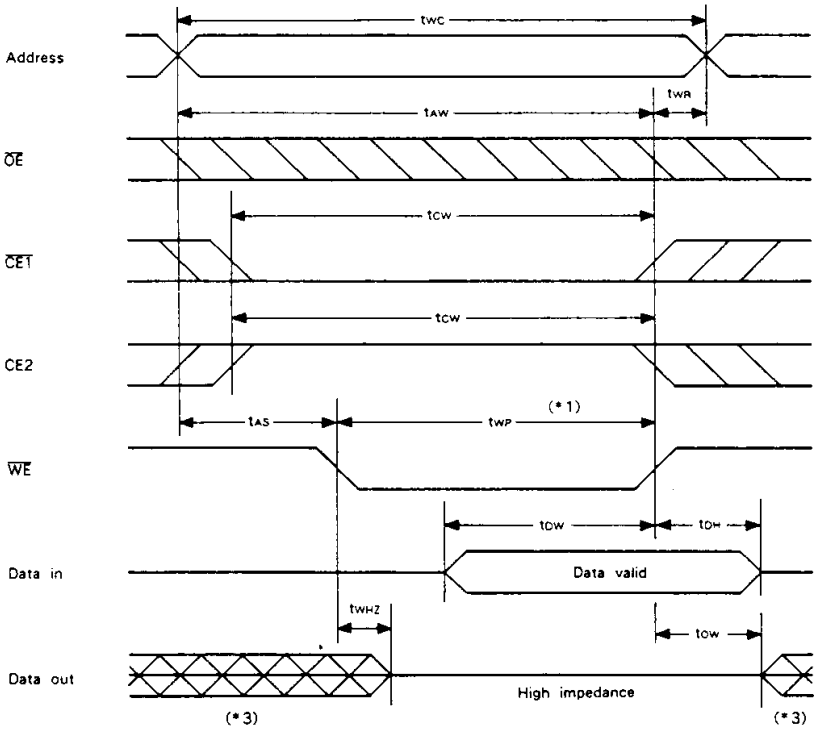
• Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



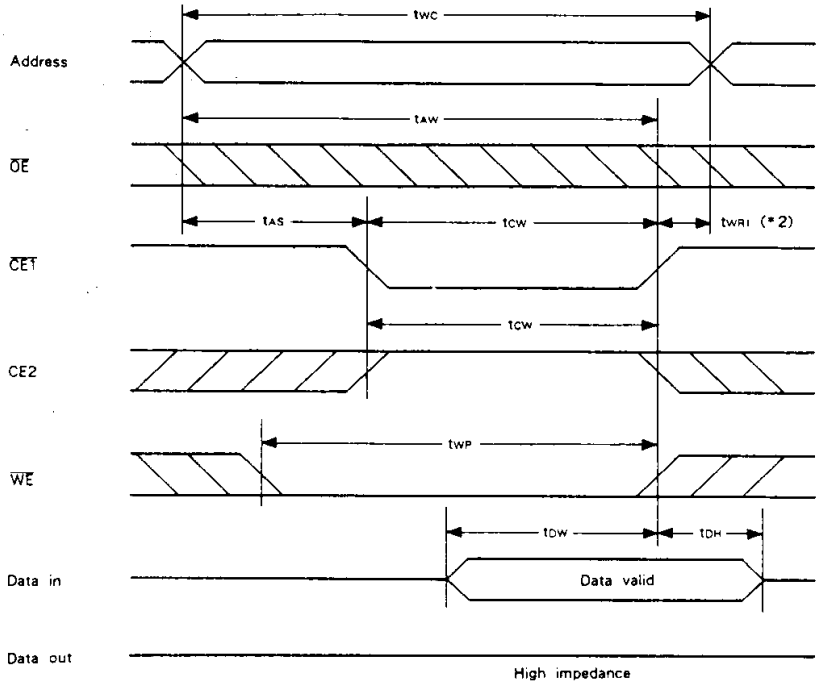

• Read cycle (2) : $\overline{WE} = V_{IH}$



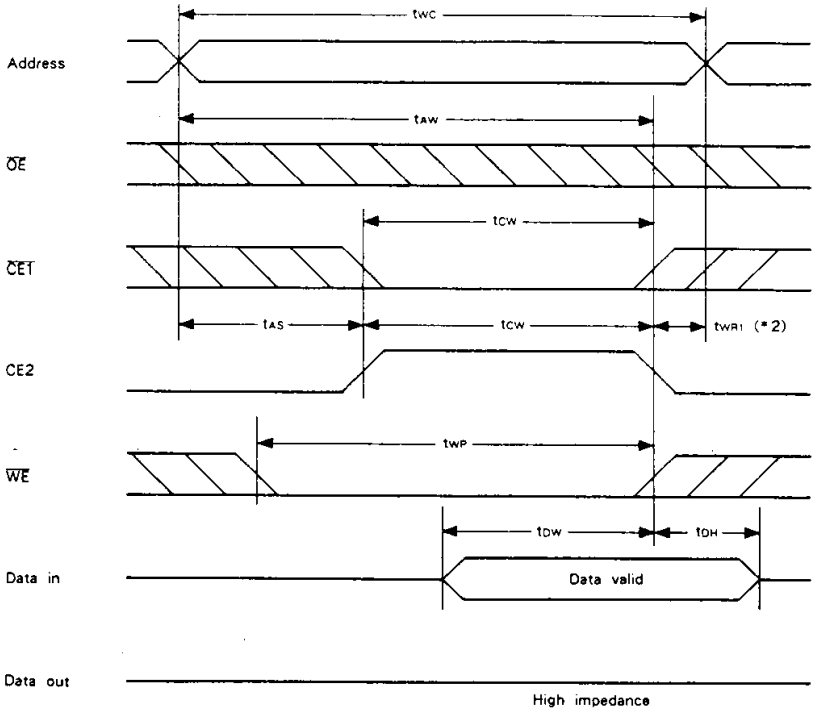

• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control




• Write cycle (3) : CE2 control




**Note)**

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2. $t_{WR1}$ is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

*3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

5

## Data Retention Characteristics

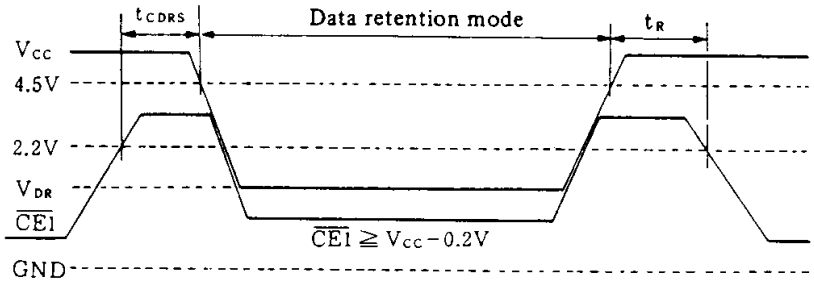
(Ta = 0 to + 70°C)

| Item | Symbol | Test conditions | | −70L/10L/12L | | | −70LL/10LL/12LL | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Data retention voltage | $V_{DR}$ | *1 | | 2.0 | — | 5.5 | 2.0 | — | 5.5 | V |
| Data retention current | $I_{CCDR1}$ | *1 Vcc = 3.0V | Ta = 0°C to 70°C | — | 1 | 35 | — | 0.5 | 15 | µA |
| | | | Ta = 0°C to 40°C | — | — | — | — | — | 3 | |
| | $I_{CCDR2}$ | Vcc = 2.0 to 5.5V, *1 | | — | 2 | 60 | — | 1 | 30 | µA |
| Data retention setup time | $t_{CDRS}$ | Chip disable to data retention mode | | 0 | — | — | 0 | — | — | ns |
| Recovery time | $t_R$ | | | $t_{RC}$*2 | — | — | $t_{RC}$*2 | — | — | ns |

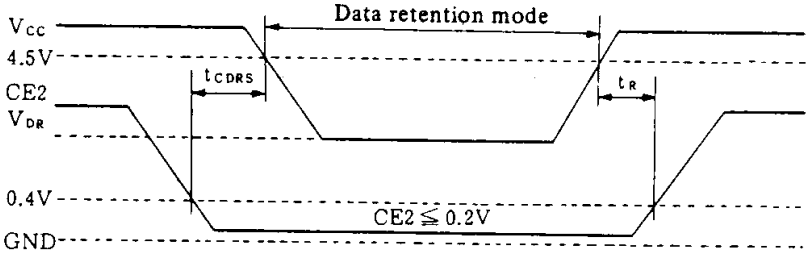
* 1. $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ [$\overline{CE1}$ Control] or $CE2 \leqq 0.2V$ [CE2 Control]
* 2. $t_{RC}$ : Read cycle time

## Data Retention Waveform

1. $\overline{CE1}$ control

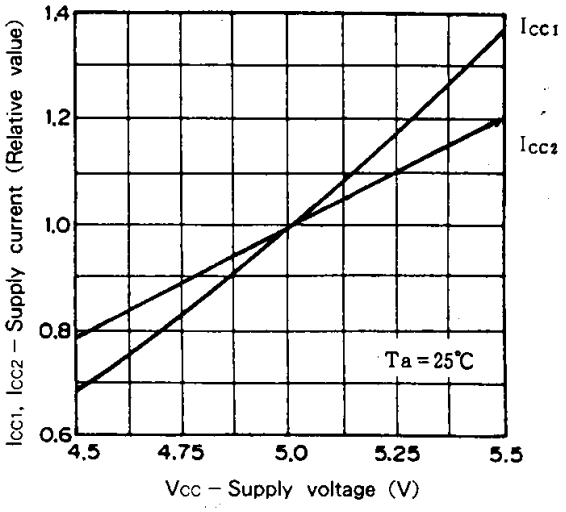



2. CE2 control

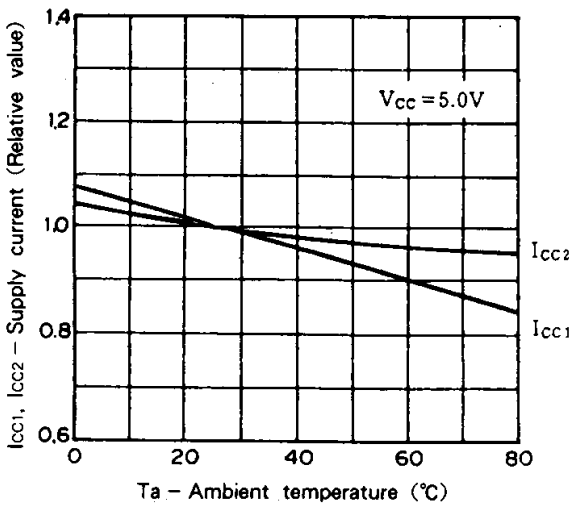


## Example of Representative Characteristics

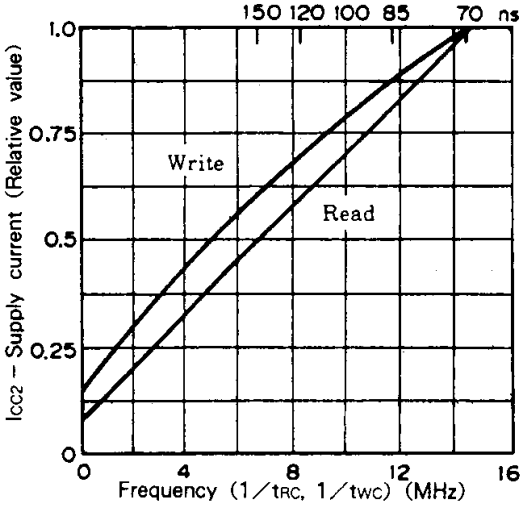
**Supply current vs. Supply voltage**



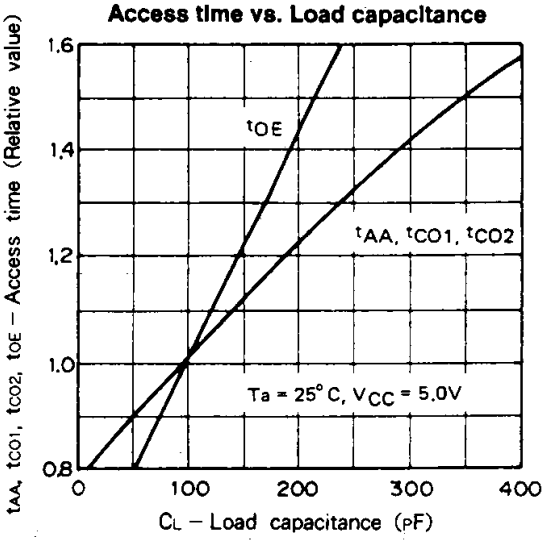

**Supply current vs. Ambient temperature**



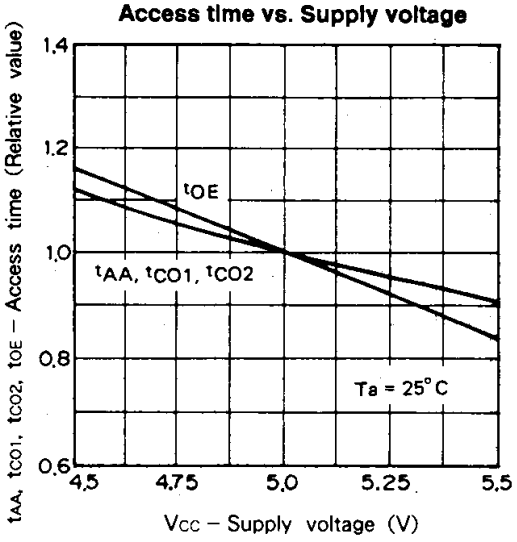

**Supply current vs. Frequency**



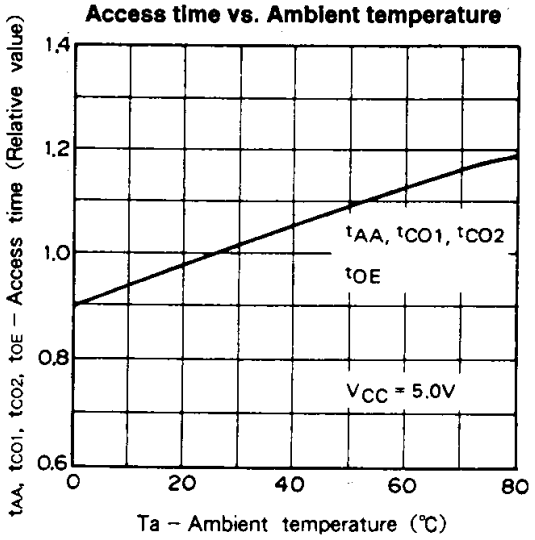

**Access time vs. Load capacitance**




**Access time vs. Supply voltage**

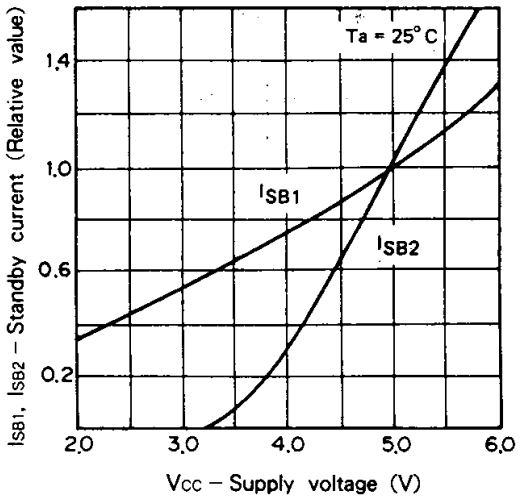



**Access time vs. Ambient temperature**

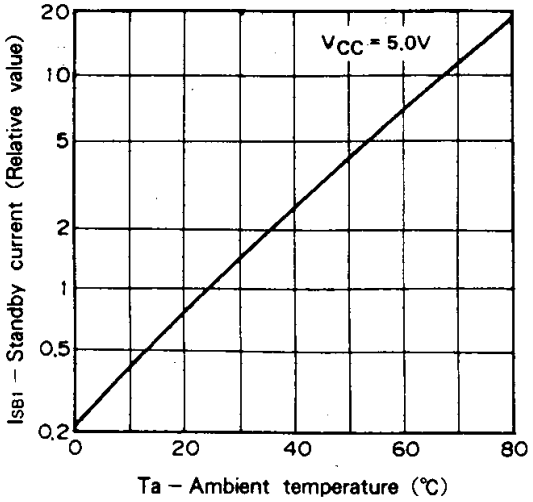



5

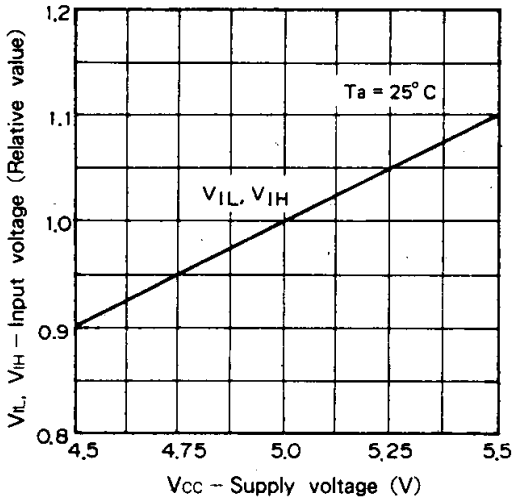
**Standby current vs. Supply voltage**



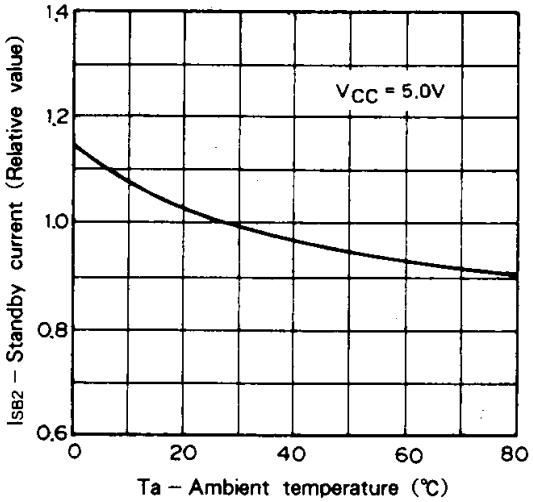

**Standby current vs. Ambient temperature**



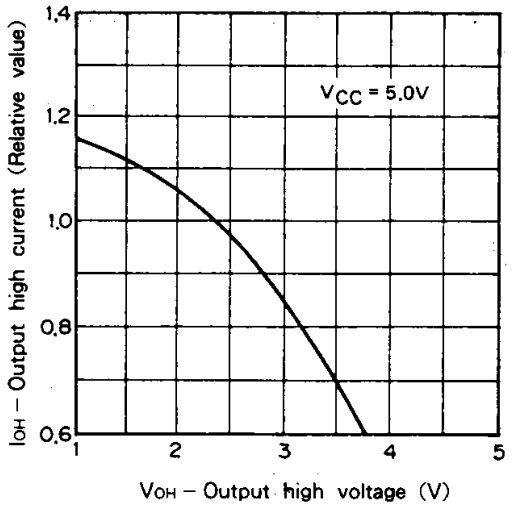

**Input voltage level vs. Supply voltage**



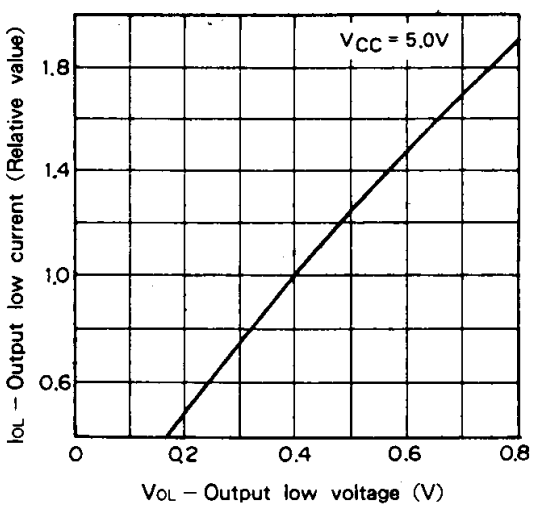

**Standby current vs. Ambient temperature**




**Output high current vs. Output high voltage**

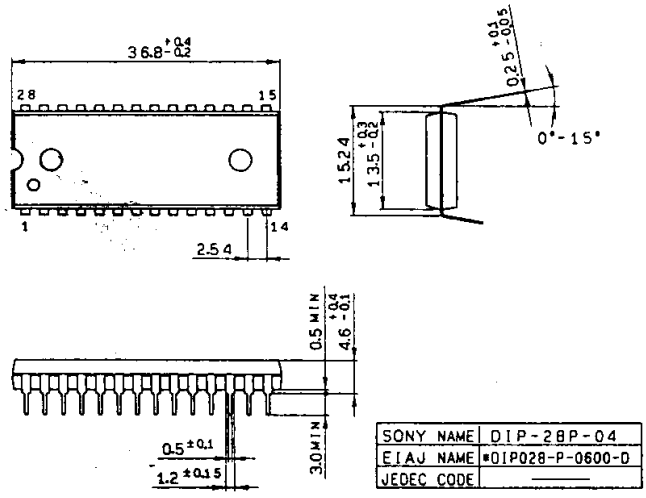



**Output low current vs. Output low voltage**



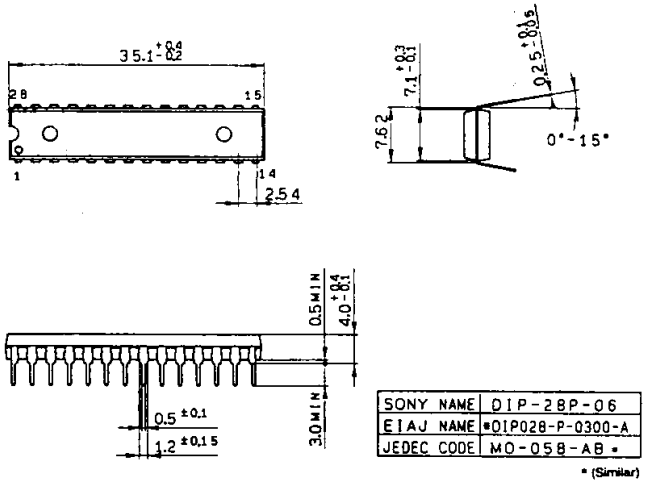
**Package Outline** Unit : mm

CXK5864BP 28 pin DIP (Plastic) 600mil 4.2g




| | |
|---|---|
| SONY NAME | DIP-28P-04 |
| EIAJ NAME | *DIP028-P-0600-D |
| JEDEC CODE | ——— |

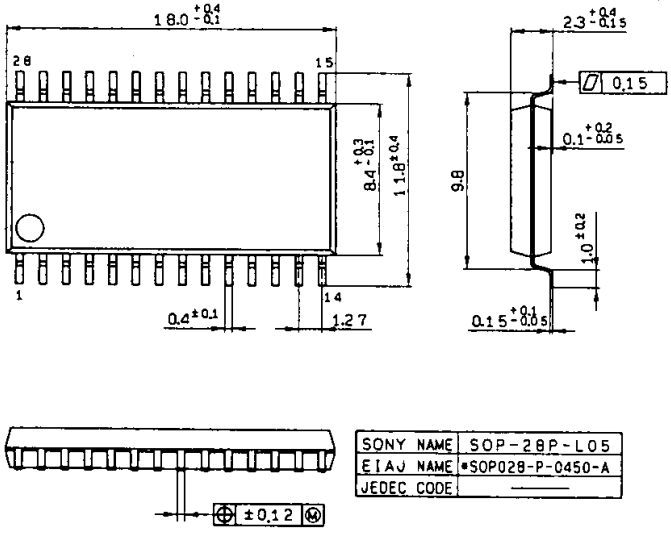
CXK5864BSP 28 pin DIP (Plastic) 300mil 2.0g




| | |
|---|---|
| SONY NAME | DIP-28P-06 |
| EIAJ NAME | *DIP028-P-0300-A |
| JEDEC CODE | MO-058-AB * |

* (Similar)

CXK5864BM 28 pin SOP (Plastic) 450mil 0.7g




| | |
|---|---|
| SONY NAME | SOP-28P-L05 |
| EIAJ NAME | *SOP028-P-0450-A |
| JEDEC CODE | ——— |