SAMSUNG ELECTRONICS

JAN. 1998

SPECIFICATION

for KS5514B-XX

SYSTEM LSI BUSINESS

SAMSUNG ELECTRONICS CO.

SAMSUNG ELECTRONICS

SPECIFICATION
for KS5514B-XX

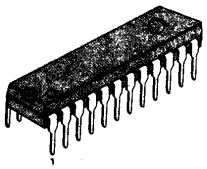
Important Notice

CONTENTS

ON SCREEN DISPLAY PROCESSOR

The KS5514B is a BICMOS LSI with on screen display function, sync. separator & expander function.

24 - SDIP - 300



FUNCTIONS

- On screen display
- Sync separator and sync detector
- General expander

FEATURES

- Character capacity : 240 (24 column × 10 row)
- Construction of character : 12 × 18 dots
- 128 kinds of character
- Display position : 62 horizontal position
  : 64 vertical position
- Character size : 4 × 4 times of normal
- Blinking : character unit
- Background coloring : 8 colors
- Synchronous ways : automatic selection internal or external synchronization via MICOM control
- General output : 3 ports (by serial data)
- Built-in sync separator & sync detector
- NTSC / PAL / SECAM mode
- Clamp circuit

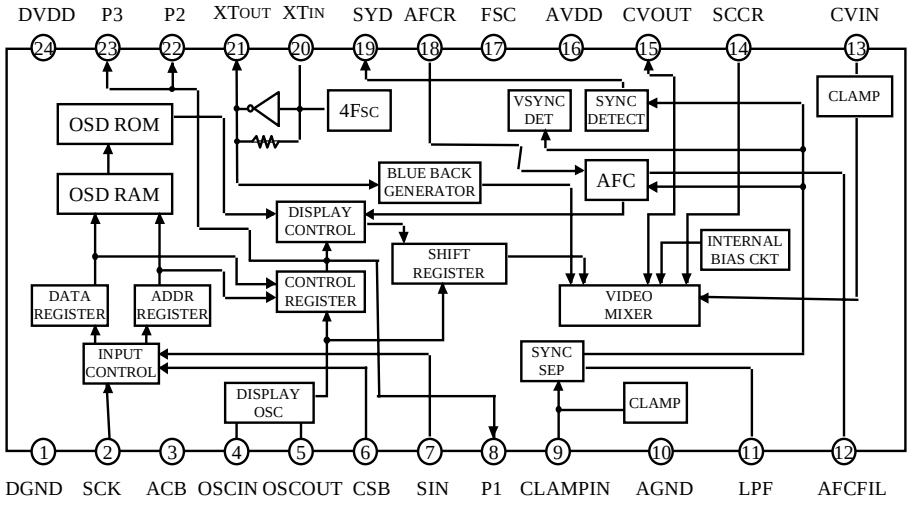
ORDERING INFORMATION

Device	Package	Operating Temprature
KS5514B-XX	24-SDIP-300	- 20 ~ + 70℃

OPTION CODE INFORMATION

Code No.	Remark
- 02	English
- 03	English, Russian
- 06	English
- 07	Korean
- 09	Korean, English
- 10	English, German
- 12	English, Arabic
- 13	English
- 14	Korean, English
- 15	English, Chinese
- 16	English, Russian, Arabic

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
1	DGND	-	Digital Ground
2	SCK	I	Serial clock input. When CSB pin is `L` then serial data is inputted by micom. Hysteresis input.
3	ACB	I	Auto clear pin. If `L`, then all circuit is reset. Built-in pull up resistor. Hysteresis input.
4	OSCIN	I	LC oscillation pin. Standard frequency is 7MHz & the horizontal start position is controlled by the clock of oscillation block.
5	OSCOUT	O	
6	CSB	I	While pin 6 is low, serial data input is active. Built - in pull up resistor
7	SIN	I	Serial data input pin. Built-in pull up resistor
8	P1	O	General output port 1
9	CLAMPIN	I	Clamp input pin of composite video signal
10	AGND	-	Analog ground
11	LPF	-	Low pass filter
12	AFCFIL	-	AFC filter output
13	CVIN	I	Composite video signal input
14	SCCR	I	SECAM chroma input
15	CVOUT	O	Composite video output : 2 Vp-p
16	AVDD	-	Analog VDD
17	FSC	I	FSC input (Not use)
18	AFCR	I	VCO oscillation frequency control
19	SYD	O	When sync signal is inputted, then SYD is high.

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Function
20	XTIN	I	X-TAL
21	XTOUT	O	X-TAL
22	P2	O	General output port 2
23	P3	O	General output port 3
24	DVDD	-	Digital VDD

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	- 0.3 ~ 6.0	V
Input Voltage	V_{IN}	V_{SS} - 0.3 ≤ V_{IN} ≤ V_{DD} + 0.3	V
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	- 20 ~ + 70	℃
Storage Temperature	Tstg	- 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, AV_{DD} = DV_{DD} = 5V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	DV_{DD}	3.5	5.0	5.5	V
Operating Voltage	AV_{DD}	4.5	5.0	5.5	V
Operating Current	Icc	10	20	25	mA
Pin 12 DC Voltage	Vpi2	2.3	2.5	2.7	V
Pin 13 DC Voltage	Vpi3	1.3	1.45	1.6	V
AFC Freerun Frequency	Ffr	15.5	15.7	15.9	KHz
AFC Pulse Width	twd	3.7	4.0	4.3	usec
AFC Delay Time	td	1.0	2.5	4.0	usec
AFC Lock Range H	Falh	+600	-	-	Hz
AFC Lock Rnage L	Fall	-	-	-900	Hz
AFC Capture Range H	Fach	+400	-	-	Hz
AFC Capture Rrange L	Fac1	-	-	-700	Hz
SYNC DET. Lock Range H	Flh	143	153	163	KHz
SYNC DET. Lock Range L	Fll	6.7	7.7	8.7	KHz
SYNC DET. Capture Range H	Fch	100	107	114	KHz
SYNC DET. Capture Range L	Fc1	14.3	15.3	16.3	KHz
V - SYNC Delay Time	tvd	10	14	-	usec
Oscillation Level	Vosc	4.0	4.5	5.0	Vpp
Oscillation Frequency	Fosc	6.3	7.0	7.7	MHz
Blueback Sync Tip Level	Vbst	1.85	2.05	2.25	V
Blueback Pedestal Level	Vbpd	2.5	2.7	2.9	V
Blueback Color Burst Level H	Vbbh	2.75	2.95	3.15	V
Blueback Color Level H	Vbch	3.1	3.3	3.5	V

OPERATION DESCRIPTION

MEMORY STRUCTURE

After KS5514B records, in DATA RAM and CONTROL REGISTER, the serial DATA that is inputted from MICOM, in recording to the V-SYNC and H-SYNC signal, mix the COMPOSITE VIDEO signal and the font ROM data that is mapped to data RAM.
In case that there is no composite video signal that is inputted to KS5514B, the SYNC detector becomes low, KS5514B makes the blue back signal in dividing the 4fsc signal and the blue back signal is outputted.
The following table is the data structure that is inputted from MICOM.

- Memory address consists of 16 bit
- The data of address 0 ~ 239 are character data which are display on the screen.
- The address 240 ~ 244 are the control registers.
- Don`t care bit : the upper 8 bits (DA8 ~ DAF) in address 0 ~ address 239, the upper 5bits (DAB ~ DAF) in address 240 ~ address 244

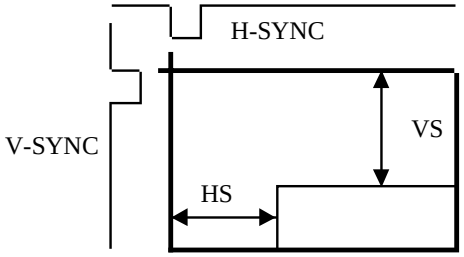
Bit / Addr	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	*	*	*	*	*	*	*	*	BLI	C6	C5	C4	C3	C2	C1	C0
												(Font ROM Address)				
.			.				.						.			
.			.				.						.			
.			.				.						.			
239	*	*	*	*	*	*	*	*	BLI	C6	C5	C4	C3	C2	C1	C0
240	*	*	*	*	*	INT/ NON	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0
241	*	*	*	*	*	BLI2	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0
242	*	*	*	*	*	DSP 3	DSP 2	DSP 1	RAM ERS	TEST	TC	LEV 1	LEV 0	PH2	PH1	PH0
243	*	*	*	*	*	-	LE BK	LE CHA	DSP ON	BLK 1	BLK 0	BLI 1	BLI 0	EX	YM	BCO
244	*	*	*	*	*	$\overline{\text{SECAM}}$	NT/ PAL	-	PD3	PD2	-	PD0	PC3	PC2	PC1	PC0

CONTROL REGISTER

1) Register 240

<table>
<tr><th rowspan="2">DA0 ~ DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>HP0</td><td>0
1</td><td rowspan="6">HS is horizontal display start position
$HS = Tc * \{ 4 * \sum_{n=0}^{5} (HPn * 2^{n}) + N \}$
Tc : osc. period (1 / 7MHz = 143 nsec)
<table><tr><th>HSZ11</th><th>HSZ10</th><th rowspan="2">N</th></tr><tr><th>HSZ21</th><th>HSZ20</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="6">Horizontal Start Position</td></tr>
<tr><td>1</td><td>HP1</td><td>0
1</td></tr>
<tr><td>2</td><td>HP2</td><td>0
1</td></tr>
<tr><td>3</td><td>HP3</td><td>0
1</td></tr>
<tr><td>4</td><td>HP4</td><td>0
1</td></tr>
<tr><td>5</td><td>HP5</td><td>0
1</td></tr>
<tr><td>6</td><td>HSZ10</td><td>0
1</td><td rowspan="2">1st line
<table><tr><th>HSZ11 \ HSZ10</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">1st line character size control to horizontal-direction</td></tr>
<tr><td>7</td><td>HSZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>HSZ20</td><td>0
1</td><td rowspan="2">2nd ~ 10 th line
<table><tr><th>HSZ21 \ HSZ20</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">2nd ~ 10th line character size control to horizontal-direction</td></tr>
<tr><td>9</td><td>HSZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>INT/ NON</td><td>0</td><td>Interlace Mode</td><td>—</td></tr>
<tr><td></td><td></td><td>1</td><td>Non-interlace Mode</td><td></td></tr>
</table>

2) Register 241

<table>
<tr><th rowspan="2">DA0 ~ DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>VP0</td><td>0
1</td><td rowspan="6">VS is vertical start position
$VS = H * \{ 4 * \sum_{n=o}^{5} (VPn * 2^{n}) + 3 \}$
H : horizontal synchronous pulse time
 
</td><td rowspan="6">Vertical Start Position</td></tr>
<tr><td>1</td><td>VP1</td><td>0
1</td></tr>
<tr><td>2</td><td>VP2</td><td>0
1</td></tr>
<tr><td>3</td><td>VP3</td><td>0
1</td></tr>
<tr><td>4</td><td>VP4</td><td>0
1</td></tr>
<tr><td>5</td><td>VP5</td><td>0
1</td></tr>
<tr><td>6</td><td>VSZ10</td><td>0
1</td><td rowspan="2"><table><tr><th>VSZ11 \ VSZ10</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">1st line character size control to vertical direction</td></tr>
<tr><td>7</td><td>VSZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>VSZ20</td><td>0
1</td><td rowspan="2"><table><tr><th>VSZ21 \ VSZ20</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">2nd ~ 10th line character size control to vertical direction</td></tr>
<tr><td>9</td><td>VSZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>BLI2</td><td>0</td><td>V - SYNC 64 divide (= 1 sec)</td><td rowspan="2">Control the blink period</td></tr>
<tr><td></td><td></td><td>1</td><td>V - SYNC 32 divide (= 0.5 sec)</td></tr>
</table>

3) Register 242

<table>
<tr><th>DA0 ~ DAA</th><th>Register</th><th colspan="2">Content</th><th>Remark</th></tr>
<tr><th></th><th></th><th>State</th><th>Function</th><th></th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">PH0</td><td>0</td><td rowspan="8"><table>
<tr><th>P2 P1 P0</th><th>NTSC</th><th>PAL</th></tr>
<tr><td>0 0 0</td><td>π/4</td><td>π/4</td></tr>
<tr><td>0 0 1</td><td>π/2</td><td>π/2</td></tr>
<tr><td>0 1 0</td><td>7π/4</td><td>-π/4</td></tr>
<tr><td>0 1 1</td><td>0</td><td>0</td></tr>
<tr><td>1 0 0</td><td>π</td><td>±π</td></tr>
<tr><td>1 0 1</td><td>3π/4</td><td>3π/4</td></tr>
<tr><td>1 1 0</td><td>3π/2</td><td>3π/2</td></tr>
<tr><td>1 1 1</td><td>5π/4</td><td>5 π/4</td></tr>
</table></td><td rowspan="2">Back ground color control bit</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">PH1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">PH2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">LEVEL0</td><td>0</td><td rowspan="4"><table>
<tr><th>level 0 / level 1</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>Internal bias 1</td><td>Internal bias 2</td></tr>
<tr><td>1</td><td>-</td><td>Internal bias 3</td></tr>
</table></td><td rowspan="4">Color level control</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">LEVEL1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">TC</td><td>0</td><td>1H = 454Tc Tc = 2 / fosc</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>1H = 455Tc</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">TEST</td><td>0</td><td>Active mode</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Test mode</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">RAM ERS</td><td>0</td><td>RAM no erase</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>RAM erase</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">DSP1</td><td>0</td><td>Display method of the 1st is fixed by BLK0 & BLK1</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display method of the 1st is variable</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">DSP2</td><td>0</td><td>Display method of 2nd - 9th is fixed by BLK0 & BLK1</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display method of 2nd - 9th is variable</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">DSP3</td><td>0</td><td>Display method of 10th is fixed by BLK0 & BLK1</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display method of 10th is variable</td></tr>
</table>

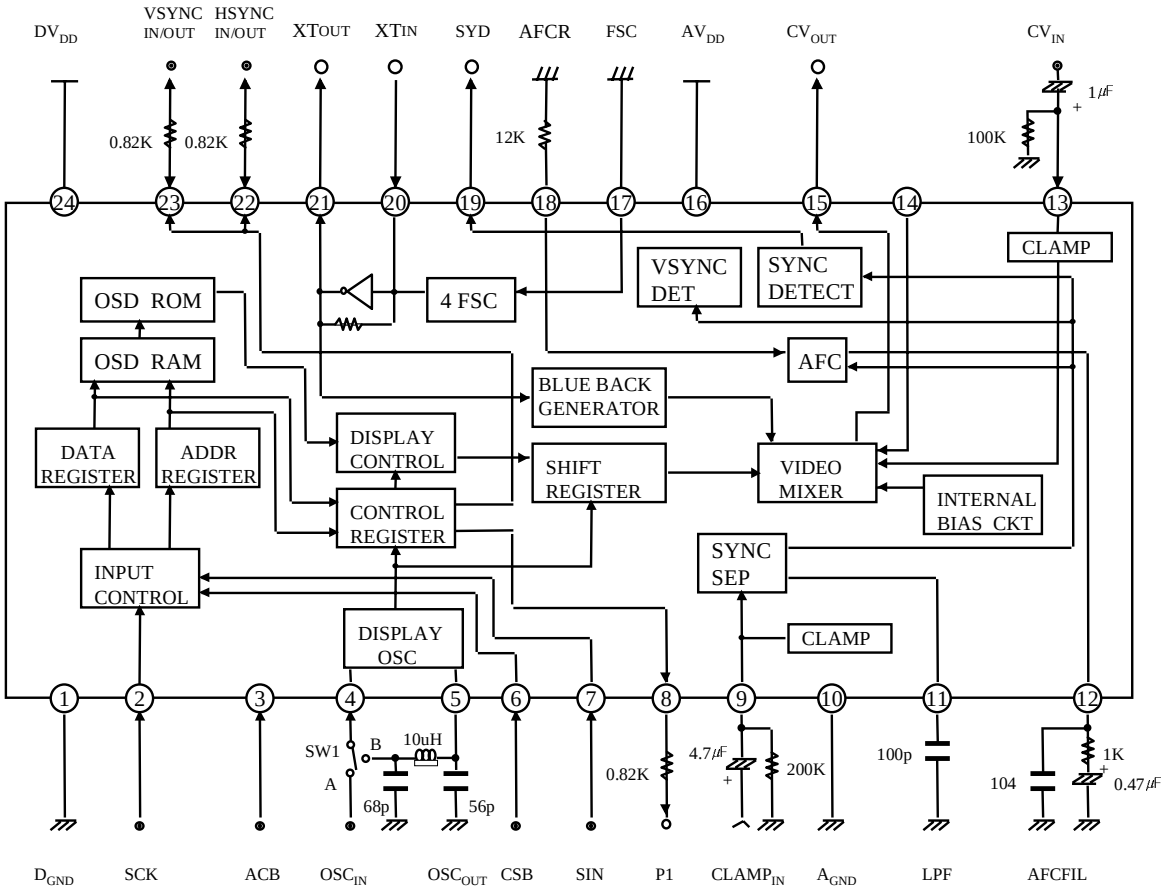
4) Register 243

<table>
<tr><th rowspan="2">DA0 ~ DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCO</td><td>0</td><td>Blanking area coloring</td><td rowspan="2">Determined by BLK0 & BLK1</td></tr>
<tr><td>1</td><td>Full TV screen coloring</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">YM</td><td>0</td><td>The same luminance level character and back ground</td><td rowspan="2">Determined by BCO, BLK0 & BLK1</td></tr>
<tr><td>1</td><td>Variable background luminance level available</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EX</td><td>0</td><td>External mode available</td><td rowspan="2">–</td></tr>
<tr><td>1</td><td>Internal mode available</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">BLI0</td><td>0</td><td rowspan="4">Blinking mode control
<table>
<tr><th>BLI1 \ BLI0</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>OFF</td><td>DUTY 25%</td></tr>
<tr><td>1</td><td>DUTY 50%</td><td>DUTY 75%</td></tr>
</table></td><td rowspan="4">Blinking duty control</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BLI1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLK0</td><td>0</td><td rowspan="4">Blanking mode control
<table>
<tr><th>BLK1 \ BLK0</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>OFF</td><td>C</td></tr>
<tr><td>1</td><td>O</td><td>R</td></tr>
</table></td><td rowspan="4">C : character
O : outline
R : raster</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BLK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">DSP ON</td><td>0</td><td>Display off</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display on</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">LECHA</td><td>0</td><td>Character luminance level 1</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Character luminance level 2</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">LEBLK</td><td>0</td><td>Blank luminance level 1</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Blank luminance level 2</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">-</td><td>0</td><td>-</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>-</td></tr>
</table>

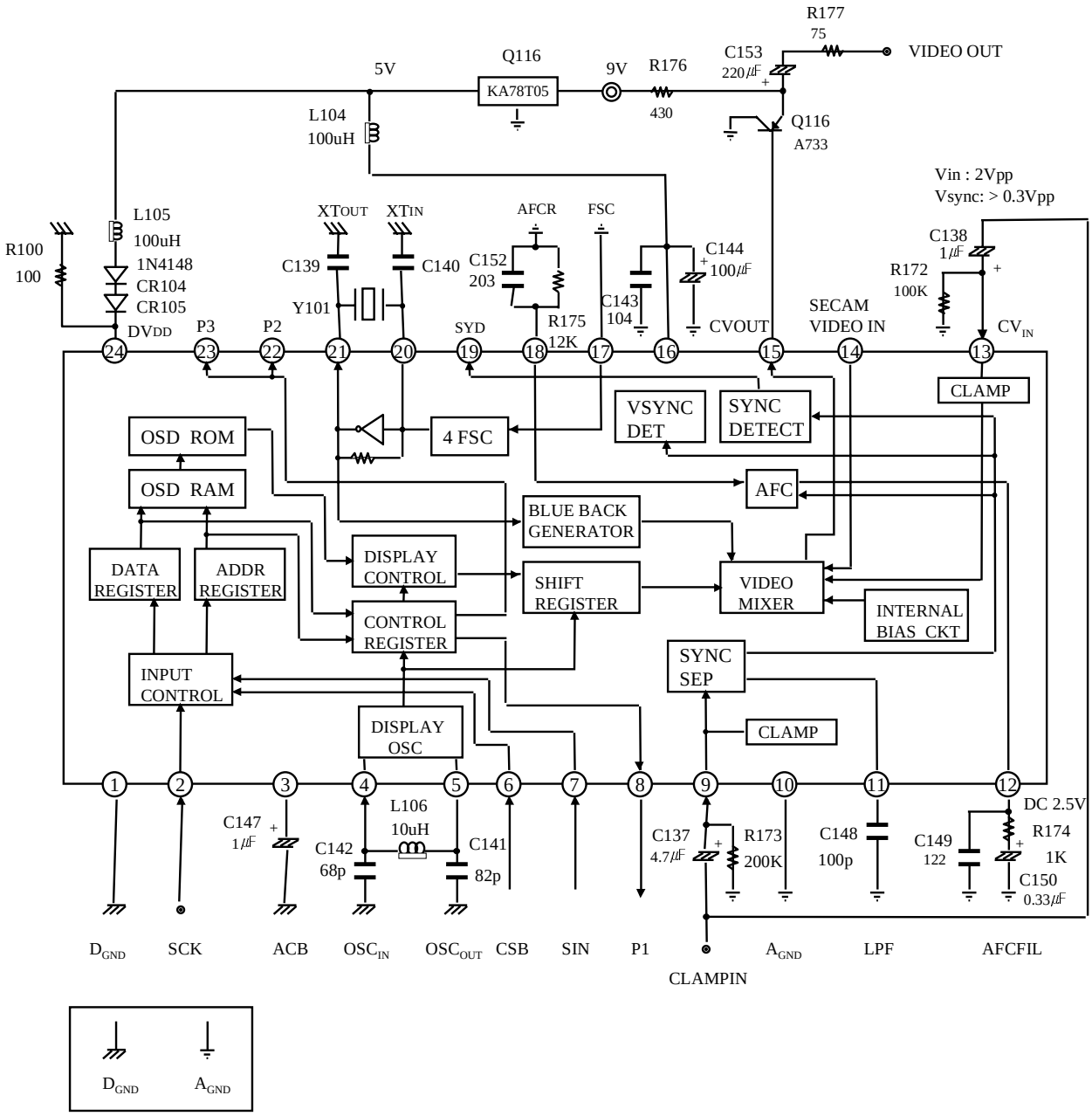
5) Register 244

<table>
<tr><th rowspan="2">DA0 ~ DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>PC0</td><td>0
1</td><td rowspan="3"><table><tr><th>PC1 \ PC0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Hsync+Vsync output</td><td>-</td></tr><tr><td>1</td><td>Port(PD0) output</td><td>Character1 output</td></tr></table></td><td rowspan="3">Pin 8 output mode setting</td></tr>
<tr><td>1</td><td>PC1</td><td>0
1</td></tr>
<tr><td>2</td><td>PC2</td><td>0
1</td><td rowspan="3"><table><tr><th>PC3 \ PC2</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Hsync(pin22) & Vsync(pin23) output</td><td>Test mode</td></tr><tr><td>1</td><td>Port(PD2/PD3) output</td><td>Character2, BLK2 output</td></tr></table></td><td rowspan="3">Pin 22/23 output mode setting</td></tr>
<tr><td>3</td><td>PC3</td><td>0
1</td></tr>
<tr><td>4</td><td>PD0</td><td>0
1</td><td>L output
H output</td><td>Pin 8 output data setting</td></tr>
<tr><td>5</td><td>-</td><td>0
1</td><td>-
-</td><td>–</td></tr>
<tr><td>6</td><td>PD2</td><td>0
1</td><td>L output
H output</td><td>Pin 22 output data setting</td></tr>
<tr><td>7</td><td>PD3</td><td>0
1</td><td>L output
H output</td><td>Pin 23 output data setting</td></tr>
<tr><td>8</td><td>-</td><td>0
1</td><td>-
-</td><td></td></tr>
<tr><td>9</td><td>NT/ PAL</td><td>0
1</td><td>NTSC mode
PAL mode</td><td></td></tr>
<tr><td>A</td><td>$\overline{\text{SECAM}}$</td><td>0
1</td><td>NTSC or PAL mode
SECAM mode</td><td></td></tr>
</table>

TEST CIRCUIT



APPLICATION CIRCUIT (APP-082)



The circuit drawn above is for Demo Board.

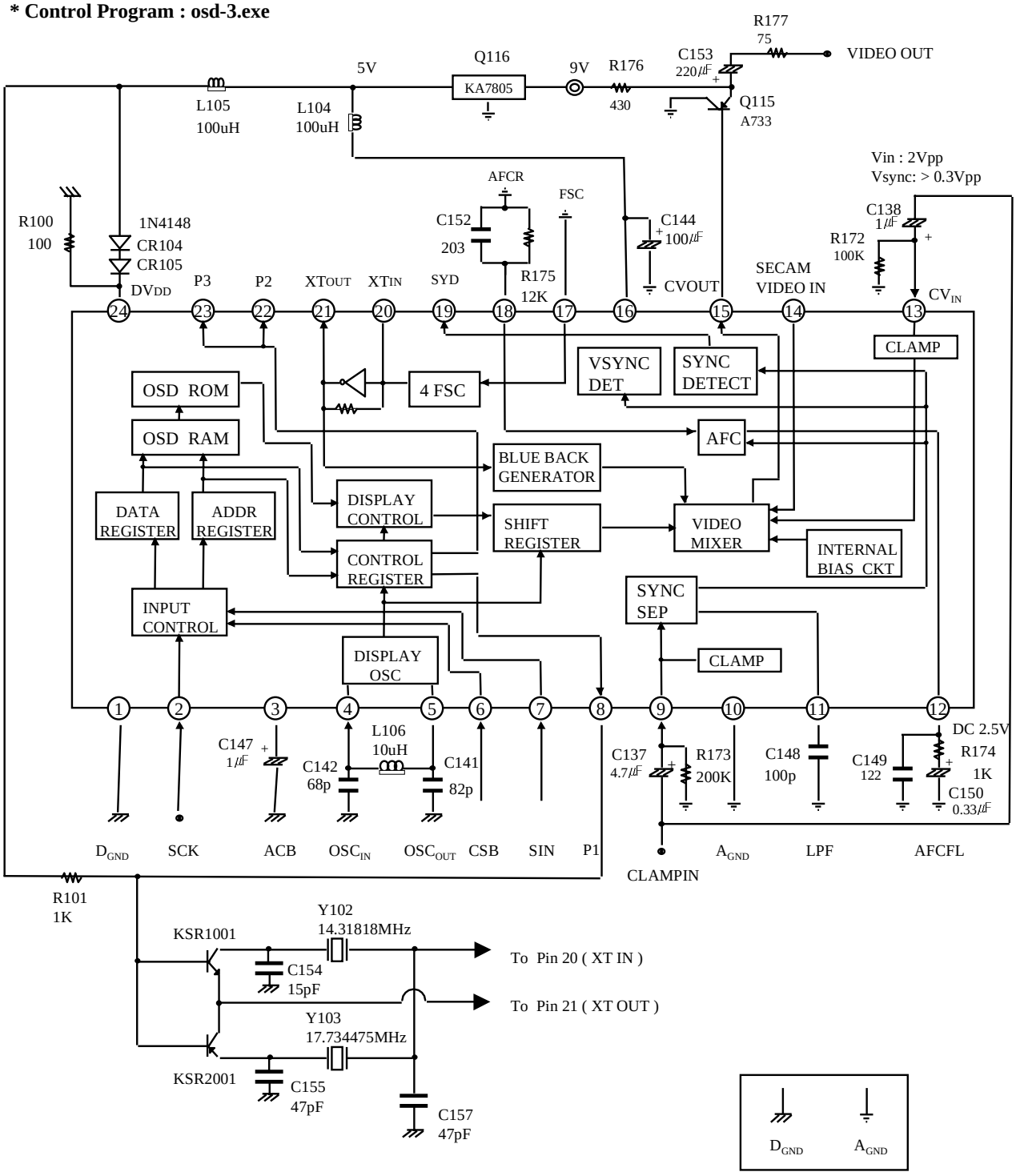
• Y101 (4fsc X-TAL) → NTSC : 14.31818MHz

PAL : 17.734475MHz

• C139 / C140 : The load CAP of X-TAL Y101 has a difference each according to its manufacturer.

APPLICATION CIRCUIT (APP-306)

*** Control Program : osd-3.exe**



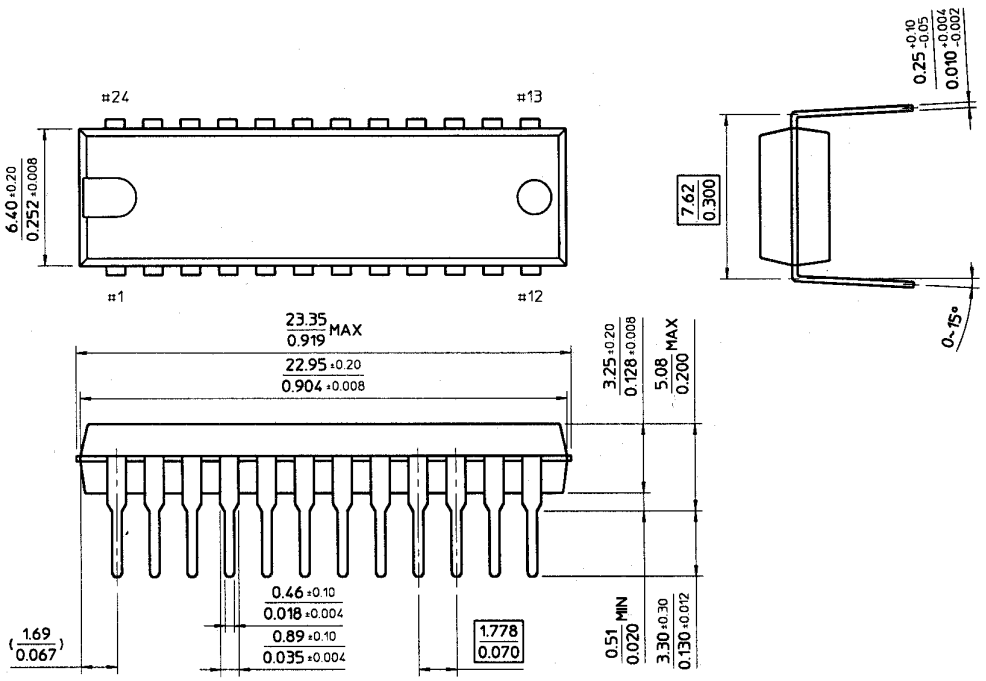
The circuit drawn above is for Demo Board.

• Y102 (4fsc X-TAL) → NTSC : 14.31818MHz

Y103 (4fsc X-TAL) → PAL : 17.734475MHz

PACKAGE DIMENSIONS

24-SDIP-300 Dimensions in Milimeters/Inches



MEMO

SAMSUNG ELECTRONICS CO., LTD.
SEMICONDUCTOR BUSINESS BEIJING OFFICE
15FL., BRIGHT CHINA CHANG AN BLDG.,
NO.7, JIANGUOMEN, NEI AVENUE,
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