

**DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET**

**DESCRIPTION**

The M74LS73AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input  $\bar{T}$ , inputs J and K and direct reset input  $\bar{R}_D$ .

**FEATURES**

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct reset input
- Q and  $\bar{Q}$  outputs
- Wide operating temperature range ( $T_a = -20 \sim +75^\circ\text{C}$ )

**APPLICATION**

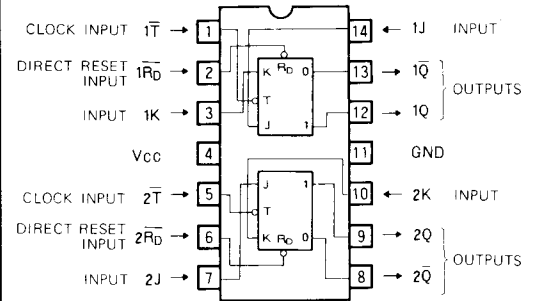
General purpose, for use in industrial and consumer equipment.

**FUNCTIONAL DESCRIPTION**

While  $\bar{T}$  is high, signals J and K are put in the read-in state, and when  $\bar{T}$  changes from high to low, the J and K signals immediately before the change emerge in outputs Q and  $\bar{Q}$  in accordance with the function table. By setting  $\bar{R}_D$  low, Q and  $\bar{Q}$  are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop,  $\bar{R}_D$  must be kept high.

Also available is M74LS107AP with the same functions and electrical characteristics. This offers easy mounting with  $V_{CC}$  positioned at pin 14 and GND at pin 7.

**PIN CONFIGURATION (TOP VIEW)**



Outline 14P4

**FUNCTIONAL TABLE** (Note 1)

$\bar{T}$	$\bar{R}_D$	J	K	Q	$\bar{Q}$
X	L	X	X	L	H
↓	H	H	H	Toggle	
↓	H	L	H	L	H
↓	H	H	L	H	L
↓	H	L	L	$Q^0$	$\bar{Q}^0$
H	H	X	X	$Q^0$	$\bar{Q}^0$

Note 1 ↓ : Transition from high to low-level (negative edge trigger)

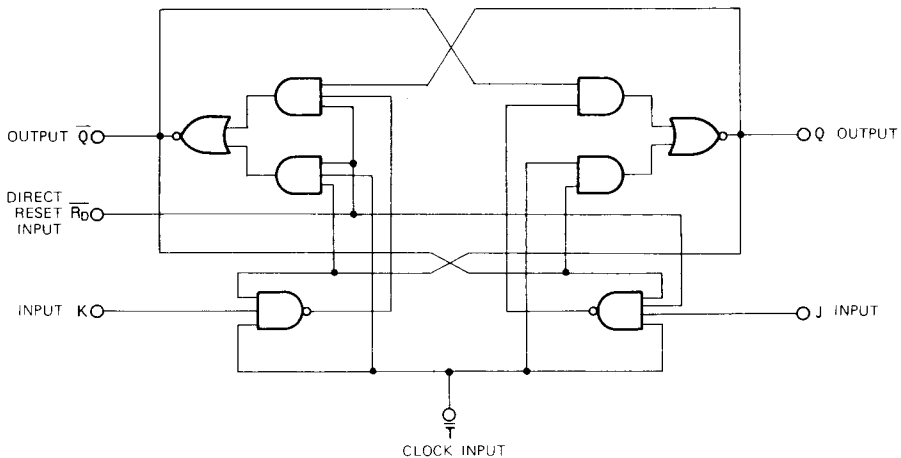
X : Irrelevant

$Q^0$  : level of Q before the indicated steady-state input conditions were established.

$\bar{Q}^0$  : level of  $\bar{Q}$  before the indicated steady-state input conditions were established.

Toggle : complement of previous state with ↓ transition of outputs

**BLOCK DIAGRAM (EACH FLIP-FLOP)**



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**ABSOLUTE MAXIMUM RATINGS** (  $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted )

Symbol	Parameter	Conditions	Limits	Unit
$V_{CC}$	Supply voltage		$-0.5 \sim +7$	V
$V_I$	Input voltage		$-0.5 \sim +15$	V
$V_O$	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
$T_{opr}$	Operating free-air ambient temperature range		$-20 \sim +75$	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$-65 \sim +150$	$^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS** (  $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted )

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.75	5	5.25	V
$I_{OH}$	High-level output current	$V_{OH} \geq 2.7\text{V}$	0		-400	$\mu\text{A}$
$I_{OL}$	Low-level output current	$V_{OL} \leq 0.4\text{V}$	0		4	mA
		$V_{OL} \leq 0.5\text{V}$	0		8	mA

**ELECTRICAL CHARACTERISTICS** (  $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted )

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ *	Max	
$V_{IH}$	High-level input voltage			2			V
$V_{IL}$	Low-level input voltage					0.8	V
$V_{IC}$	Input clamp voltage		$V_{CC} = 4.75\text{V}$ , $I_{IC} = -18\text{mA}$			-1.5	V
$V_{OH}$	High-level output voltage		$V_{CC} = 4.75\text{V}$ , $V_I = 0.8\text{V}$ $V_I = 2\text{V}$ , $I_{OH} = -400\mu\text{A}$	2.7	3.4		V
$V_{OL}$	Low-level output voltage		$V_{CC} = 4.75\text{V}$		0.25	0.4	V
			$V_I = 0.8\text{V}$ , $V_I = 2\text{V}$		0.35	0.5	V
$I_{IH}$	High-level input current	J, K	$V_{CC} = 5.25\text{V}$ $V_I = 2.7\text{V}$			20	$\mu\text{A}$
		$\overline{R_D}$				60	$\mu\text{A}$
		$\overline{T}$				80	$\mu\text{A}$
		J, K	$V_{CC} = 5.25\text{V}$ $V_I = 10\text{V}$			0.1	mA
		$\overline{R_D}$				0.3	mA
		$\overline{T}$				0.4	mA
$I_{IL}$	Low-level input current	J, K	$V_{CC} = 5.25\text{V}$			-0.4	mA
		$\overline{R_D}$ , $\overline{T}$	$V_I = 0.4\text{V}$			-0.8	mA
$I_{OS}$	Short-circuit output current (Note 2)		$V_{CC} = 5.25\text{V}$ , $V_O = 0\text{V}$	-20		-100	mA
$I_{CC}$	Supply current		$V_{CC} = 5.25\text{V}$ (Note 3)		4	6	mA

\* : All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

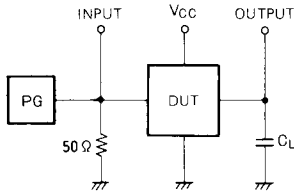
Note 3: Supply current measurements should be done with Q and  $\overline{Q}$  set alternately high and  $\overline{T}$  should be set low during actual measurement.

**SWITCHING CHARACTERISTICS** (  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , unless otherwise noted )

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$f_{max}$	Maximum clock frequency		$C_L = 15\text{pF}$ (Note 4)	30	45		MHz
$t_{PLH}$	Low-to-high-level, high-to-low-level output propagation time, from $\overline{T}$ to Q, $\overline{Q}$				8	20	ns
$t_{PHL}$	High-to-low-level, high-to-low-level output propagation time, from $\overline{T}$ to Q, $\overline{Q}$				6	20	ns
$t_{PLH}$	Low-to-high-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, $\overline{Q}$				10	20	ns
$t_{PHL}$	High-to-low-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, $\overline{Q}$				7	20	ns

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Note 4: Measurement circuit

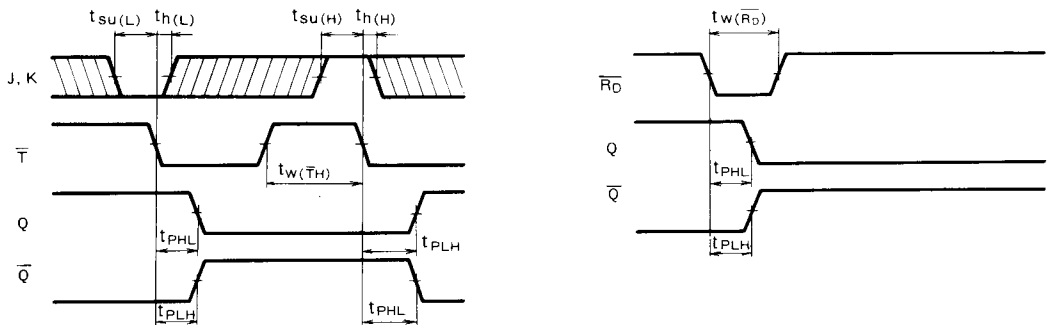


- (1) The pulse generator (PG) has the following characteristics:  
 $PRR = 1\text{MHz}$ ,  $t_r = 6\text{ns}$ ,  $t_f = 6\text{ns}$ ,  $t_w = 500\text{ns}$ ,  
 $V_p = 3V_{p.p.}$ ,  $Z_o = 50\Omega$
- (2)  $C_L$  includes probe and jig capacitance.

TIMING REQUIREMENTS ( $V_{CC} = 5V$ ,  $T_a = 25^\circ C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(\bar{T}H)$	Clock input $\bar{T}$ high pulse width		20	12		ns
$t_w(\bar{R}D)$	Direct reset input pulse width		25	4		ns
$t_r$	Clock rise time			650	100	ns
$t_f$	Clock fall time			900	100	ns
$t_{su}(H)$	Setup time high $\bar{T}$ to J, K		20	9		ns
$t_{su}(L)$	Setup time low $\bar{T}$ to J, K		20	10		ns
$t_h(H)$	Hold time high $\bar{T}$ to J, K		0	- 8		ns
$t_h(L)$	Hold time low $\bar{T}$ to J, K		0	- 5		ns

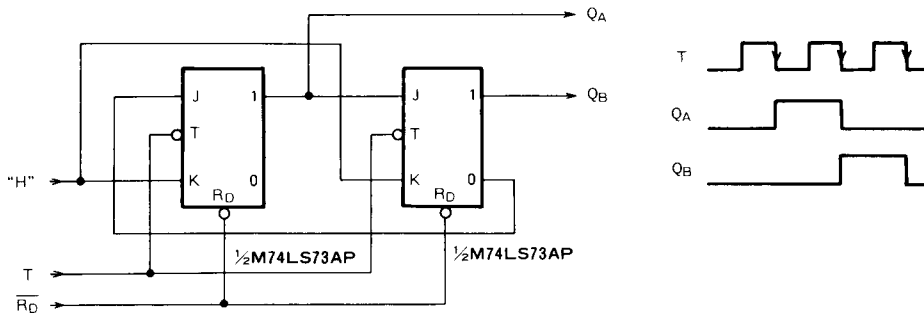
TIMING DIAGRAM (Reference level = 1.3V)



Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

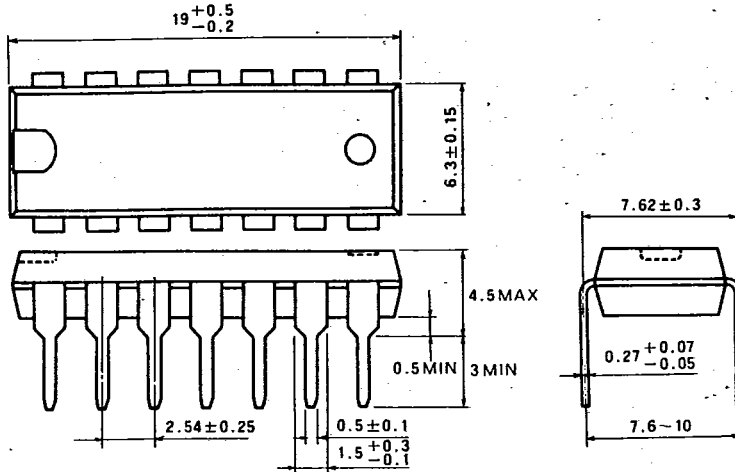
High-speed 1/3 divider



T-90-20

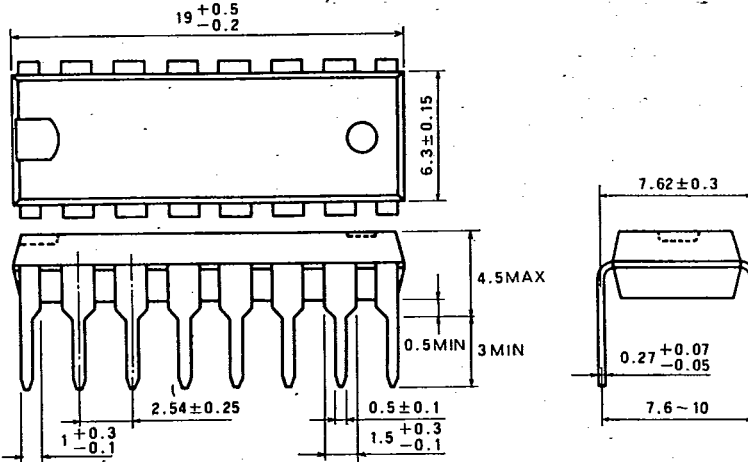
**TYPE 14P4 14-PIN MOLDED PLASTIC DIL**

Dimension in mm



**TYPE 16P4 16-PIN MOLDED PLASTIC DIL**

Dimension in mm



**TYPE 20P4 20-PIN MOLDED PLASTIC DIL**

Dimension in mm

