Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUFFERS

IDT54/74FCT827A
IDT54/74FCT827B
IDT54/74FCT827C

FEATURES:

- Faster than AMD's Am29827 series
- Equivalent to AMD's Am29827 bipolar buffers in pinout/ function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT827A equivalent to FAST™
- **IDT54/74FCT827B 35% faster than FAST**
- **IDT54/74FCT827C 45% faster than FAST**
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

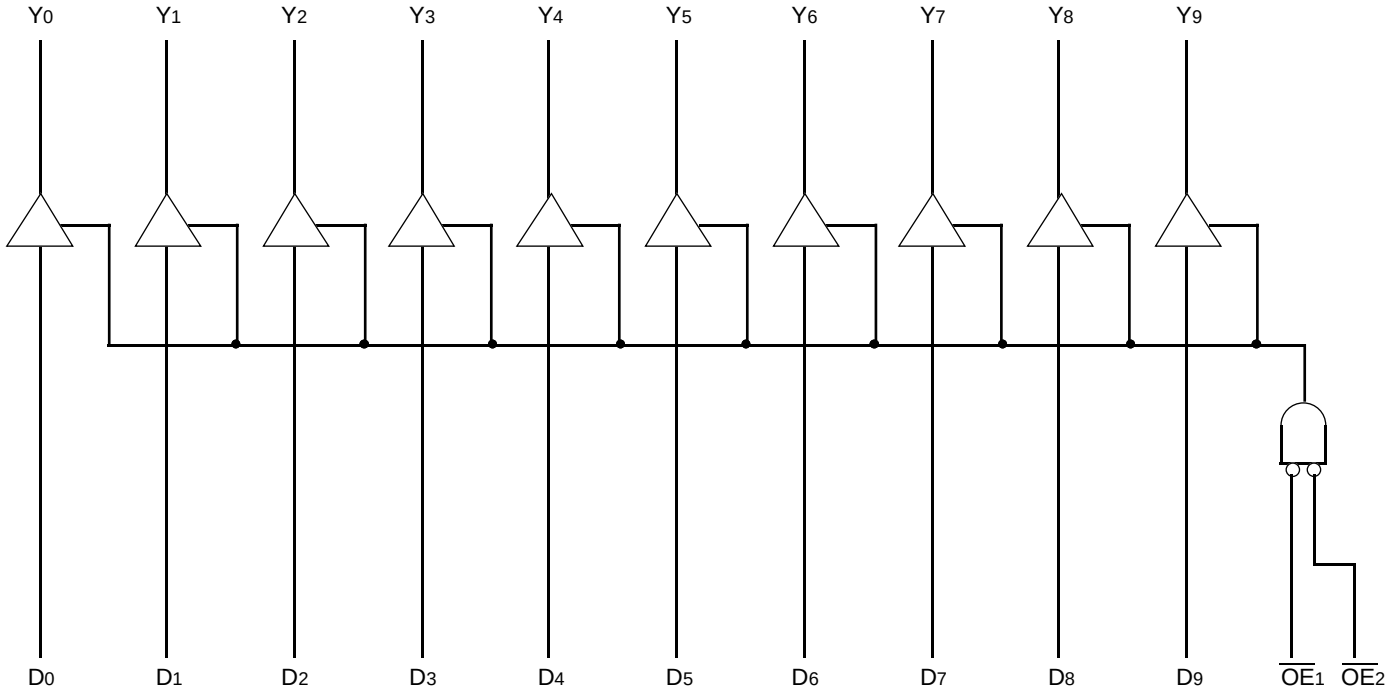
DESCRIPTION:

The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT827A/B/C 10-bit bus drivers provide high-performance bus interface buffering for wide data/ address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

	10-Bit Buffer
Non-inverting	IDT54/74FCT827A/B/C

2609 tbl 01

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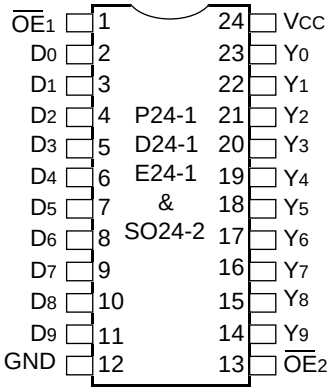
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



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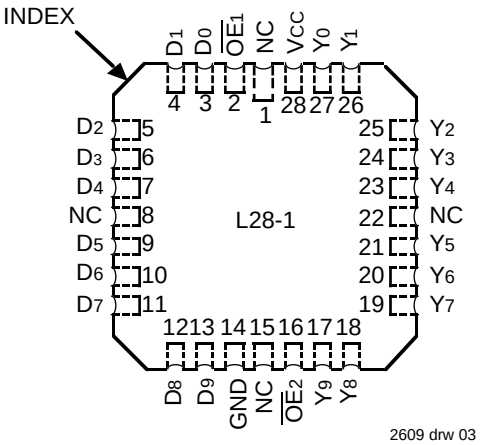
DIP/CERPACK/SOIC
TOP VIEW



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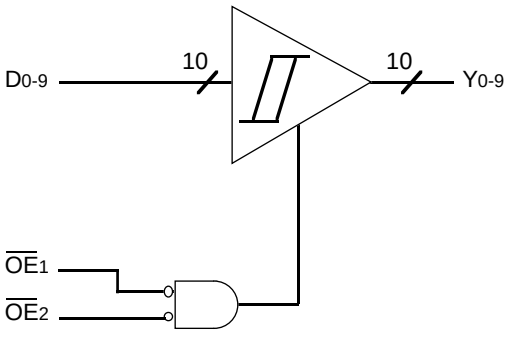
LCC
TOP VIEW

LOGIC SYMBOL



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PIN DESCRIPTION

Name	I/O	Description
$\overline{OE}_I$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

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FUNCTION TABLE(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE: 2609 tbl 03

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2609 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2609 tbl 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2609 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		50% Duty Cycle $\overline{OE}_1$ = $\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		50% Duty Cycle $\overline{OE}_1$ = $\overline{OE}_2$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

NOTES: 2609 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Conditions[1]	IDT54/74FCT827A				IDT54/74FCT827B				IDT54/74FCT827C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_I to Y_I	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	1.5	4.4	1.5	5.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_I$ to Y_I	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	1.5	14.0	1.5	15.0	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_I$ to Y_I	C_L = 5pF[3] R_L = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	1.5	5.7	1.5	6.7	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.0	1.5	7.0	

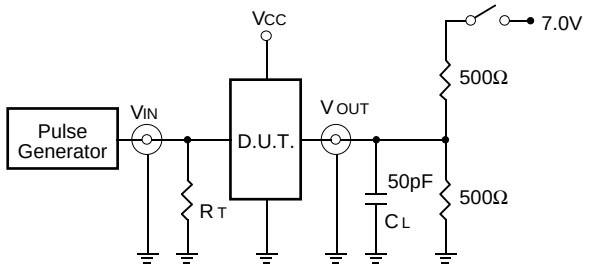
NOTES:

2609 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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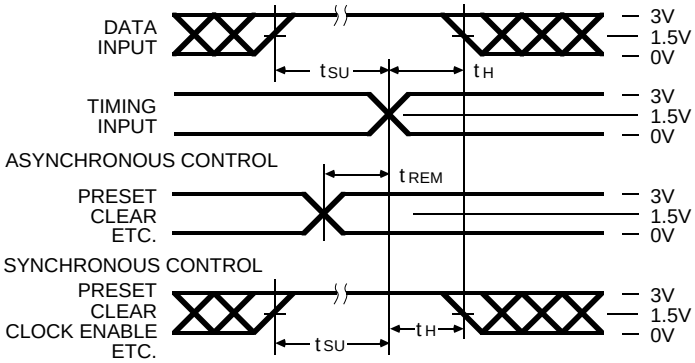
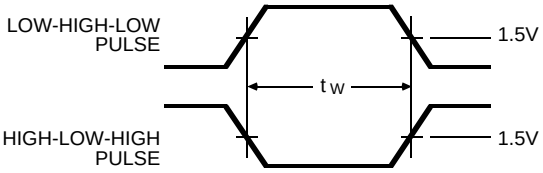
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

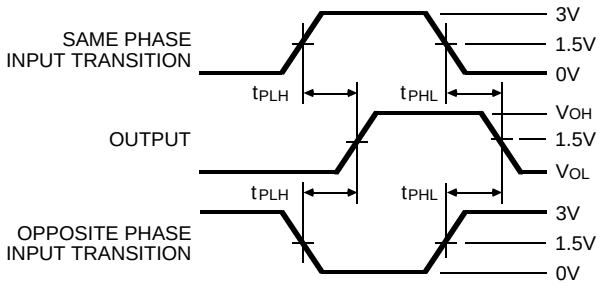
SET-UP, HOLD AND RELEASE TIMES



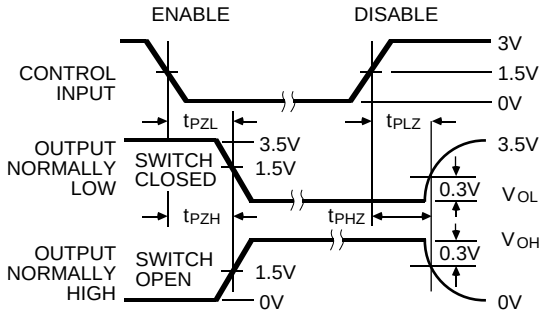
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



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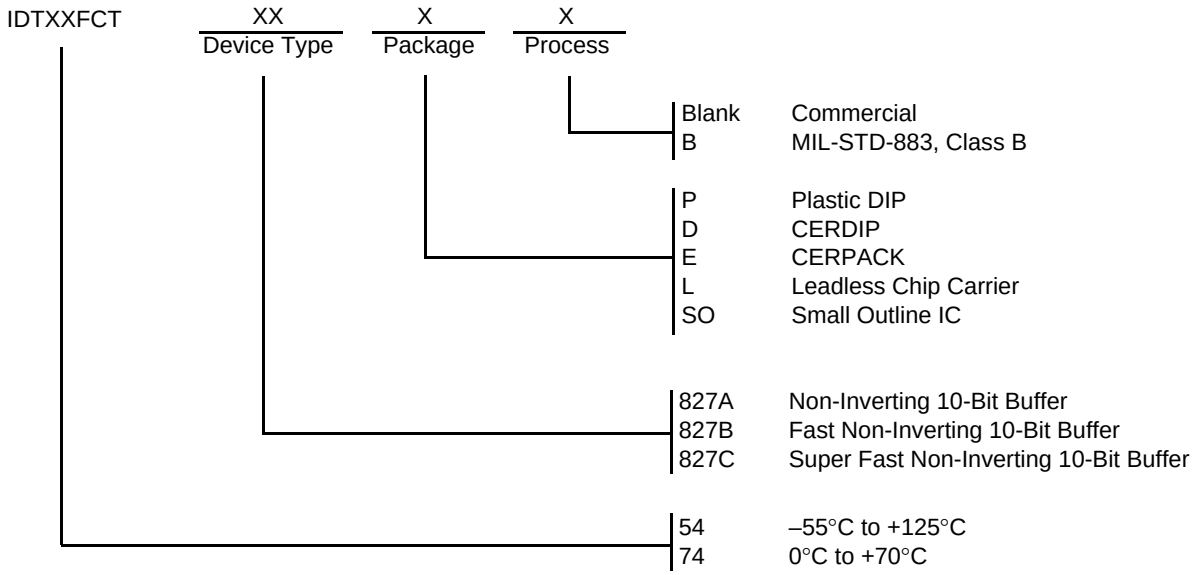
NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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