

## SPI CONTROLLED H-BRIDGE

PRELIMINARY DATA

### 1 Features

- OPERATING SUPPLY VOLTAGE 5V TO 28V
- TYPICAL  $R_{DSon} = 150\text{ m}\Omega$  FOR EACH OUTPUT TRANSISTOR (AT 25°C)
- CONTINUOUS DC LOAD CURRENT 5A ( $T_{case} < 100\text{ }^\circ\text{C}$ )
- OUTPUT CURRENT LIMITATION AT TYP. 8.6A
- SHORT CIRCUIT SHUT DOWN FOR OUTPUT CURRENTS OVER TYP. 10.6A
- LOGIC- INPUTS TTL/CMOS-COMPATIBLE
- OPERATING-FREQUENCY UP TO 30 kHz
- OVER TEMPERATURE PROTECTION
- SHORT CIRCUIT PROTECTION
- UNDERVOLTAGE DISABLE FUNCTION
- DIAGNOSTIC BY SPI OR STATUS-FLAG (CONFIGURABLE)
- ENABLE AND DISABLE INPUT
- SO20 POWER PACKAGE

### 2 Description

The L9929 is an SPI controlled H-Bridge, designed for the control of DC and stepper motors in safety critical applications and under extreme environmental conditions.

Figure 1. Package

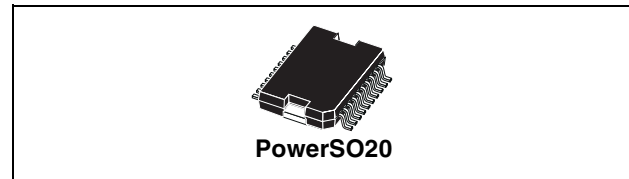


Table 1. Order Codes

Part Number	Package
L9929	PowerSO20

The H-Bridge is protected against over temperature and short circuits and has an under voltage lockout for all the supply voltages "V<sub>s</sub>" (Main DC power supply). All malfunctions cause the output stages to go tristate.

The H-Bridge contains integrated free-wheel diodes. In case of free-wheeling condition, the low side transistor is switched on in parallel of its diode to reduce the current injected into the substrate. Switching in parallel is only allowed, if the voltage level of the according output-stage is below the ground-level. In this case it must be ensured, that the upper transistor is switched off.

Figure 2. Block Diagram

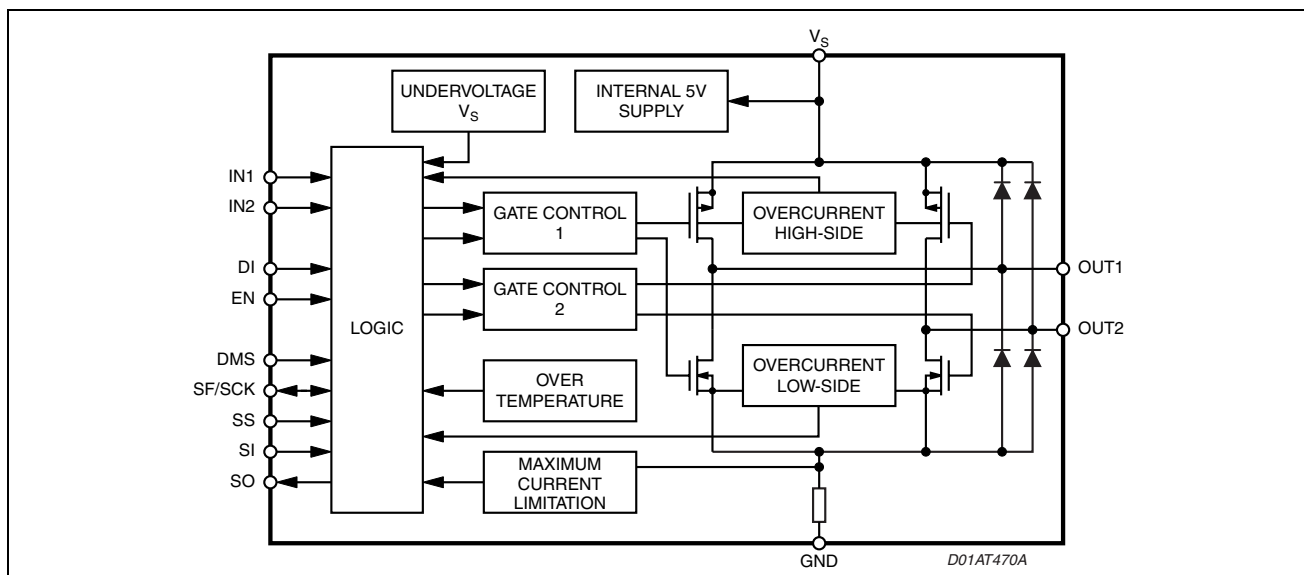
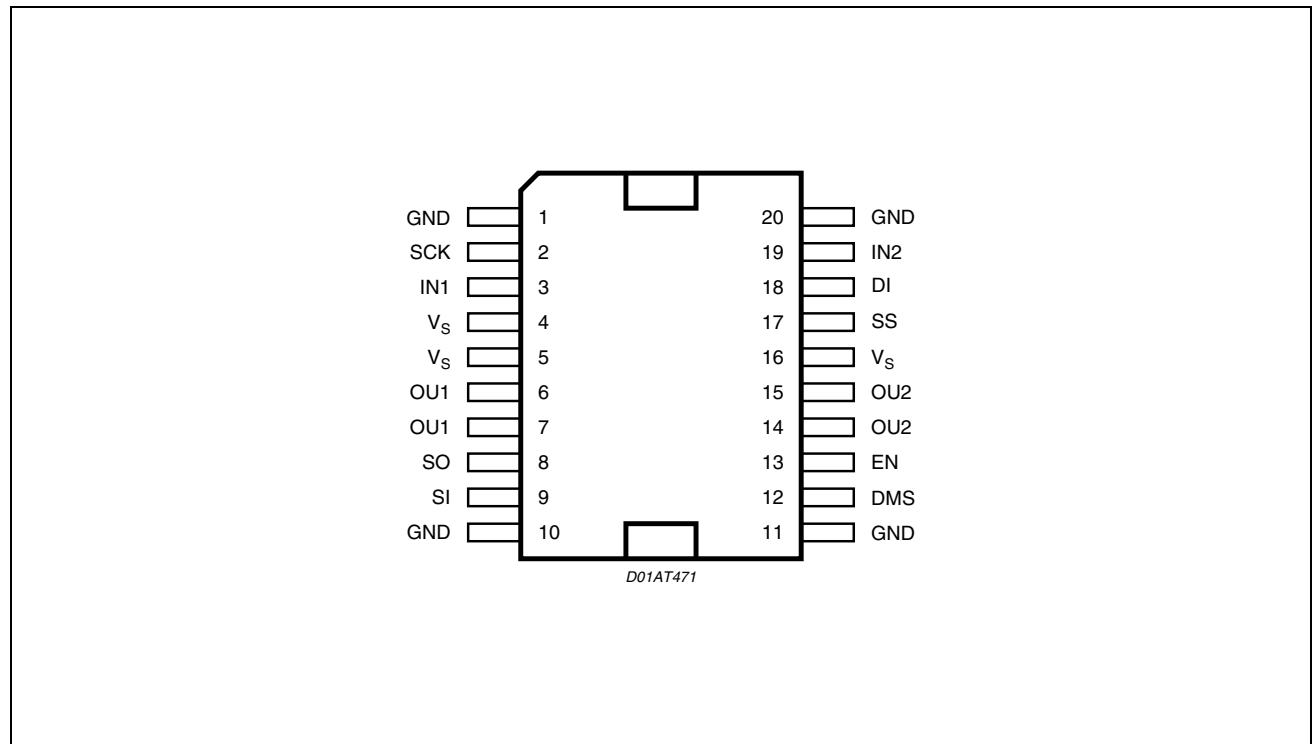


Table 2. Pin Function

N°	Pin	Description
1	GND	Ground
2	SCK/SF	SPI-Clock/Status-flag
3	IN1	Input 1
4	V <sub>S</sub>	Supply voltage
5	V <sub>S</sub>	Supply voltage
6	OU1	Output 1
7	OU1	Output 1
8	SO	serial out
9	SI	serial in
10	GND	Ground
11	GND	Ground
12	DMS	Diagnostic-Mode selection (+ Supply Voltage for SPI-Interface)
13	EN	Enable
14	OU2	Output 2
15	OU2	Output 2
16	V <sub>S</sub>	Supply voltage
17	SS	Slave select
18	DI	Disable
19	IN2	Input 2
20	GND	Ground

Figure 3. Pin Connection (Top view)



**Table 3. Absolute Maximum Ratings**

The integrated circuit must not be destroyed by use at the limit values.

Each limit value can be used, as long as no other limit is violated.

Voltage reference point: All values are, if not otherwise stated, relative to ground.

Direction of current flow: Current flow into a pin is positive.

Rise-, fall- and delaytimes: If not otherwise stated, all rise times are between 10% and 90%, fall times between 90% and 10% and delay times at 50% of the relevant steps.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>S</sub>	Supply voltage	static destruction proof	-1		40	V
		dynamic destruction proof t < 0.5s (single pulse, T <sub>j</sub> < 85°C)	-2		40	V
V <sub>LI</sub>	Logic inputs IN1, IN2, DI, EN, SS, SI, SCK, DMS		-0.5		7	V
V <sub>LO</sub>	Logic outputs SF, SO		-0.5		7	V

**Table 4. Thermal Data**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T <sub>j</sub>	Junction temperature		-40		+150	°C
		dynamic t < 1 s			+175	°C
T <sub>stg</sub>	Storage temperature		-55		+125	°C
T <sub>amb</sub>	Ambient temperature		-40		+125	°C
R <sub>th j-case</sub>	Thermal resistance junction to case (*)				3	°C/W
T <sub>j_s</sub>	Thermal Shutdown Junction Temperature Threshold		160	175	190	°C
T <sub>j_reg</sub>	Start of Temperature dependent Current Regulation		150	165	180	°C

(\*) Guaranteed by design and package characterization.

**Table 5. Electrical Characteristics**

(T<sub>j</sub> = -40 to +150°C; V<sub>S</sub> = 5 to 28V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>POWER SUPPLY</b>						
V <sub>S</sub>	Supply Voltage	Static Condition	4.5		28	V
		Dynamic Condition (t < 500ms)			40	V
	Undervoltage Shutdown	(at least down to 2.5V) (*)				
	Switch OFF voltage				4.4	V
	Switch ON voltage				4.7	V
	Hysteresis			200		mV
V <sub>DMS</sub>	SPI Undervoltage Shutdown	Device used in SPI mode	2.5	2.8	3.1	V
I <sub>S</sub>	Supply current	f = 0 kHz, I <sub>O</sub> = 0 A			13	mA
		f = 20kHz, I <sub>O</sub> = 0 A			30	mA

(\*) For supply voltages down to 2.5V the output stages are in tristate condition and the status flag is set to low. Below 2.5V the device operates in undefined condition

**Table 5. Electrical Characteristics** (continued)(T<sub>j</sub> = -40 to +150°C; V<sub>S</sub> = 5 to 28V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Logic inputs</b>						
V <sub>IH</sub>	Logic Input Voltage High IN1, IN2, DI, EN		2.14			V
V <sub>IL</sub>	Logic Input Voltage Low IN1, IN2, DI, EN				0.86	V
V <sub>H</sub>	Logic Input Voltage Hysteresis IN1, IN2, DI, EN		0.1		0.6	V
I <sub>I</sub>	Logic Input Current IN1, IN2, DI	V <sub>I</sub> ≤ 1V	-200	-125		μA
I <sub>EN</sub>	Logic Input Current EN	V <sub>IEN</sub> ≥ 1V			100	μA
t <sub>dt</sub>	Detection Time EN, DI			3	4	μs
<b>Power Outputs (OUT1, OUT2)</b>						
R <sub>S</sub>	Switch on Resistance LS	R <sub>OUT-VS</sub> , V <sub>S</sub> > 5 V		150	250	mΩ
	Switch on Resistance HS	R <sub>OUT-GND</sub> , V <sub>S</sub> > 5 V		150	250	mΩ
I <sub>OU</sub> max	Switch-off Current (*)	-40 °C < T <sub>j</sub> < 165 °C T <sub>j</sub> < 175 °C	7.8	8.6 2.5	10.5(tbd)	A A
t <sub>a</sub>	Switch-off time		12	17	22	μs
t <sub>b</sub>	Blanking time		8	11.5	15	μs
t <sub>a</sub> /t <sub>b</sub>	Tracking		1.3	1.5	1.7	
I <sub>OUK</sub>	Short circuit detection current (*)		8.9	10.6	-	A
ΔI <sub>OUK</sub>	Short Circuit Current Trecking (*)		1.3	2.0	-	A
t	Reactivation time after internal shut down	Overcurrent- or overtemperature shut down to reactivation of the output stage			200	μs
I <sub>L</sub>	Leakage Current	Output stage switched off			1	mA
V <sub>FD</sub>	Free-wheel diode forward voltage	I <sub>O</sub> = 3A, V <sub>S</sub> = 0V			2	V
I <sub>SF</sub>	Output „high“ (SF not set)	V <sub>SF</sub> = 5V			20	μA
I <sub>SF</sub>	Output „low“ (SF set)	V <sub>SF</sub> = 0.5V	350			μA
		V <sub>SF</sub> = 0.8V	400			μA
		V <sub>SF</sub> = 1V	400			μA
<b>Timing</b>						
f	Maximum PWM Frequency	min. operating time 10μs Device can not be controlled with higher frequency (specify in max ratings?)		2	30	kHz
f <sub>S</sub>	Switching Frequency during current limitation	f = 1/(t <sub>a</sub> +t <sub>b</sub> )		20	50	kHz
t <sub>don</sub>	Output ON-delay	IN1 --> OUT1 or IN2 --> OUT2		3	7.5	μs
t <sub>doff</sub>	Output OFF-delay			3	5	μs
t <sub>r</sub>	Output rise time	OUT1H--> OUT1L, OUT2H--> OUT2L, I <sub>OUT</sub> = 3 A OUT1L--> OUT1H, OUT2L--> OUT2H		1	5	μs
t <sub>f</sub>	Outout fall time			1	3	μs
t <sub>ddis</sub>	Disable Delay Time	DI --> OUTn, En --> OUTn		3	7	μs
t <sub>dp</sub>	Power on Delay Time	V <sub>S</sub> = on --> output stage active			1	ms
t <sub>err</sub>	Delay time for fault detection		1		6	μs

(\*) In case of SC OUTx to gnd resp. to VS the SC switch off current is always higher than the start value of current regulation (ΔI<sub>OUK</sub> = I<sub>OUK</sub> - I<sub>OUmax</sub>)

Figure 4. Output delay time

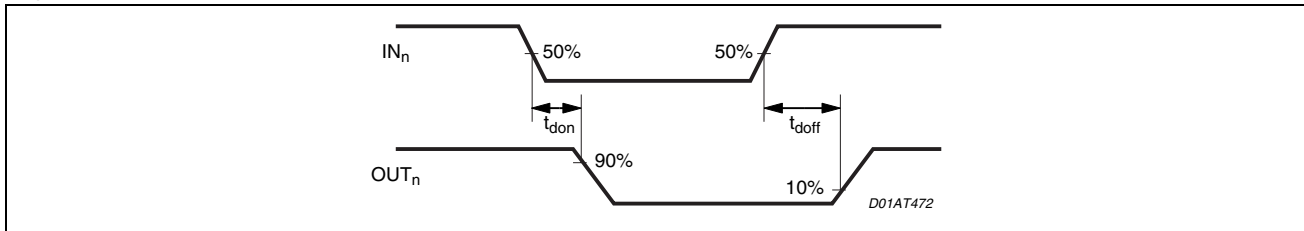


Figure 5. Disable delay time

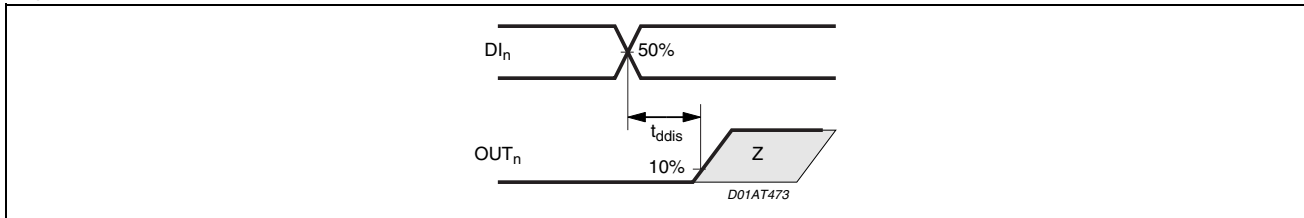


Figure 6. Output switching time

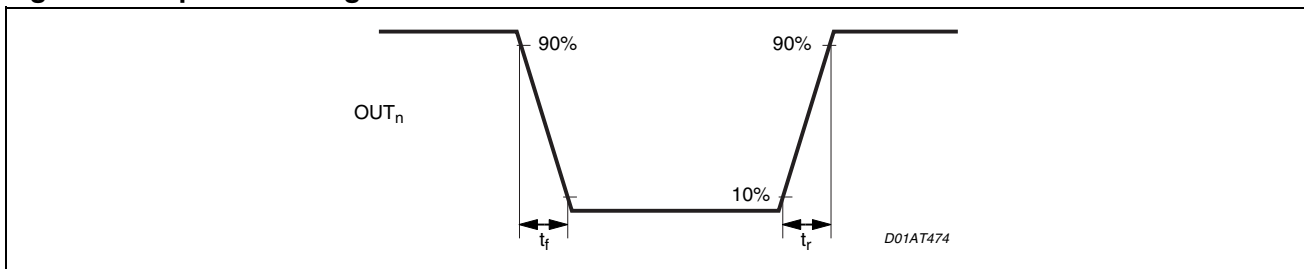


Figure 7. Current values to be inserted after characterization

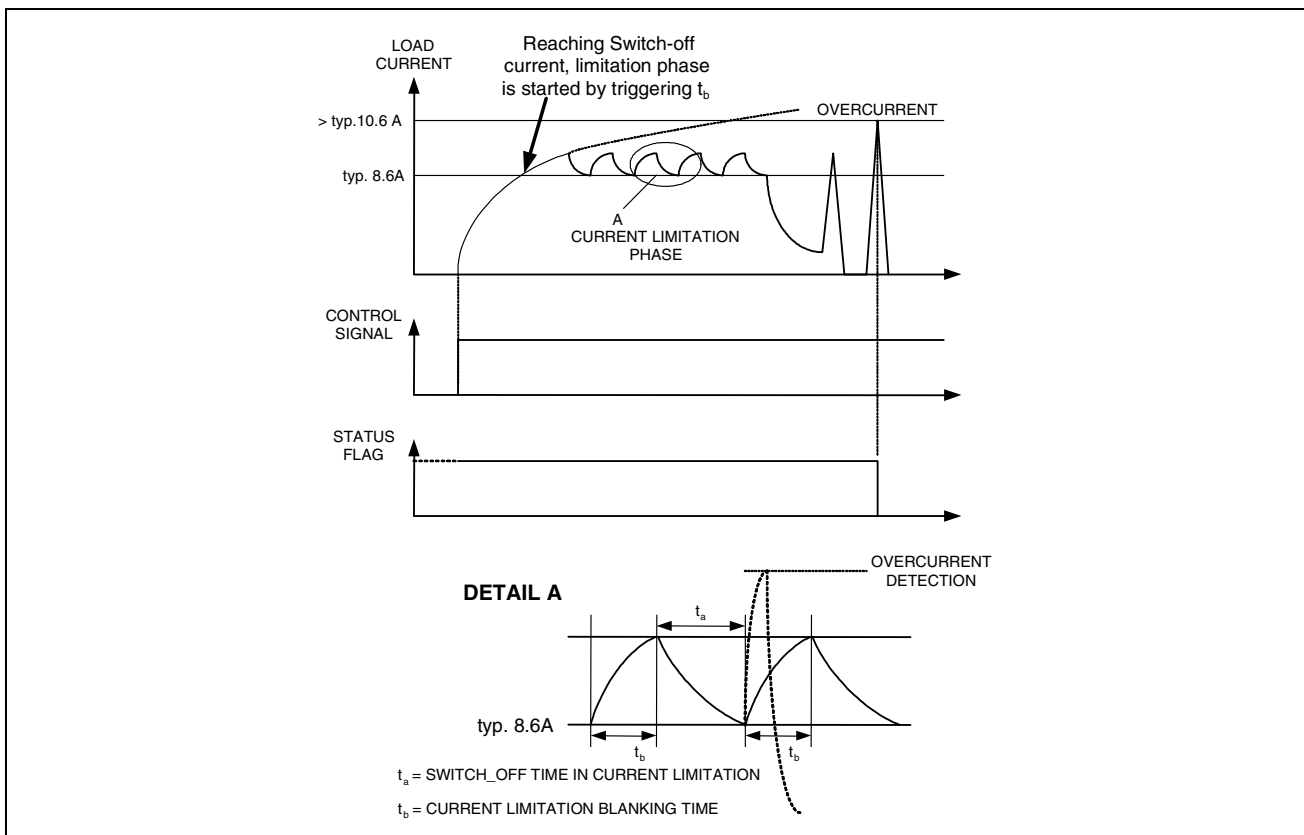


Figure 8.

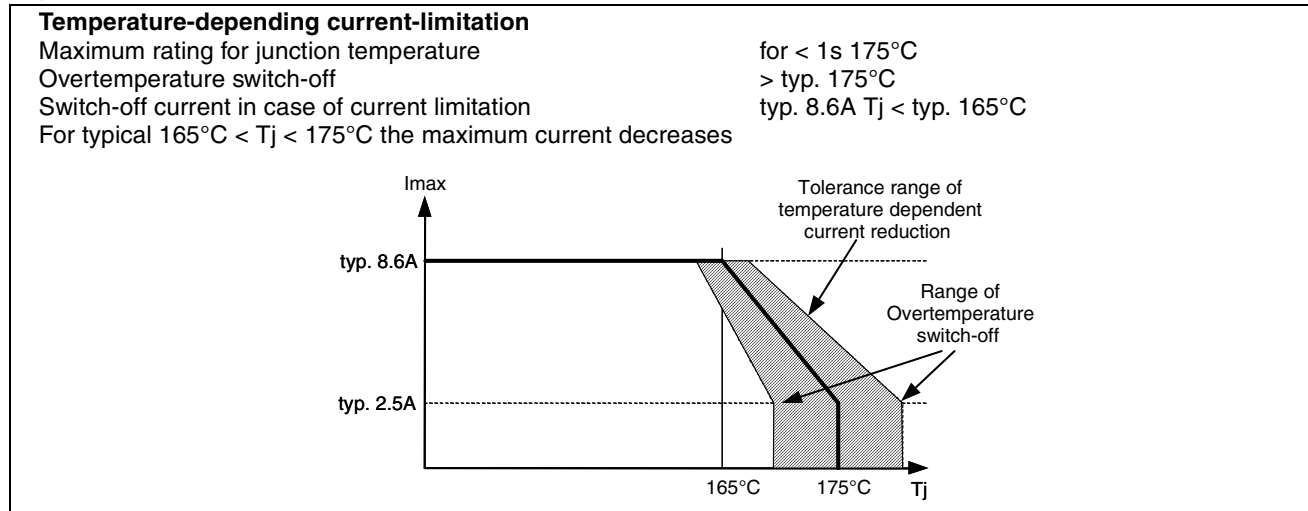


Table 5. Electrical Characteristics (continued)

**Spi Interface**

The timing of L9929 is defined as follows:

- The change at output (SO) is forced by the rising edge of the SCK signal.
- The input signal (SI) is taken over on the falling edge of the SCK signal.
- $\overline{SS} = \text{active}$  without any clocks at SCK is not allowed
- The data received during a writing access is taken over into the internal registers on the rising edge of the  $\overline{SS}$  signal, if exactly 16 SPI clocks have been counted during  $\overline{SS} = \text{active}$ .

Figure 9.

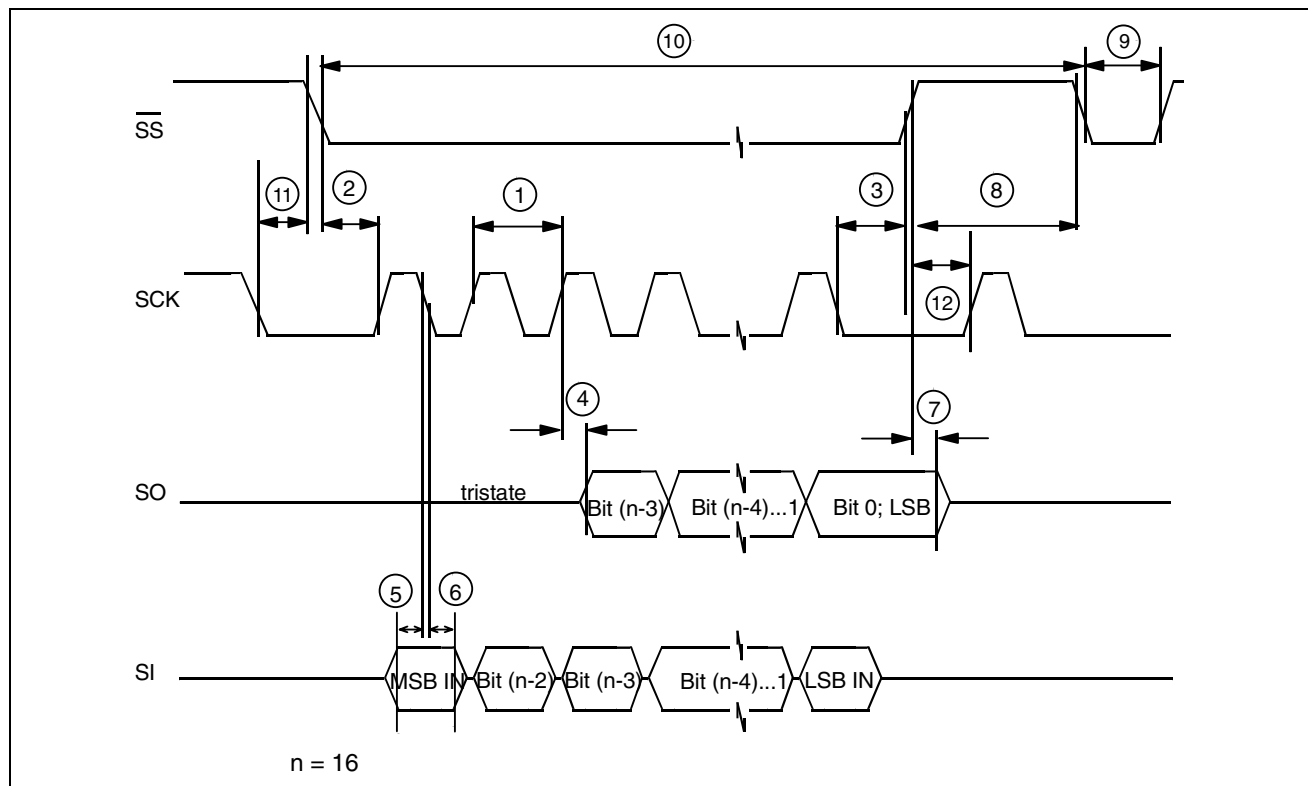


Table 5. Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Input SCK</b> (SPI clock input)						
V <sub>SCKL</sub>	Low Level				1	V
V <sub>SCKH</sub>	High Level		2			V
ΔV <sub>SCK</sub>	Hysteresis		0.1		0.4	V
C <sub>SCK</sub>	Input Capacity				10	pF
-I <sub>SCK</sub>	Input Current	Pull up current source connected to V <sub>S</sub>		20	50	μA
<b>Input SS</b> (Slave select signal)						
V <sub>SSL</sub>	Low Level	L9929 is selected			1	V
V <sub>SSH</sub>	High Level		2			V
ΔV <sub>SS</sub>	Hysteresis		0.1		0.4	V
C <sub>SS</sub>	Input Capacity				10	pF
-I <sub>SS</sub>	Input Current	Pull up current source connected to V <sub>S</sub>		20	50	μA
<b>Input SI</b> (SPI data input)						
V <sub>SIL</sub>	Low Level				1	V
V <sub>SIH</sub>	High Level		2			V
ΔV <sub>SI</sub>	Hysteresis		0.1		0.4	V
C <sub>SI</sub>	Input Capacity	Guaranteed by design			10	pF
-I <sub>SI</sub>	Input Current	Pull up current source connected to V <sub>S</sub>		20	50	μA
<b>Output SO</b> (Tristate output of the L9929 (SPI output); On active reset (DI) output SO is in tristate.)						
V <sub>SOL</sub>	Low Level	I <sub>SO</sub> = 2mA			1	V
V <sub>SOH</sub>	High Level	I <sub>SO</sub> = -2mA	2			V
C <sub>SO</sub>	Capacity	Capacity of the pin in tristate			10	pF
-I <sub>SO</sub>	Leakage Current	In tristate	-10		10	μA
<b>Input DMS</b> (Supply-Input for the SPI-Interface and Selection Pin for SPI- or SF-Mode)						
V <sub>i</sub>	Input Voltage	SPI-Mode Status-Flag-Mode	4.5		0.8	V V
I <sub>c</sub>	Input Current	SPI-Mode			10	mA
<b>Timing</b>						
t <sub>cyc</sub>	Cycle-Time (1)		200			ns
t <sub>lead</sub>	Enable Lead Time (2)		100			ns
t <sub>lag</sub>	Enable Lag Time (3)		150			ns
t <sub>v</sub>	Data Valid CL = 40pF (4) Data Valid CL = 200pF (referred to L9929)				40 150	ns ns
t <sub>su</sub>	Data Setup Time (5) (referred to master)		50			ns
t <sub>h</sub>	Data Hold Time (6)		20			ns
t <sub>dis</sub>	Disable Time (7) (referred to L9929)				100	ns

Table 5. Electrical Characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t <sub>dt</sub>	Transfer Delay (8) (referred to master)		150			ns
t <sub>SCKH</sub>	Serial clock high time (9) (referred to master)		50			ns
t <sub>SCKL</sub>	Access time (10) (referred to master)		8.35			μs
	Clock inactive before chipselct becomes valid (11)		200			ns
	Clock inactive after chipselct becomes valid (12)		200			ns
t <sub>rs</sub>	Rise-, fall time	Load on SO 50pF	20			ns
<b>TIMING</b>						
<b>Diagnostic Threshold</b> (Open Load Detection DMS > 3.1V, EN < 18V and/or DI > 2V)						
V <sub>OUT1</sub> V <sub>OUT2</sub>		Load is available	0.8 0.8			V V
V <sub>OUT1</sub> V <sub>OUT2</sub>		Load is missing	1		V <sub>s</sub> 0.8	V V
I <sub>OUT2</sub> I <sub>OUT1</sub>	Diagnostic Current	DMS > 3.1V, EN < 0.8V EN < 18V and/or DI > 2V	700 1000	1000 1500	1350 2000	μA μA
	Tracking Diagnostic Current	I <sub>OUT1</sub> / I <sub>OUT2</sub>	1.4	1.5	1.6	
t <sub>D</sub>	Delay Time	* After disabling the device, the load has to be demagnetized during t <sub>D</sub> , to avoid erroneous OL detection	30		100	ms

### 3 Truth Table

Table 6. Truth Table

Pos.	DI	EN	IN1	IN2	OUT1	OUT2	SF <sup>3)</sup>	SPI <sup>4)</sup> DIA_REG
1. Forward	L	H	H	L	H	L	H	See Diagnostics / Encoding of Failures
2. Reverse	L	H	L	H	L	H	H	
3. Free-wheeling low	L	H	L	L	L	L	H	
4. Free-wheeling high	L	H	H	H	H	H	H	
5. Disable	H	X	X	X	Z	Z	L	
6. Enable	X	L	X	X	Z	Z	Z	
7. IN1 disconnected	L	H	Z	X	H	X	H	
8. IN2 disconnected	L	H	X	Z	X	H	L	
9. DI disconnected	Z	X	X	X	Z	Z	L	
10. EN disconnected	X	Z	X	X	Z	Z	L	
11. Current limit. active	L	H	X	X	Z	Z	H	
12. Undervoltage active <sup>1.)</sup>	X	X	X	X	Z	Z	L	
13. Overtemperature <sup>2.)</sup>	X	X	X	X	Z	Z	L	
14. Overcurrent <sup>2.)</sup>	X	X	X	X	Z	Z	L	



- 1.) In case of undervoltage tristate and status-flag are reset automatically.
- 2.) Whenever overcurrent or overtemperature is detected, the fault is stored (i.e. status-flag remains low).  
The tristate conditions and the status-flag<sup>3)</sup> are reset via DI or EN.

L = Low

H = High

X = High or Low

Z = High impedance

(all output stage transistors are switched off in static state. For more inform. see next page)

Overcurrent:  $I_{OUT1,2} > 10.6 \text{ A}$

Overtemperature:  $T_j > 175^\circ\text{C}$

Undervoltage:  $V_{VS-GND} < 4.5\text{V}$  (at least down to 2.5V)

- 3.) If Mode „Status-Flag“ is selected (see chapter "Diagnostic / Status-Flag")
- 4.) If Mode „SPI-Diagnosis“ is selected (see chapter "Diagnostic / SPI-Interface")

### Description of the state „Z“

The state „Z“ has, depending on the previous operating condition different meaning.

#### 1. dynamical

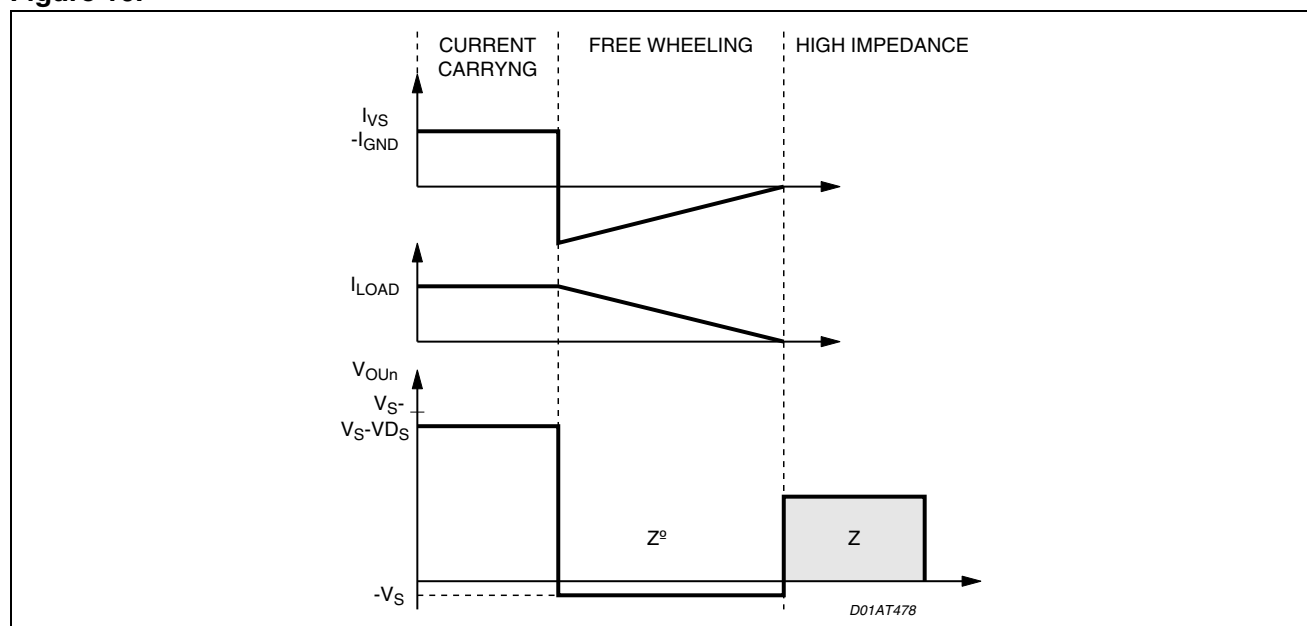
i. e. the inductive load is current carrying and is switched off according to Pos. 5, 6, 9, 10, 11, 12, 13, or 14 of the truth table

- a.) All output stage transistors are switched off.
- b.) The current flow is continued via the free wheeling diodes.
- c.) Free wheeling is detected by a negative voltage-level at OUn.
- d.) Switch on of the parallel-transistor of the current carrying diode.
- f.) Free wheeling is finished, if the voltage-level on OUn is positive again.

#### 2. statical

- g.) all output-stages switched off.

**Figure 10.**



## 4 Diagnostic

The Diagnosis-Mode can be selected between SPI-Diagnosis and Status-Flag Diagnosis.

The choice of the Diagnosis-Mode is selected by the voltage-level on pin 12 (DMS Diagnosis Mode Selection).

DMS = GND    Status-Flag

DMS = Vcc    SPI-Diagnostic

For the connection of pins SI, SO, SS and SCK/SF see Fig. 13 respectively Fig. 14.

### 4.1 Status-Flag

The Status-Flag shows the condition „tristate“.

At the following fault-cases the output-stages switches in tristate and set the status-flag from high to low.

- Short circuit of OUT1 or OUT2 against  $V_S$  or GND
- Short circuit between OUT1 and OUT2
- Overcurrent
- Overtemperature
- Undervoltage on  $V_S$

In cause of short circuit or overcurrent, the fault will be stored.

The output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is exceeded.

If the voltage level changes from high to low on DI or from low to high on EN, the output stage switches on again and the status-flag is reset to high-level.

In cause of overtemperature the fault will be stored.

The output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is exceeded.

If the voltage level changes from high to low on DI or from low to high on EN, the output stage switches on again and the status-flag is reset to high-level.

In cause of undervoltage on  $V_{Batt}$  the output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is fallen. If the voltage has risen about the specified value again, the output stage switches on again and the status-flag is reset to high-level.

The maximum current which can flow under normal operating conditions is limited to typical  $I_{max.} = 8.6A$  .

When the maximum current value is reached, the output stages are switched tristate for a fixed time.

According to the time-constant the current decreases exponentially until the next switch-on occurs.

At the end if the fixed time the output stage switches on again and the status-flag is reset to high-level.

## 5 SPI-INTERFACE

### 5.1 General Discription

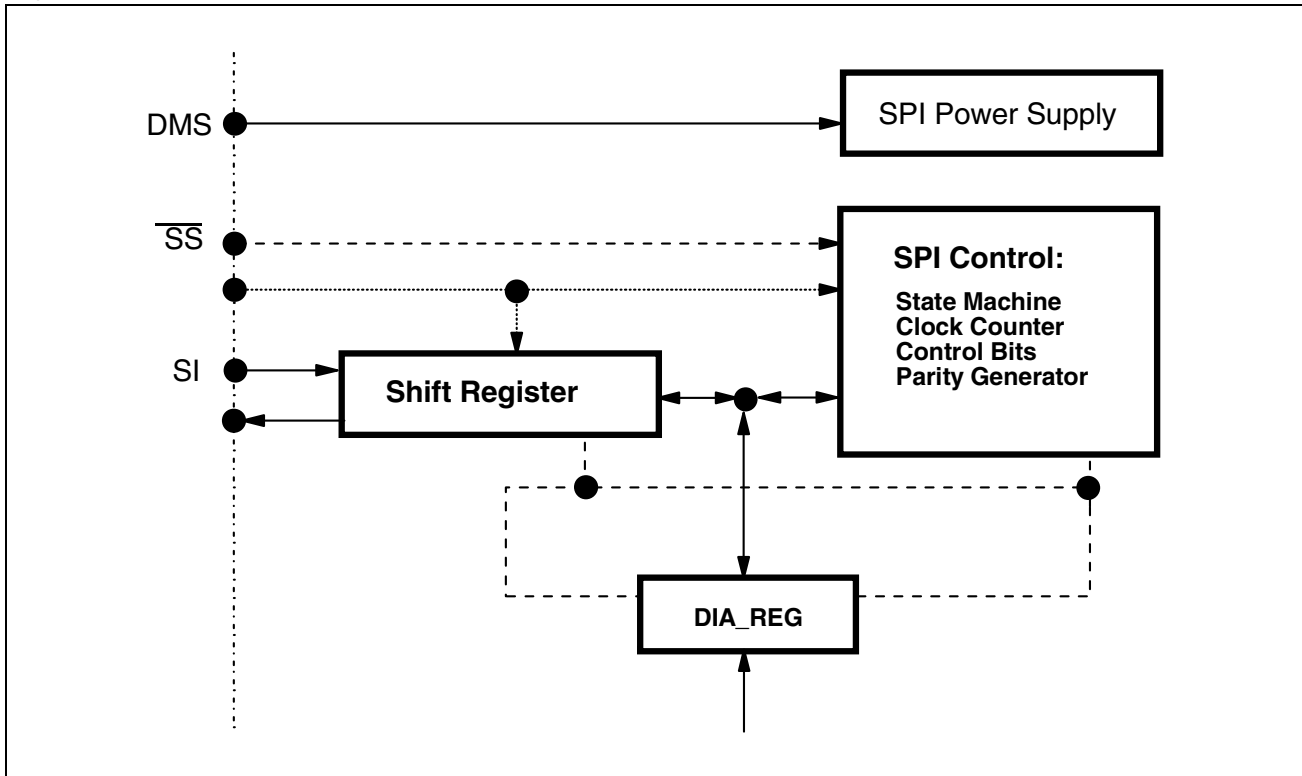
The serial SPI interface establishes a communication link between L9929 and the systems microcontroller. L9929 always operates in slave mode whereas the controller provides the master function.

The maximum baud rate is 2 MBaud (200pF).

Applying an active slave select signal at SS L9929 is selected by the SPI master. SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI clock is provided by the master.

In case of inactive slave select signal (High) the data output SO goes into tristate.

Figure 11.



## 5.2 Power Supply of the SPI-Interface

SPI-Logic and I/O-Pins are alternativ supplied from DMS or Vcc internal, depending on which voltage is higher. That is why diagnosis of the EN-/DI-Pins is always possible, even in case of missing H-Bridge-power supply e.g. during „Vorlauf/Nauchlauf“.

## 5.3 Characteristics of the SPI Interface

- 1) When DMS is > 3.1V, the SPI is active, independent of the state of EN or DI and the voltage on V<sub>S</sub>. During active reset conditions (DMS < 2.5V) the SPI is driven into its default state. When reset becomes inactive, the state machine enters into a waitstate for the next instruction.
- 2) If the slave select signal at SS is inactive (high), the state machine is forced to enter the waitstate, i.e. the state machine waits for the following instruction.
- 3) During active (low) state of the select signal  $\overline{SS}$  the falling edge of the serial clock signal SCK will be used to latch the input data at SI. Output data at SO are driven with the rising edge of SCK. Further processing of the data according to the instruction ( i.e. modification of internal registers) will be triggered by the rising edge of the  $\overline{SS}$  signal. (-> See Note)
- 4) Chipaddress: In order to establish the option of extended addressing the uppermost two bits of the instruction-byte ( i.e the first two SI-bits of a Frame ) are reserved to send a chipaddress. To avoid a busconflict the output SO must stay high impedant during the addressing phase of a frame (i.e. until the addressbits are recognised as valid chipaddress). This tristate behavior should be realised in any case, regardless wether the extended addressoption is used or not. If the chipaddress does not match, the according access will be ignored and SO remains high impedant for the complete frame regardless which frametype is applied.
- 5) Check byte: Simultaneously to the receipt of an SPI instruction L9929 transmitts a check byte via the output SO to the controller. This byte indicates regular or irregular operation of the SPI. It contains an initial bitpattern and a flag indicating an invalid instruction of the previous access.

- 6) On the read access the databits at the SPI input SI are rejected.
- 7) Invalid instruction/access: An instruction is invalid, if one of the following conditions is fulfilled:
  - An unused instruction code is detected (see tables with SPI instructions).
  - In case the previous transmission is not completed in terms of internal data processing. ( Violation of the minimum Access-Time. )
  - In case of the previous transmission has detected more than 16 SCK pulses
  - Reset has occurred (Undervoltage on DMS)

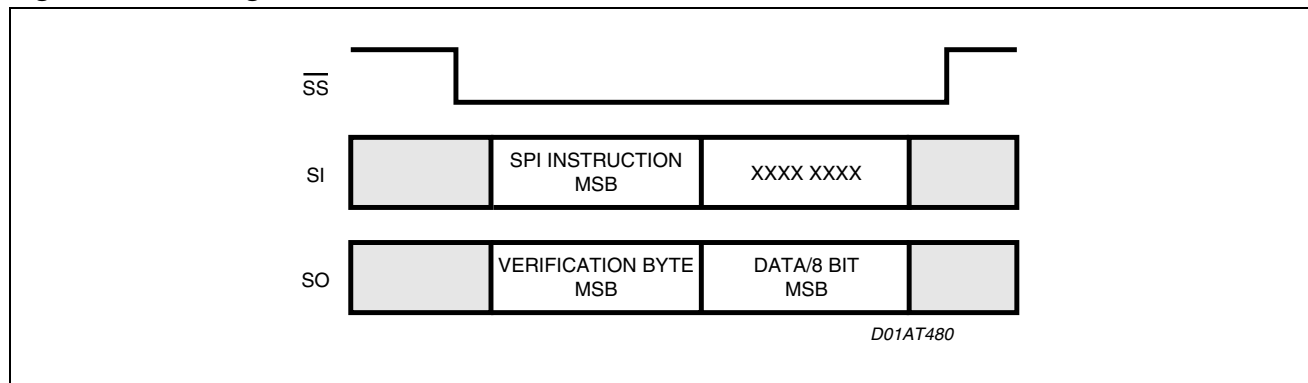
If an invalid instruction is detected, any modifications on registers of L9929 are not allowed.

In case an unused instruction code occurred the databyte "ffh ex" will be transmitted after having sent the check byte.

In addition any access is invalid if the number of SPI clock pulses (falling edge) counted during active SS differs from exactly 16 clock pulses (-> See Note).

### 5.4 SPI Communication

Figure 12. Reading access / 8 bit



### 5.5 SPI Instruction

The uppermost 2 bit of the instruction byte contains the chipaddress. The chipaddress of L9929 is 00.

MSB							
7	6	5	4	3	2	1	0
0	0	INSTR5	INSTR4	INSTR3	INSTR2	INSR1	INSR0

SPI Instruction	Encoding		Description
	bit 7,6 CPAD1,0	bit 5,4,3,2,1,0 INSTR(5...0)	
RD_IDENT	00	000 000	Read identifier
RD_VERSION	00	000 011	Read version
RD_DIA	00	001 001	Read DIA_REG
		All others	No function

## 5.6 Reset of the Diagnostic Register DIA\_REG

On the following conditions DIA\_REG is reset:

- With the rising edge of the SS-signal after the SPI-Instruction RD\_DIA (only if error free while SS, new errors will actualize DIA\_REG with the rising edge of SS).
- When the voltage on DMS exceeds the threshold for detecting SPI-Mode. (after undervoltage condition or after power up)
- - If VS rises over about the undervoltage level, the Bits of DIA\_REG are restored (when VS internal or DMS > 3,1V)

Verification byte:

MSB							
7	6	5	4	3	2	1	0
Z	Z	1	0	1	0	1	TRANS_F
Bit	Name		Description				
0	TRANS_F		Bit = 1: error detected during previous transfer Bit = 0: previous transfer was recognised as valid				
1			Fixed to High				
2			Fixed to Low				
3			Fixed to High				
4			Fixed to Low				
5			Fixed to High				
6			Send as high impedance				
7			Send as high impedance				

## 5.7 Diagnostics/Encoding of Failures

Description of the SPI Registers (SPI Instructions: RD\_DIA)

Register: DIA_REG							
7	6	5	4	3	2	1	0
Active	OT	CurrRed	CurrLim	DIA21	DIA20	Dia11	DIA10
State of Reset: FFH							
Access by Controller: Read only							
Bit	Name		Description				
0	DIA 10		Diagnosis-Bit1 of OUT1				
1	DIA 11		Diagnosis-Bit2 of OUT1				
2	DIA 20		Diagnosis-Bit1 of OUT2				
3	DIA 21		Diagnosis-Bit2 of OUT2				
4	CurrLim		Is set to „0“ in case of current limitation				
5	CurrRed		Is set to „0“ in case of temperature dependet current limitation				
6	OT		Is set to „0“ in case of overtemperature				
7	Active		Shows the wired-or state of the Pins EN and DI				

Encoding of the Diagnostic Bits of the Output-Stages OUT1 and OUT2				
DIA21	DIA20	DIA11	DIA10	
-	-	0	0	Short circuit over load (SCOL)
-	-	0	1	Short circuit to battery on OUT1 (SCB1)
-	-	1	0	Short circuit to ground on OUT1 (SCG1)
-	-	1	1	No error detected on OUT1
0	0	-	-	Open load
0	1	-	-	Short circuit to battery on OUT2 (SCB2)
1	0	-	-	Short circuit to ground on OUT2 (SCG2)
1	1	-	-	No error detected on OUT2

0	0	0	0	Undervoltage on Pin V <sub>S</sub>
---	---	---	---	------------------------------------

Description of DIA\_REG Bit7

EN	DI	DIA_REG Bit7
0	0	0
0	1	0
1	0	1
1	1	0

## 5.8 Device Identifier and Revision Number

The IC's identifier is used for production test purposes and features plug & play functionality depending on the systems software release. It is made up on a device-number and a revision number each one read-only accessible via standardised instructions.

The Device number is defined once to allow identification of different IC-Types by software.

The Revision number may be utilised to distinguish different states of hardware. The contents is divided into an upper 4 bit field reserved to define revisions correspondending to specific software releases. The lower 4 bit field is utilised to identify the actual maskset.

Both (SWR and MSR) will start with 0000b and are increased by 1 every time an according modification of the hardware is introduced.

## 5.9 Reading the IC Identifier (SPI Instruction: RD\_IDENT):

IC Identifier1 (Device ID)							
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Bit	Name		Description				
7...0	ID(7...0)		ID-No.: 1010 0001				

## 5.10 Reading the IC revision number (SPI Instruction: RD\_VERSION):

IC's revision number							
7	6	5	4	3	2	1	0
SWR3	SWR2	SWR1	SWR0	MSR3	MSR2	MSR1	MSR0
Bit	Name		Description				
7...4	SWR(3...0)		Revision corresponding to Software release: 0Hex				
3...0	MSR(3...0)		Revision corresponding to Maskset: 8Hex				

Figure 13. Application example with SPI-Interface

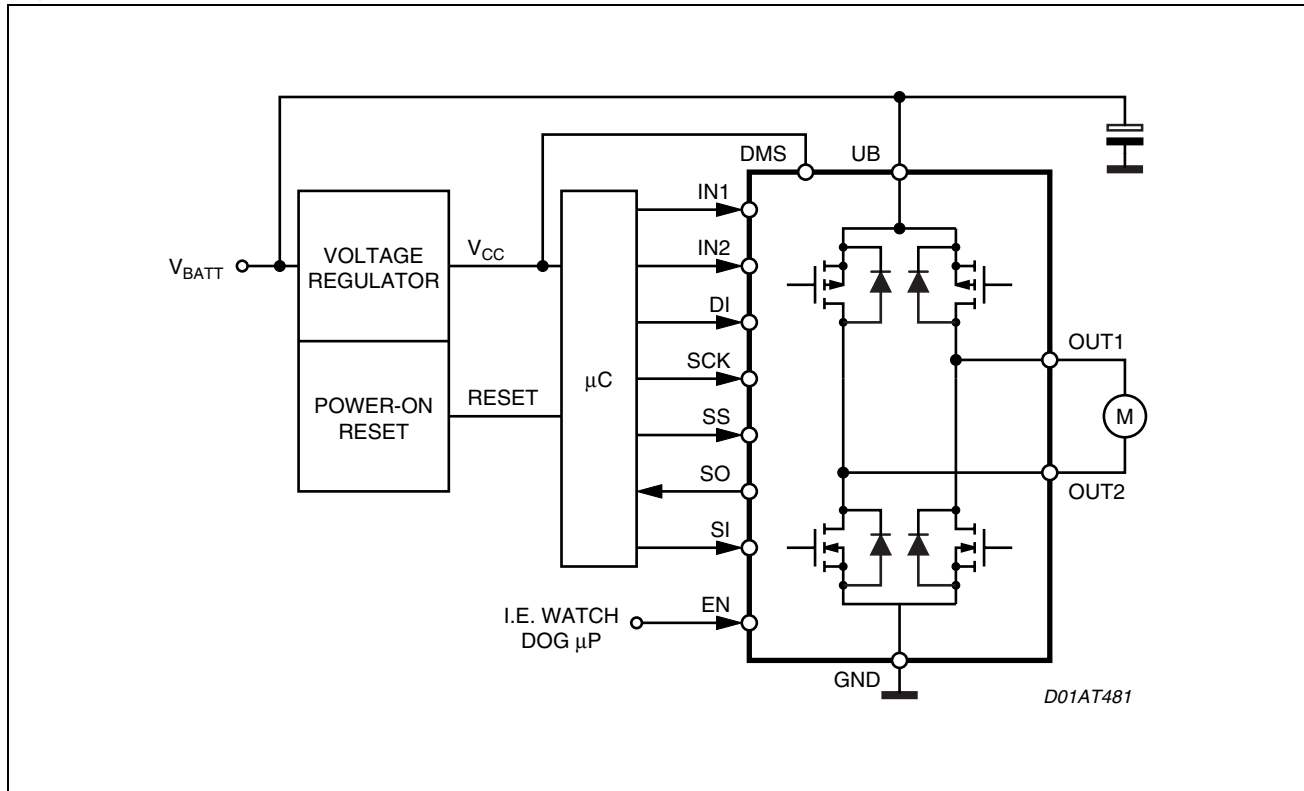


Figure 14. Application example with Status-Flag

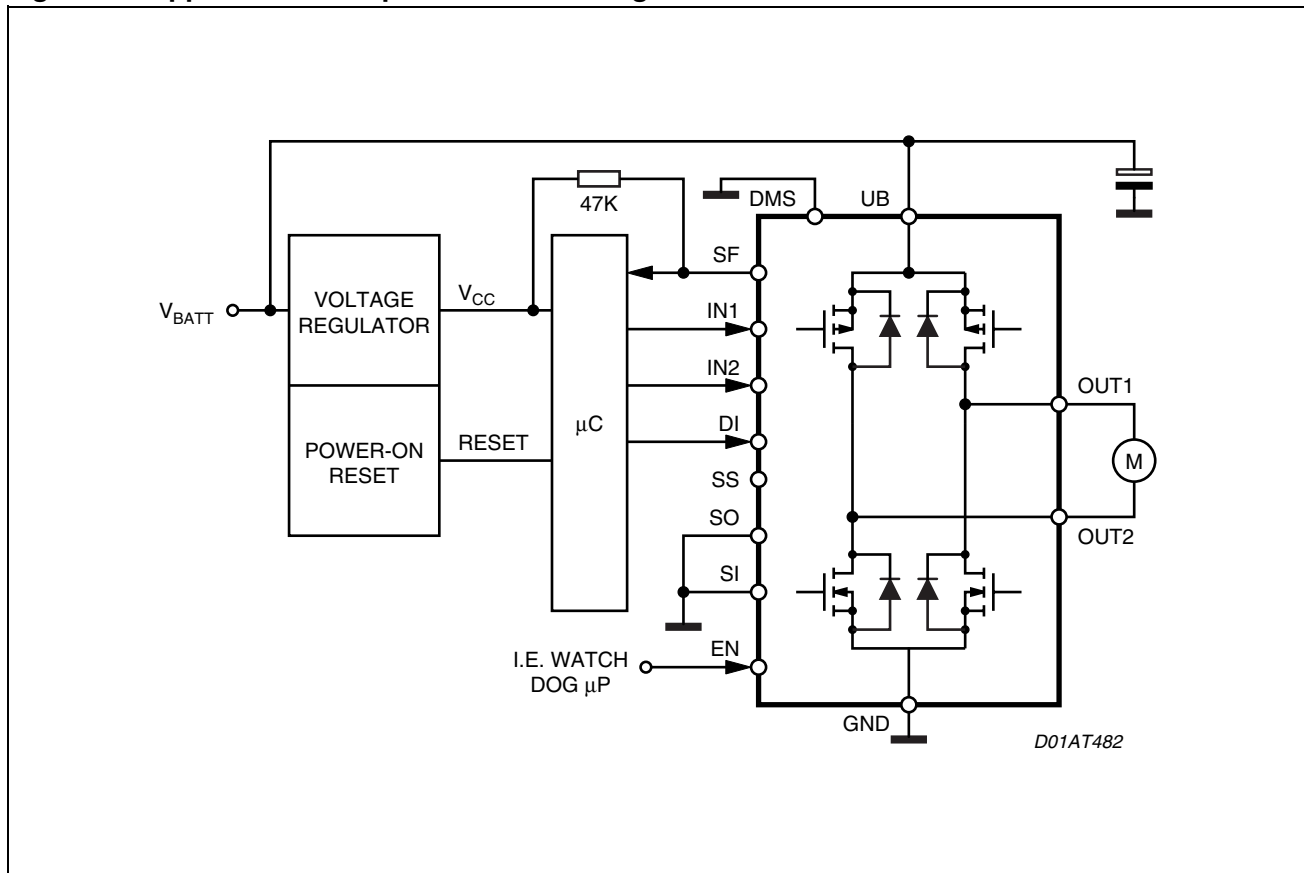
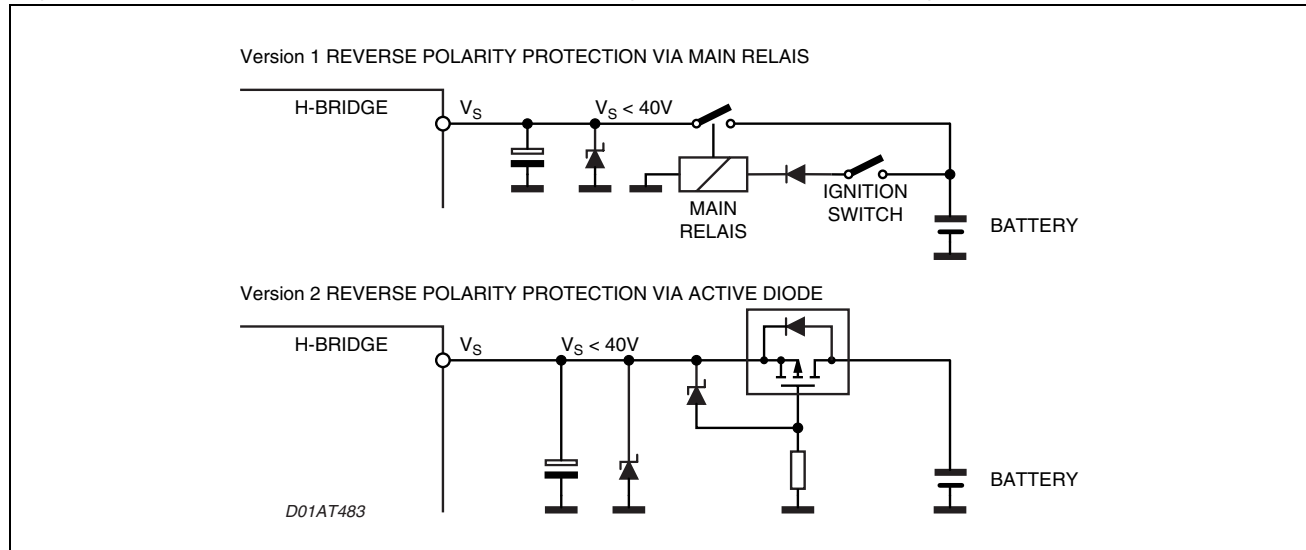


Figure 15. Application examples for Overvoltage- and Reverse-Voltage Protection



## 6 ESD-SOLIDITY

The connection pins of the IC have to be protected against Electrostatic Discharge (ESD) by suitable integrated protection structures.

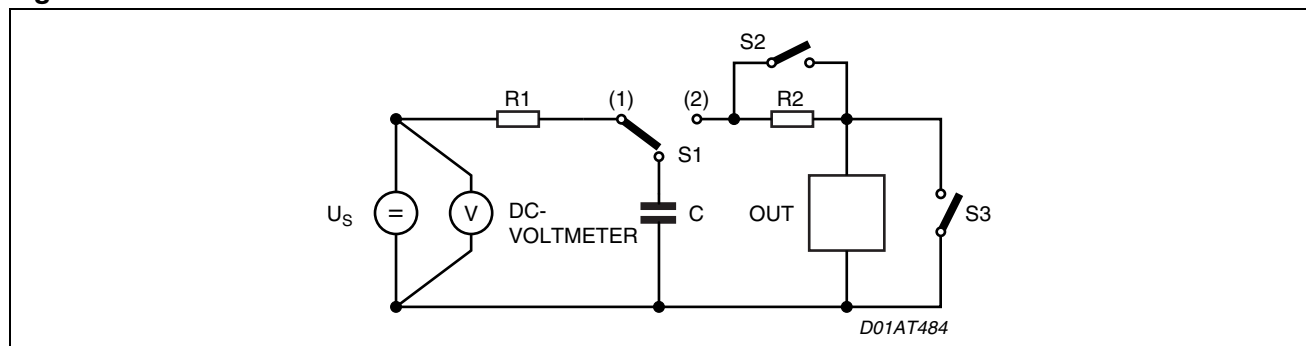
The integrated circuit has to meet the demand of the „Human-Body-Model“ with  $V_C = \pm 4\text{kV}$   
 $C = 100\text{pF}$  and  $R_2 = 1,5\text{k}\Omega$  ( $330\Omega$  for OUT1 and OUT2).

Thereby any defect or destruction of the integrated circuit must not occur.

The protection structures realized to reach the ESD-strength have to be coordinated.

The ESD-strength has to be verified by the test circuit given as below.

Figure 16.



For the Pins 4, 5, 6, 7, 14 and 15

$U_C = \pm 4\text{kV}$

$R_1 = 100\text{k}\Omega$

$R_2 = 330\Omega$

$C = 100\text{pF}$

Number of pulses each pin: 18

Frequency: 1Hz

Arrangement and performance:

The requirements of MIL883D Methode 3015 have to be fulfilled.



## 7 ISO-PULSES

In the main-power-supply-system disturbance transients according to ISO 7637-1 First Edition 1990-06-01 may occur.

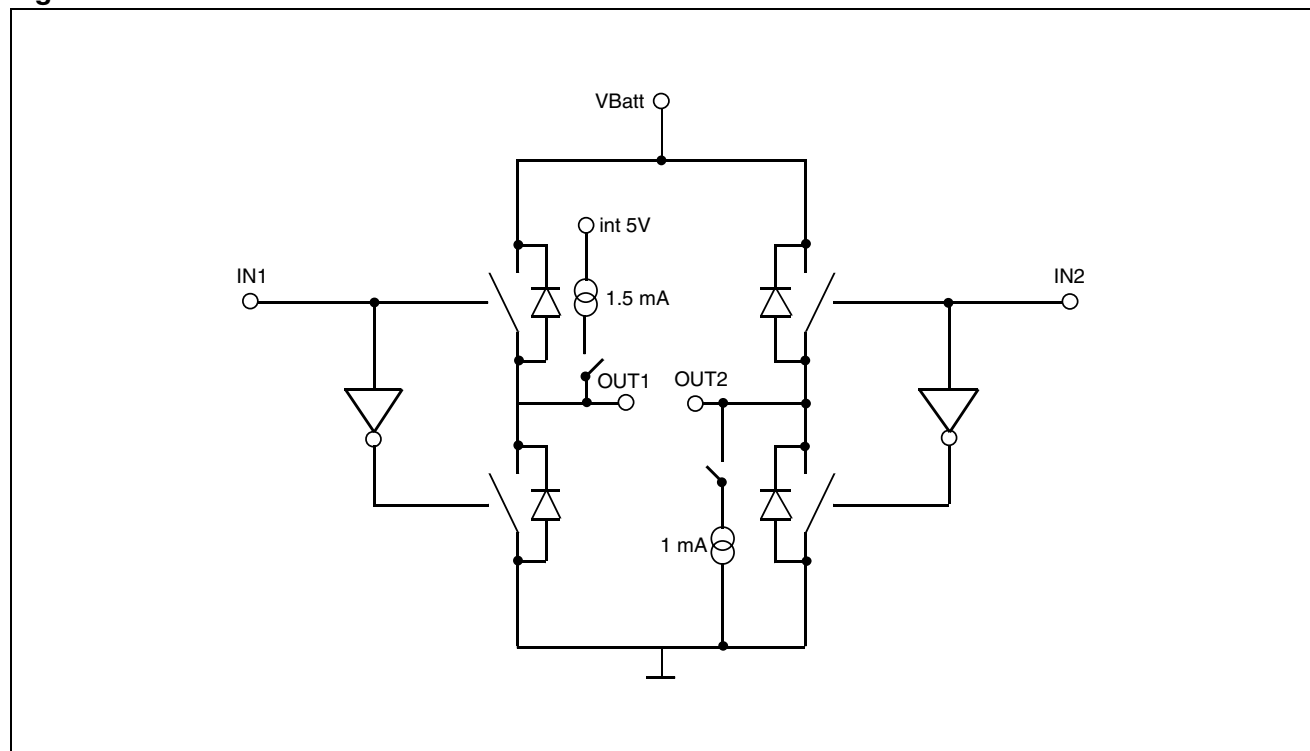
By means of external components (see Fig. 12) the following maximum ratings of the IC will not be exceeded.

statical	-1V ..... +40V
dynamical for $t < 500$ ms	-2V ..... +40V

### APPENDIX A

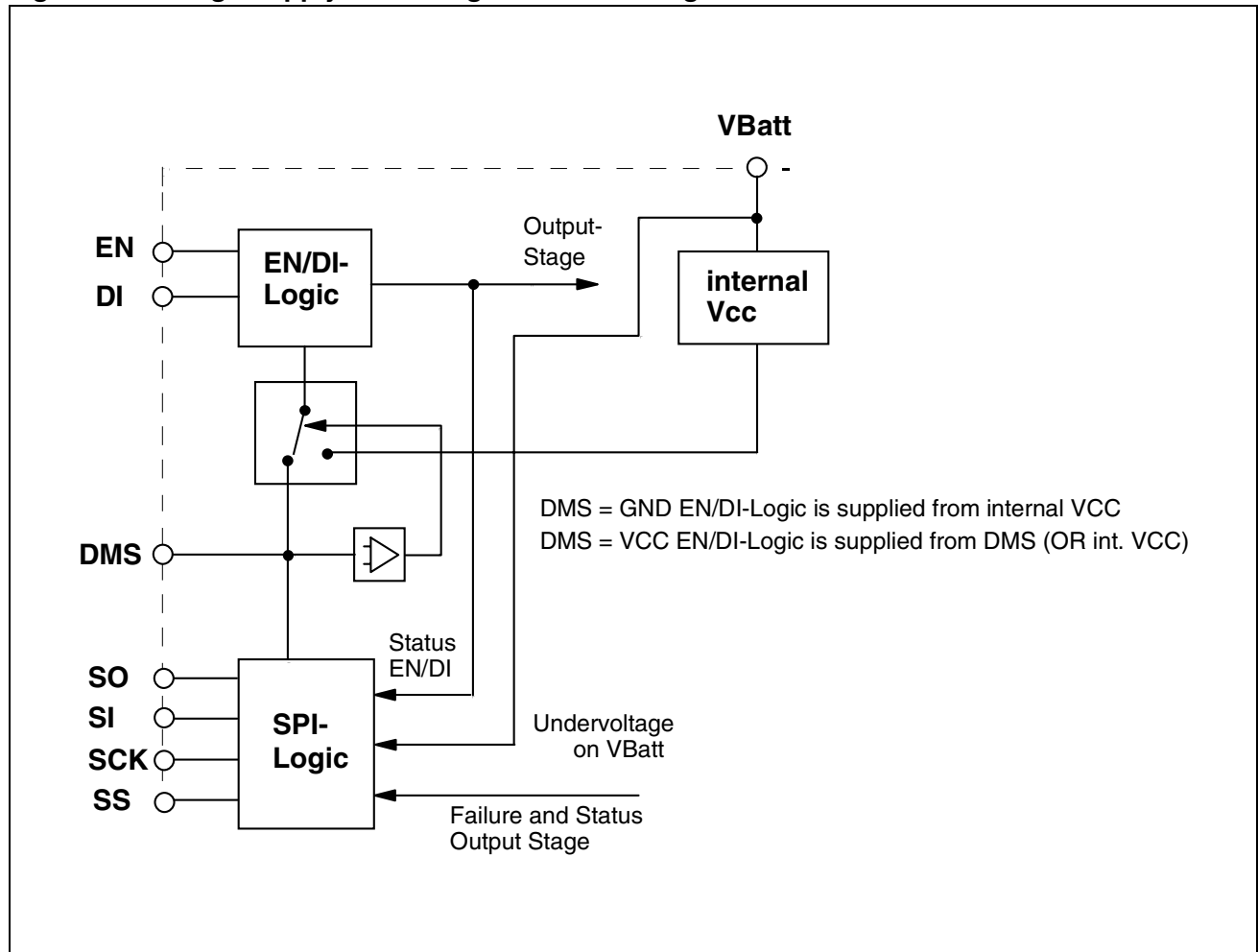
	OUT1	OUT2	
Load available	1	1	
Open Load	1	0	
SC -> GND on OUT1 with Load	0	0	SC detected on normal operation
SC -> GND on OUT2 with Load	0	0	SC detected on normal operation
SC -> UB on OUT1 with Load	1	1	SC detected on normal operation
SC -> UB on OUT2 with Load	1	1	SC detected on normal operation
SC -> GND on OUT1 Open Load	0	0	OL not detected Double Fault
SC -> GND on OUT2 Open Load	1	0	OL detected
SC -> UB on OUT1 Open Load	1	0	OL detected
SC -> UB on OUT2 Open Load	1	1	OL not detected Double Fault

Figure 17.



## 8 APPENDIX B

Figure 18. Voltage Supply of SPI-Logic and EN/DI-Logic



## 9 Package Information

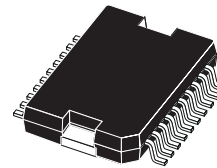
Figure 19. PowerSO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max. )					
T		10			0.394	

- (1) "D and E1" do not include mold flash or protrusions.  
 - Mold flash or protrusions shall not exceed 0.15mm (0.006")  
 - Critical dimensions: "E", "G" and "a3".  
 (2) For subcontractors, the limit is the one quoted in jecdec MO-166

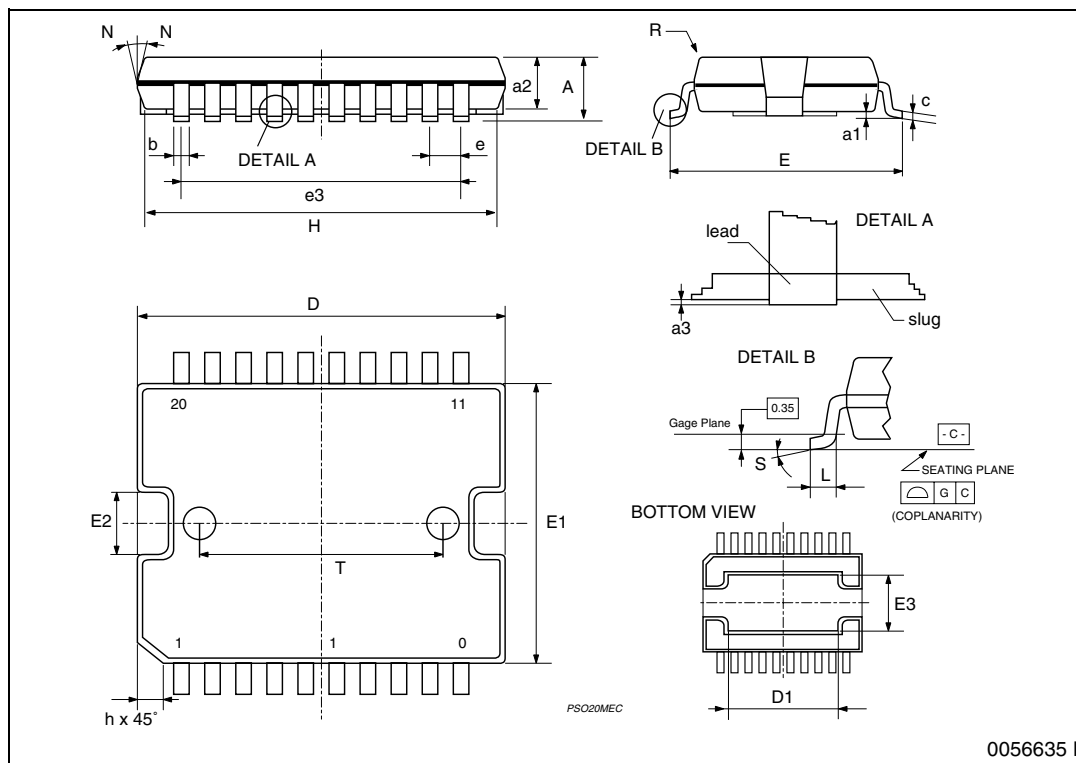
### OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO20



## 10 Revision History

Table 7. Revision History

Date	Revision	Description of Changes
07-Mar-2005	1	First Issue

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