M62356P

8-BIT 8CH D-A CONVERTER

DESCRIPTION

The M62356P is an integrated circuit semiconductor of C-MOS structure with 8 channels of built-in D-A converters.
The input data is a easy-to-use 3-wires serial data transfer method and it is able to cascading serial use with Do terminal.

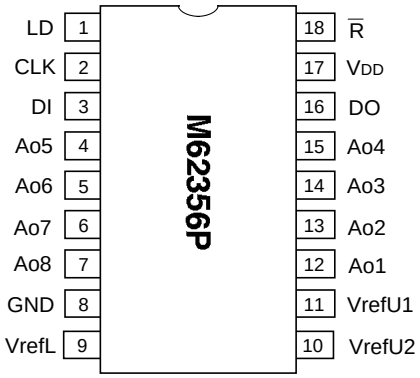
FEATURES

•Digital data transfer format
3-wires serial data transfer method
•Output voltage range 0V to 12V
•Short setting time
•D-A converter high level reference voltage is possess two input terminal then two reference voltage is possible to input.
Digital voltage supply.....V_{DD}=5V±10%

APPLICATION

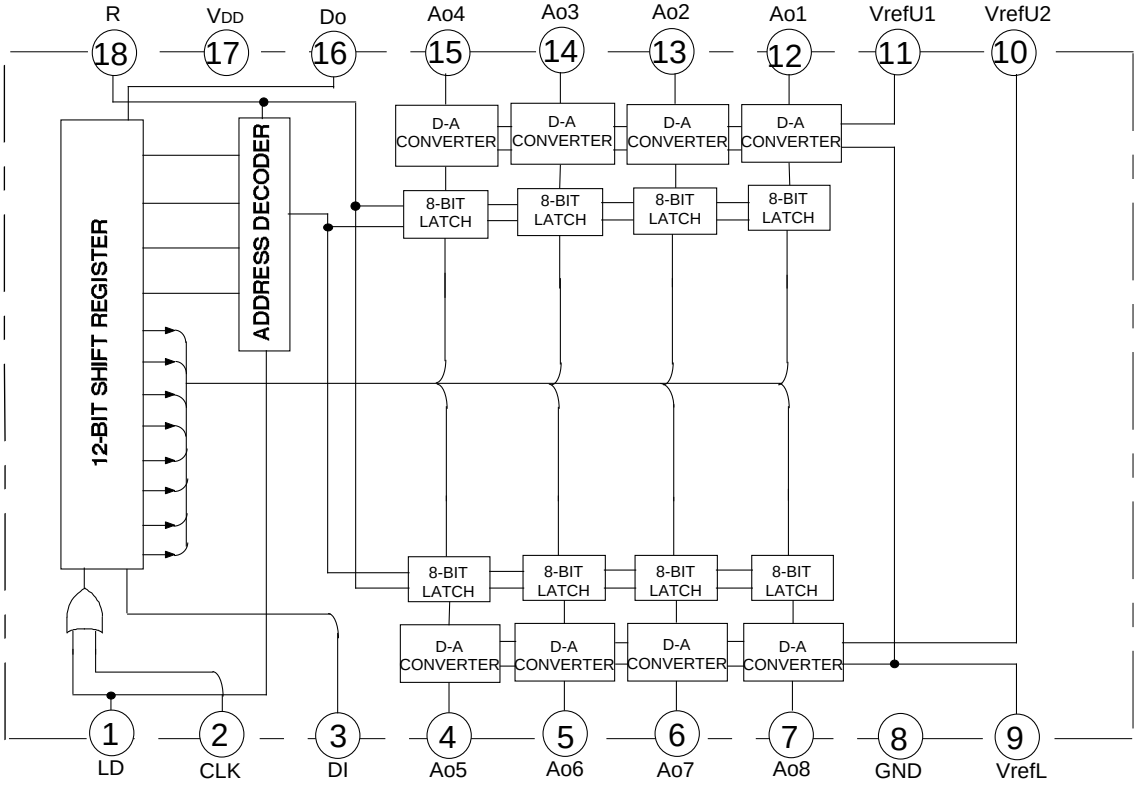
Conversion from digital control data to analog control data for home-use and industrial equipment.
Automatic adjustment by combination with EEPROM and microcomputer(replacement of conventional half-fixed resistor).
Signal gain control of DISPLAY-MONITOR or CTV.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
③	DI	Serial data input terminal
⑯	DO	Serial data output terminal
②	CLK	Serial clock input terminal
①	LD	LD terminal input high level than latch circuit data load
⑰	V_{DD}	Digital power supply terminal
⑪	VrefU1	D-A converter upper reference voltage input terminal(CH1~CH4)
⑧	GND	GND
⑩	VrefU2	D-A converter upper reference voltage input terminal(CH5~CH8)
⑨	VrefL	D-A converter lower reference voltage input terminal
⑱	$\overline{R}$	Reset terminal
⑫	Ao1	8-bit D-A converter output terminal
⑬	Ao2	
⑭	Ao3	
⑮	Ao4	
④	Ao5	
⑤	Ao6	
⑥	Ao7	
⑦	Ao8	

ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		-0.3~7.0	V
VrefU	D-A converter upper reference voltage		12.5	V
V_{IN}	Input voltage		-0.3~Vcc+0.3	V
I_{DO}	Output current		-5~+5	mA
I_{AO}	D-A converter output current		10	µA
T_{opr}	Operating temperature		-20~+75	°C
T_{stg}	Storage temperature		-40~+125	°C

RECOMMENDED OPERATING CONDITIONS

•Digital voltage supply V_{DD} 5V±10%

ELECTRICAL CHARACTERISTICS

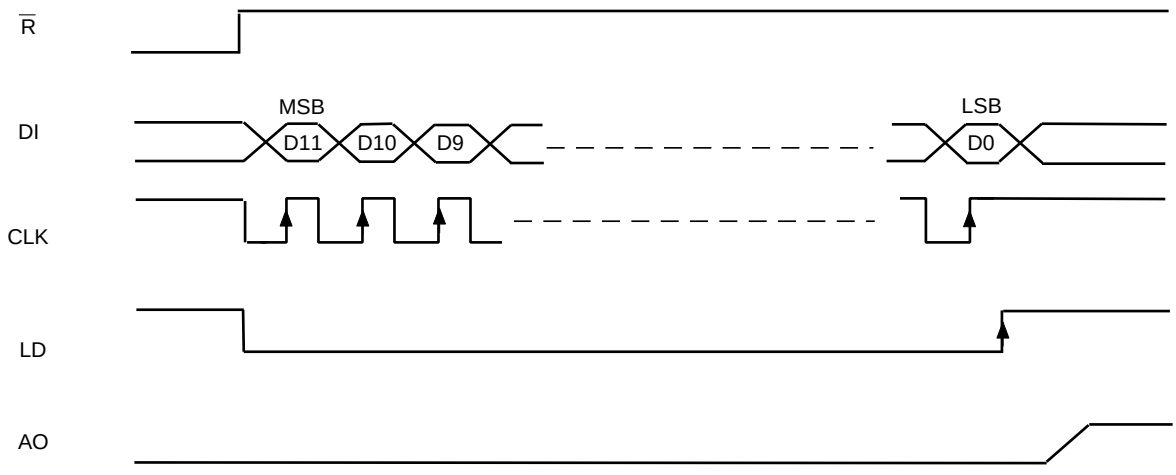
Digital part(Ta=25°C,V_{DD}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.5		5.5	V
I_{DD}	Circuit current	CLK=1MHz operation			1	mA
V_{IL}	Input low voltage				0.2V_{DD}	V
V_{IH}	Input high voltage		0.8V_{DD}			V
V_{OL}	Output low voltage	I_{OL}=1.0mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-400µA	V_{DD}-0.4			V

Analog part(V_{DD}=+5V,VrefU=12V,VrefL=0V,Ta=-20°C~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
IrefU	D-A converter upper reference input current max	All ch's set up at 107/256		1.2	2.5	mA
V_{refU}	D-A converter upper reference voltage range		3.5		12	V
V_{refL}	D-A converter lower reference voltage range				1.5	V
V_{AO}	D-A converter output voltage range		VrefL +2.5LSB		VrefU -1.5LSB	V
DNL	Differential nonlinearity	Guaranteed monotonic			±1.0	LSB
NL	Nonrineality				±1.5	LSB

TIMING CHART (MODEL)

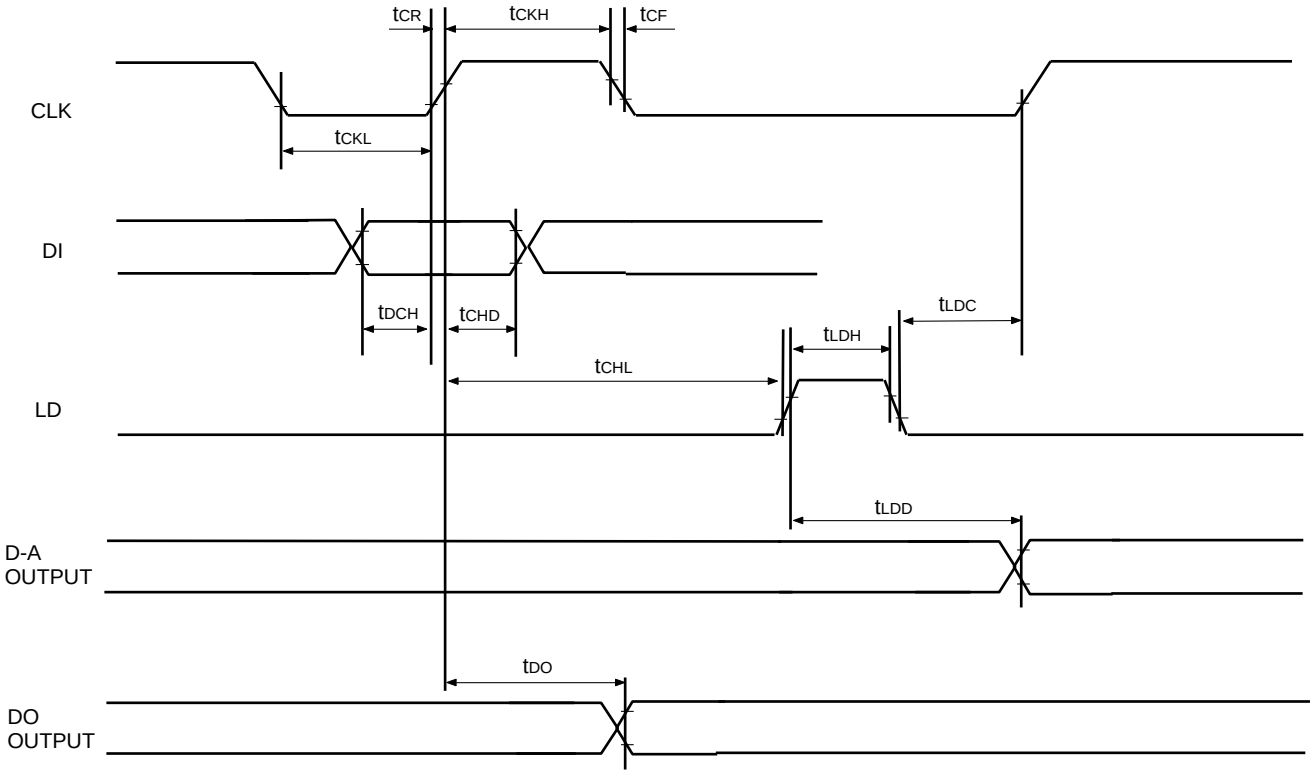


Input data is carried out LD signal Low besides CLK signal positive edge.
CLK,LD is keep generally High level.

AC CHARACTERISTICS(Ta=25°C,V_{DD}=+5V,VrefU=12V,VrefL=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CKL}	Clock "L"pulse width		200			ns
t_{CKH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data set up time		60			ns
t_{CHD}	Data hold time		100			ns
t_{CHL}	LD set up time		200			ns
t_{LDC}	LD hold time		100			ns
t_{LDH}	LD "H" pulse width		100			ns
t_{DO}	Data output delay time	C_L≤100pF	70		350	ns
t_{LDD}	Data output setting time	Without load			20	µs

TIMING CHART

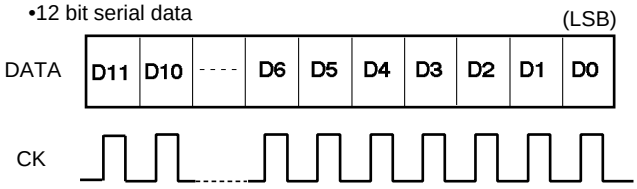


DIGITAL FORMAT

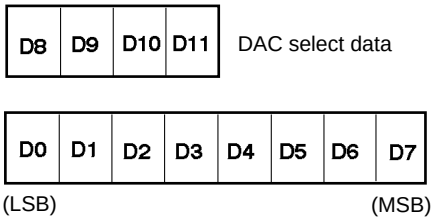
1.12-bit shift register

To set DAC,12-bit data is input in series at CLK signal"positive" edges while the LD pin status is "Low".

•12 bit serial data



•Data assignment



2.Decoder(DAC select data)

One DAC circuit is selected from among 8 circuits according to the DAC select data(4-bits:D8,D9,D11 and D14).

•DAC select data

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2 selection
0	0	1	1	Ao3 selection
0	1	0	0	Ao4 selection
0	1	0	1	Ao5 selection
0	1	1	0	Ao6 selection
0	1	1	1	Ao7 selection
1	0	0	0	Ao8 selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

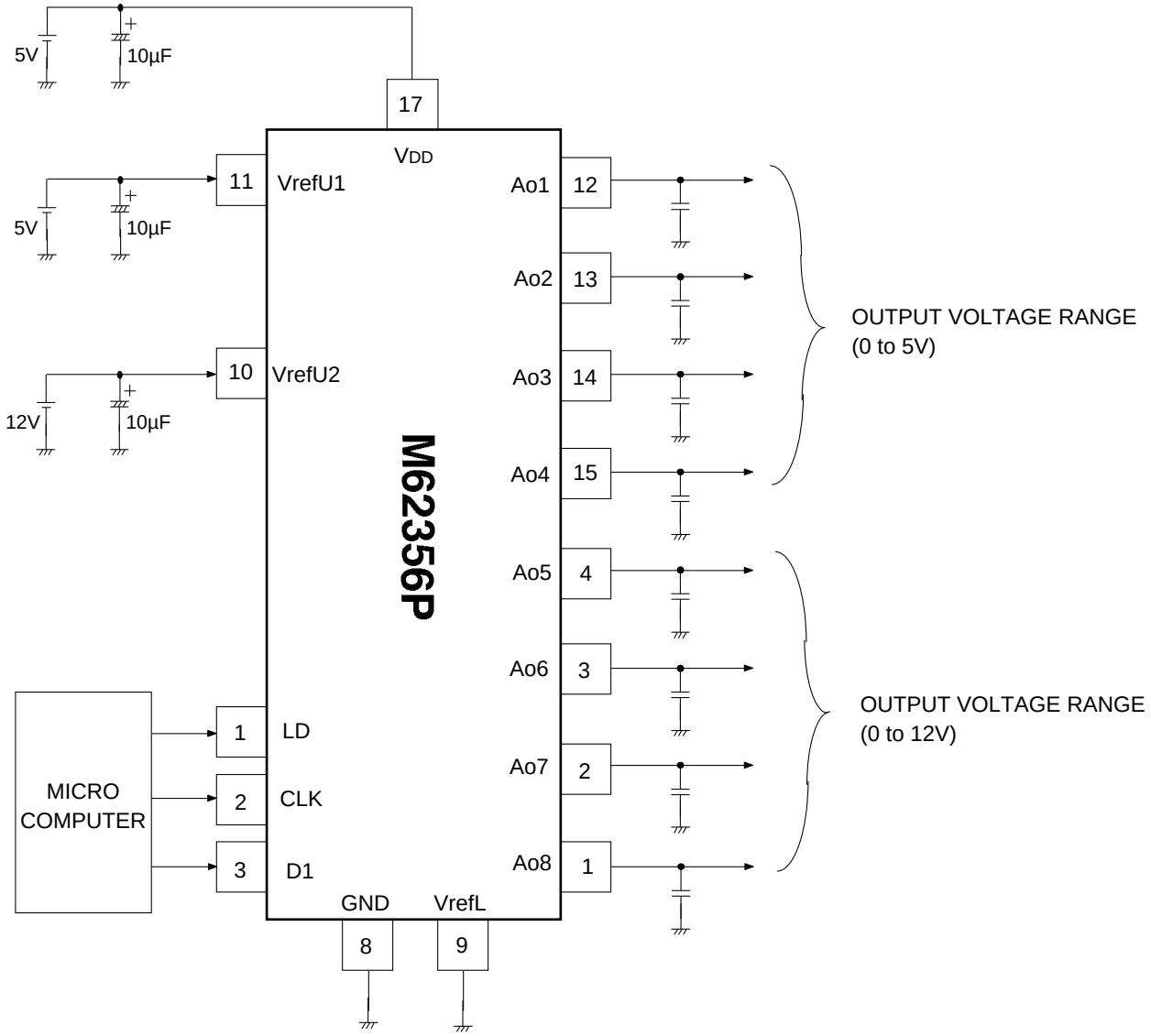
•DAC set up data

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	Output voltage
0	0	0	0	0	0	0	0	1/256•(VrefU-VrefL)+VrefL
1	0	0	0	0	0	0	0	2/256•(VrefU-VrefL)+VrefL
0	1	0	0	0	0	0	0	3/256•(VrefU-VrefL)+VrefL
1	1	0	0	0	0	0	0	4/256•(VrefU-VrefL)+VrefL
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	255/256•(VrefU-VrefL)+VrefL
1	1	1	1	1	1	1	1	256/256•(VrefU-VrefL)+VrefL

$$Ao = \frac{2^0 \times D0 + 2^1 \times D1 + 2^2 \times D2 + \cdots\cdots\cdots + 2^6 \times D6 + 2^7 \times D7 + 1}{256} \cdot (VrefU - VrefL) + VrefL$$

APPLICATION CIRCUIT



*This IC has relatively high output impedance.To reduce the influence of noise when an output line is long,connect capacitance of a few hundred picofarads to a few thousand picofarads between the output and GND.

This application circuit is connected to two reference voltages.

To use this IC with a single reference voltage,short-circuit pins (10) ,(11) ; the outputs from pins Ao1 ~ Ao8 will be controlled at an even level.

To prevent interference by noise;be sure to connect capacitance of 10µF to the power supply pin and VrefU pin.