M36D0R6040T0
M36D0R6040B0

64 Mbit (4Mb x16, Multiple Bank, Page) Flash Memory and 16 Mbit (1Mb x16) PSRAM, Multi-Chip Package

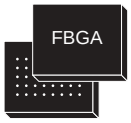
FEATURES SUMMARY

- MULTI-CHIP PACKAGE
  - 1 die of 64 Mbit (4Mb x 16) Flash Memory
  - 1 die of 16 Mbit (1Mb x 16) Pseudo SRAM
- SUPPLY VOLTAGE
  - V_{DDF} = V_{DDP} = 1.7V to 1.95V
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code (Top Flash Configuration), M36D0R6040T0: 8810h
  - Device Code (Bottom Flash Configuration), M36D0R6040B0: 8811h
- PACKAGE
  - Compliant with Lead-Free Soldering Processes
  - Lead-Free Versions

FLASH MEMORY

- PROGRAMMING TIME
  - 8µs by Word typical for Fast Factory Program
  - Double/Quadruple Word Program option
  - Enhanced Factory Program options
- MEMORY BLOCKS
  - Multiple Bank Memory Array: 4 Mbit Banks
  - Parameter Blocks (Top location)
- ASYNCHRONOUS READ
  - Asynchronous Page Read mode
  - Random Access: 70ns
- DUAL OPERATIONS
  - Program Erase in one Bank while Read in others
  - No delay between Read and Write operations
- BLOCK LOCKING
  - All blocks locked at Power-up
  - Any combination of blocks can be locked
  - $\overline{WP}_F$ for Block Lock-Down

Figure 1. Package



Stacked TFBGA67 (ZAI)
12 x 8mm

- SECURITY
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK

PSRAM

- ACCESS TIME: 70ns
- LOW STANDBY CURRENT: 110µA
- DEEP POWER DOWN CURRENT: 10µA

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SUMMARY DESCRIPTION

The M36D0R6040T0 and M36D0R6040B0 combine two memory devices in a Multi-Chip Package: a 64-Mbit, Multiple Bank Flash memory, the M58WR064FT/B, and a 16-Mbit Pseudo SRAM, the M69AR024B. Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA67 (12 x 8mm, 8x8 ball array, 0.8mm pitch) package.

In addition to the standard version, the packages are also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECOPACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive.

All packages are compliant with Lead-free soldering processes.

The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

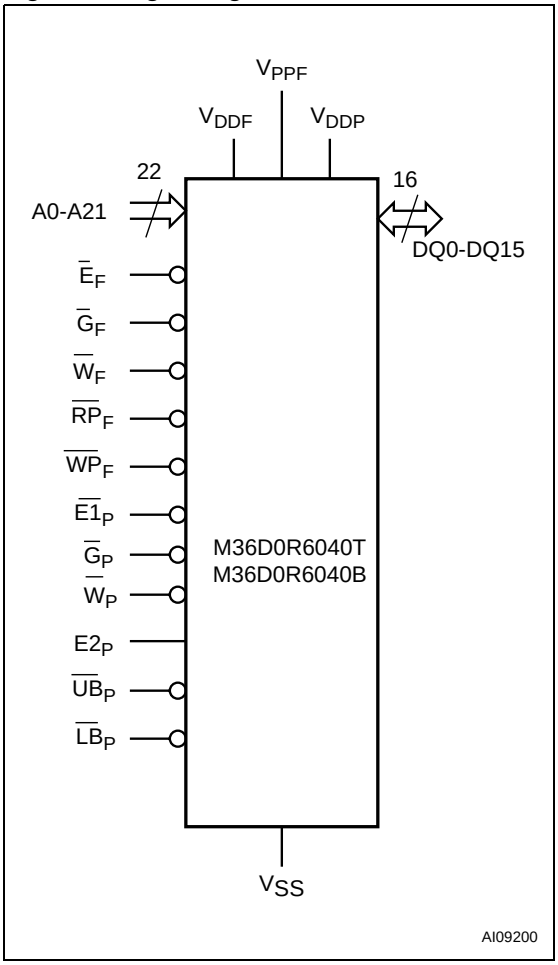
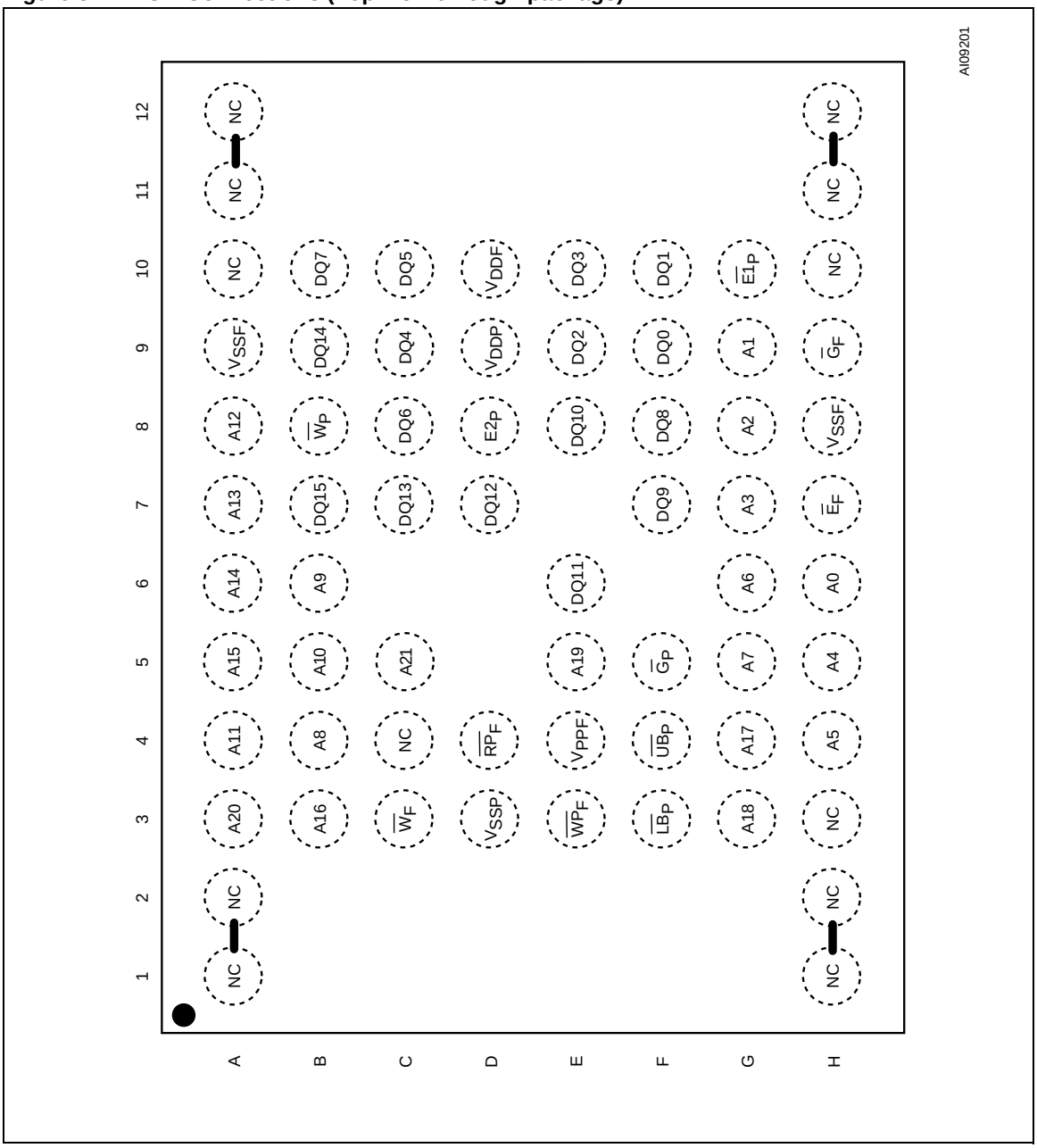


Table 1. Signal Names

A0-A19	Common Address Inputs
DQ0-DQ15	Common Data Input/Output
V_{DDF}	Flash Memory Power Supply
V_{PPF}	Common Flash Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
V_{DDP}	PSRAM Power Supply
NC	Not Connected Internally
Flash Memory Signals	
A21-A20	Address Inputs for the Flash memory only
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
PSRAM Signals	
$\overline{E1}_P$	Chip Enable input
$\overline{G}_P$	Output Enable input
$\overline{W}_P$	Write Enable input
$E2_P$	Power-down input
$\overline{UB}_P$	Upper Byte Enable input
$\overline{LB}_P$	Lower Byte Enable input

Figure 3. TFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A19). Addresses A0-A19 are common inputs for the Flash Memory and PSRAM components. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Flash memory internal state machine and they select the cells to access in the PSRAM.

The Flash memory is accessed through the Chip Enable signal ($\overline{E}_F$) and through the Write Enable (W_F) signal, while the PSRAM is accessed through two Chip Enable signals ($\overline{E1}_P$ and $E2_P$) and the Write Enable signal (W_P).

Address Inputs (A20-A21). Addresses A20-A21 are inputs for the Flash Memory component only. The Flash Memory is accessed through the Chip Enable signals ($\overline{E}_F$) and through the Write Enable (W_F) signal.

Data Input/Output (DQ0-DQ15). The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Write Bus operation.

Flash Chip Enable ($\overline{E}_F$). The Chip Enable inputs activate the memory control logics, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

Flash Output Enable ($\overline{G}_F$). The Output Enable pins control data outputs during Flash memory Bus Read operations.

Flash Write Enable ($\overline{W}_F$). The Write Enable controls the Bus Write operation of the Flash memories' Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

Flash Write Protect ($\overline{WP}_F$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (Refer to Lock Status Table in M58WR064F(T/B) datasheet).

Flash Reset ($\overline{RP}_F$). The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to Table 7., Flash Memory DC Characteristics - Currents, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to Table 8., Flash Memory DC Characteristics - Voltages).

PSRAM Chip Enable ($\overline{E1}_P$). When asserted (Low), the Chip Enable, $\overline{E1}_P$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

PSRAM Chip Enable ($E2_P$). The Chip Enable, $E2_P$, puts the device in Deep Power-down mode when it is driven Low. This is the lowest power mode.

PSRAM Output Enable ($\overline{G}_P$). The Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

PSRAM Write Enable ($\overline{W}_P$). The Write Enable, $\overline{W}_P$, controls the Bus Write operation of the memory's Command Interface.

PSRAM Upper Byte Enable ($\overline{UB}_P$). The Upper Byte Enable, $\overline{UB}_P$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

PSRAM Lower Byte Enable ($\overline{LB}_P$). The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

V_{DDF} Supply Voltage. V_{DDF} provides the power supply to the internal core of the Flash memory component. It is the main power supplies for all Flash memory operations (Read, Program and Erase).

V_{DDP} Supply Voltage. The V_{DDP} Supply Voltage supplies the power for all operations (Read or Write) and for driving the refresh logic, even when the device is not being accessed.

V_{PPF} Program Supply Voltage. V_{PPF} is both a Flash Memory control input and a Flash Memory power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDF}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLKF} gives an absolute protection against Program or Erase, while $V_{PPF} > V_{PP1F}$ enables these functions (see Tables 7 and 8, DC Characteristics for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPHF} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

V_{SS} Ground. V_{SS} is the common ground reference for all voltage measurements in the Flash (core and I/O Buffers) and PSRAM chips.

Note: Each Flash memory device in a system should have its supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Table 5., AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

FUNCTIONAL DESCRIPTION

The Flash memory and PSRAM components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E1}_P$ and $E2_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on the Flash memory and the PSRAM, which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 4. Functional Block Diagram

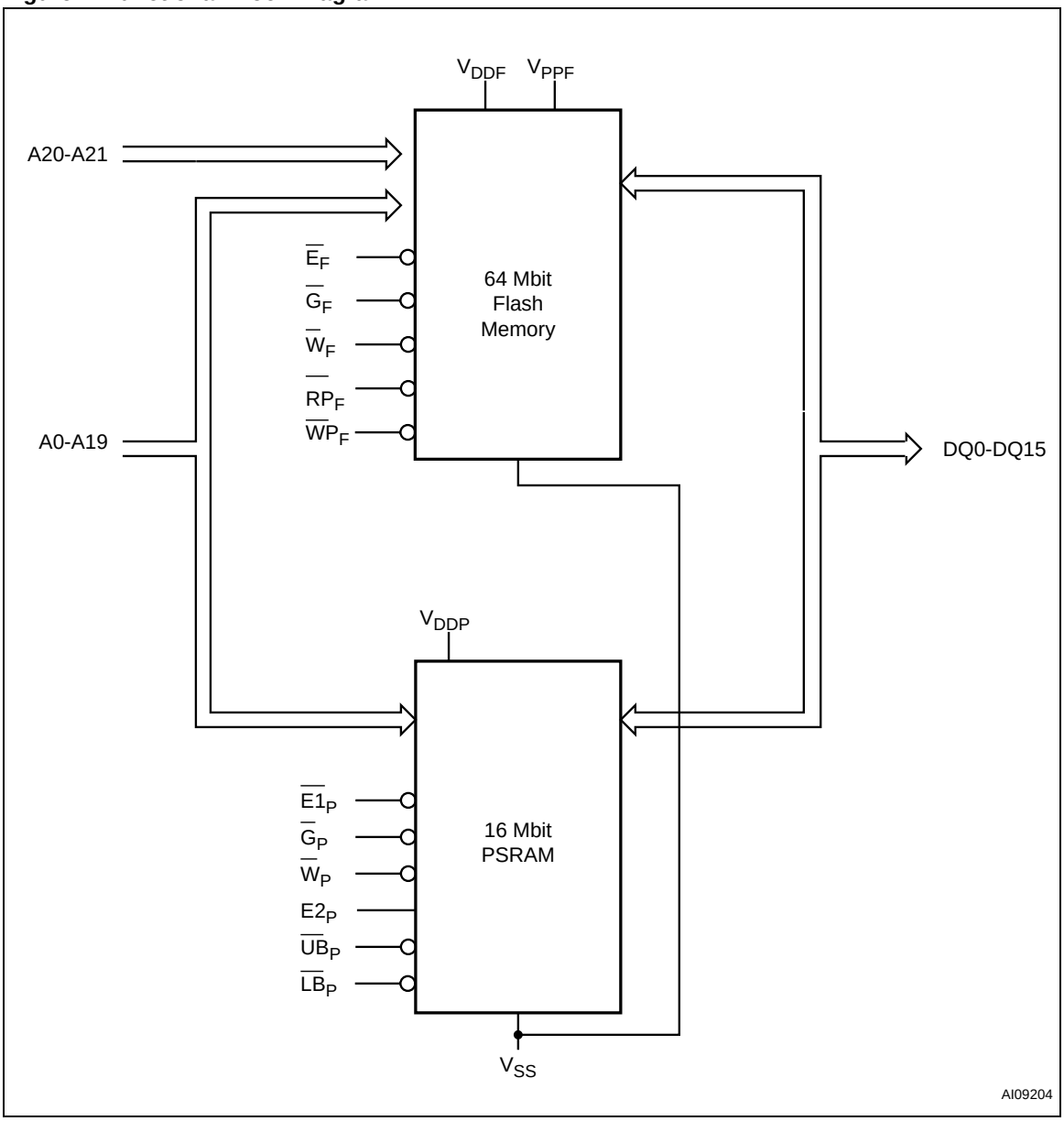


Table 2. Main Operating modes

Operation	$\overline{E}_F$	$\overline{G}_P$	$\overline{W}_P$	$\overline{L}_F$	$\overline{RP}_F$	$WAIT_F$[4]	$\overline{E1}_P$	$\overline{E2}_P$	$\overline{G}_P$	$\overline{W}_P$	$\overline{UB}_P$	$\overline{LB}_P$	DQ15-DQ0
Flash Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}[2]	V_{IH}		PSRAM must be disabled						Flash Data Out
Flash Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}[2]	V_{IH}								Flash Data In
Flash Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}								Flash Data Out or Hi-Z [3]
Flash Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}		Any PSRAM mode is allowed						Flash Hi-Z
Flash Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z							Flash Hi-Z
Flash Reset	X	X	X	X	V_{IL}	Hi-Z							Flash Hi-Z
PSRAM Read	Flash Memory must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	PSRAM data out
PSRAM Write							V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	PSRAM data in
Output Disable	Any Flash mode is allowed.						V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	PSRAM Hi-Z
PSRAM Standby							V_{IH}	V_{IH}	X	X	X	X	PSRAM Hi-Z
PSRAM Deep Power-Down							X	V_{IL}	X	X	X	X	PSRAM Hi-Z

Note: 1. X = Don't care.
2. L_F can be tied to V_{IH} if the valid address has been previously latched.
3. Depends on $\overline{G}_F$.
4. WAIT signal polarity is configured using the Set Configuration Register command. Refer to M58WR064F(T/B) datasheet for details.

FLASH MEMORY COMPONENT

The M36D0R6040T0 and M36D0R6040B0 contain a 64Mbit Flash memory, the M58WR064F(T/B). The burst mode of this device is not available in the M36D0R6040(T/B).

For detailed information on how to use the Flash memory, see the M58WR064F(T/B) datasheet which is available from your local STMicroelectronics distributor.

PSRAM COMPONENT

The M36D0R6040T0 and M36D0R6040B0 contain a 16Mbit PSRAM. For detailed information on how to use it, see the M69AR024B datasheet which is available from the internet site *http://www.st.com* or from your local STMicroelectronics distributor.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–30	85	°C
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–65	155	°C
T_{LEAD}	Lead Temperature during Soldering		(1)	°C
V_{IO}	Input or Output Voltage	–0.5	V_{DD}(1)+0.6	V
V_{DDF}	Flash Memory Core Supply Voltage	–0.2	2.45	V
V_{DDP}	PSRAM Supply Voltage	–0.2	3.3	V
V_{PPF}	Flash Memory Program Voltage	–0.2	14	V
I_O	Output Short Circuit Current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

Note: 1. $V_{DDF} = V_{DDP} = V_{DD}$.
2. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

DC AND AC PARAMETERS

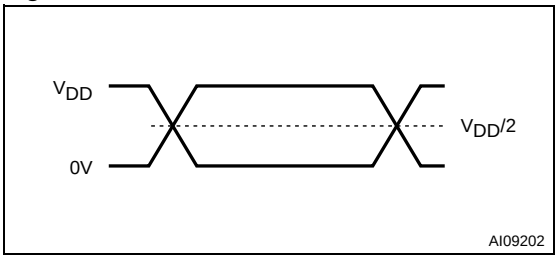
This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	Flash Memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	1.7	1.95	–	–	V
V_{DDP} Supply Voltage	–	–	1.7	1.95	V
V_{PPF} Supply Voltage (Factory environment)	11.4	12.6	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDF} +0.4	–	–	V
Ambient Operating Temperature	–40	85	–30	85	°C
Load Capacitance (C_L)	30		50		pF
Input Rise and Fall Times		5			ns
Input Pulse Voltages(1)	0 to V_{DD}		0 to V_{DD}		V
Input and Output Timing Ref. Voltages(1)	$V_{DD}/2$		$V_{DD}/2$		V

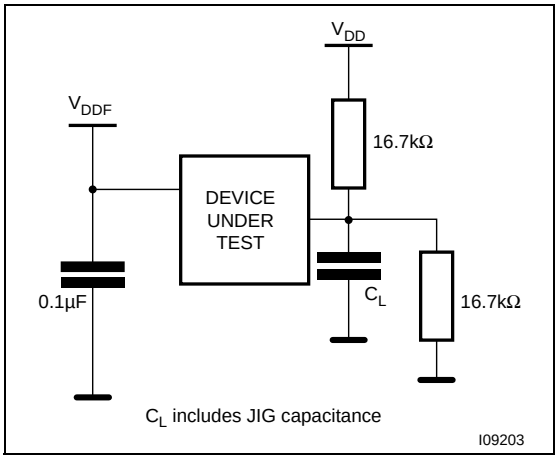
Note: 1. $V_{DDF} = V_{DDP} = V_{DD}$.

Figure 5. AC Measurement I/O Waveform



Note: $V_{DDF} = V_{DDP} = V_{DD}$.

Table 5. AC Measurement Load Circuit



Note: $V_{DDF} = V_{DDP} = V_{DD}$.

Table 6. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		15	pF

Note: Sampled only, not 100% tested.

Table 7. Flash Memory DC Characteristics - Currents

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDF}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDF}$			±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=6MHz)	$\overline{E}_F = V_{IL}$, $\overline{G}_F = V_{IH}$		3	6	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP}_F = V_{SSF} \pm 0.2V$		10	50	µA
I_{DD3}	Supply Current (Standby)	$\overline{E}_F = V_{DDF} \pm 0.2V$		10	50	µA
I_{DD4}	Supply Current (Automatic Standby)	$\overline{E}_F = V_{IL}$, $\overline{G}_F = V_{IH}$		10	50	µA
I_{DD5} (1)	Supply Current (Program)	$V_{PPF} = V_{PPH}$		8	15	mA
		$V_{PPF} = V_{DDF}$		10	20	mA
	Supply Current (Erase)	$V_{PPF} = V_{PPH}$		8	15	mA
		$V_{PPF} = V_{DDF}$		10	20	mA
I_{DD6} (1,2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank		13	26	mA
I_{DD7}(1)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E}_F = V_{DDF} \pm 0.2V$		10	50	µA
I_{PP1}(1)	V_{PPF} Supply Current (Program)	$V_{PPF} = V_{PPH}$		2	5	mA
		$V_{PPF} = V_{DDF}$		0.2	5	µA
	V_{PPF} Supply Current (Erase)	$V_{PPF} = V_{PPH}$		2	5	mA
		$V_{PPF} = V_{DDF}$		0.2	5	µA
I_{PP2}	V_{PPF} Supply Current (Read)	$V_{PPF} \le V_{DDF}$		0.2	5	µA
I_{PP3}(1)	V_{PPF} Supply Current (Standby)	$V_{PPF} \le V_{DDF}$		0.2	5	µA

Note: 1. Sampled only, not 100% tested.
2. V_{DDF} Dual Operation current is the sum of read and program or erase currents.

Table 8. Flash Memory DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.5		0.4	V
V_{IH}	Input High Voltage		V_{DDF} –0.4		V_{DDF} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDF} –0.1			V
V_{PP1}	V_{PPF} Program Voltage-Logic	Program, Erase	1	1.8	3.3	V
V_{PPH}	V_{PPF} Program Voltage Factory	Program, Erase	11.4	12	12.6	V
V_{PPLK}	Program or Erase Lockout				0.4	V
V_{LKO}	V_{DDF} Lock Voltage		1			V
V_{RPH}	$\overline{RP}_F$ pin Extended High Voltage				3.3	V

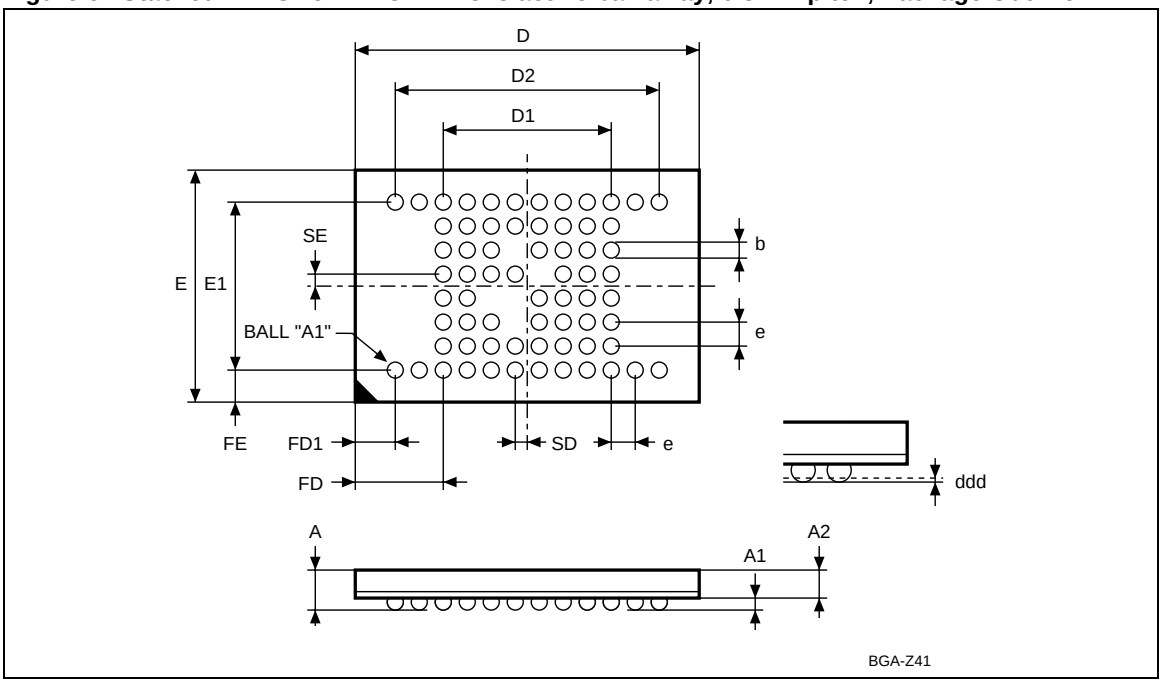
Table 9. PSRAM DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{CC1}	V_{CC} Active Current	V_{DDP} = 1.95V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1}_P = V_{IL}$ and $E2_P = V_{IH}$, I_{OUT} = 0mA	t_{AVAV} Read / t_{AVAV} Write = minimum		20	mA
I_{CC2}			t_{AVAV} Read / t_{AVAV} Write = maximum		3	mA
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDP}$		–1	1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDP}$		–1	1	µA
I_{PD}	Deep Power Down Current	V_{DDP} = 1.95V, $\overline{E1}_P \ge V_{DDP} - 0.2V$ or $\overline{E1}_P \le V_{IL}$, $V_{IN} \ge V_{DDP} - 0.2V$ or $V_{IN} \le 0.2V$			10	µA
I_{SB}	Standby Supply Current CMOS	V_{DDP} = 1.95V, $\overline{E1}_P = E2_P \ge V_{DDP} - 0.2V$, I_{OUT} = 0mA			110	µA
V_{IH} (1)	Input High Voltage			$0.8V_{DDP}$	V_{DDP} + 0.2	V
V_{IL} (2)	Input Low Voltage			–0.3	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.5mA		$V_{DDP} - 0.2$		V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.2	V

Note: 1. The maximum DC voltage on input and I/O pins is V_{DDP}+0.2V. During voltage transitions, inputs may overshoot V_{DDP} by 1.0V for periods of up to 5ns.
2. The minimum DC voltage on input or I/O pins is –0.3V. During voltage transitions, inputs may undershoot V_{SS} by 1.0V for periods of up to 5ns.

PACKAGE MECHANICAL

Figure 6. Stacked TFBGA67 12x8mm - 8x8 active ball array, 0.8mm pitch, Package Outline



Note: Drawing is not to scale.

Table 10. Stacked TFBGA67 12x8mm - 8x8 ball array, 0.8mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
Symbol	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.810			0.0319		
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	12.000	11.900	12.100	0.4724	0.4685	0.4764
D1	5.600	–	–	0.2205	–	–
D2	8.800	–	–	0.3465	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.600	–	–	0.2205	–	–
e	0.800	–	–	0.0315	–	–
FD	3.200	–	–	0.1260	–	–
FD1	1.600	–	–	0.0630	–	–
FE	1.200	–	–	0.0472	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M36 D 0 R 6 0 4 0 T 0 ZAI T

Device Type
M36 = Multi-Chip Package (Flash + RAM)

Flash 1 Architecture
D = Multiple Bank, Page mode

Flash 2 Architecture
0 = none present

Operating Voltage
R = V_{DDF} = V_{DDP} = 1.7V to 1.95V

Flash 1 Density
6 = 64 Mbit

Flash 2 Density
0 = none present

RAM 1 Density
4 = 16 Mbit

RAM 0 Density
0 = none present

Parameter Blocks Location
T = Top Boot Block Flash
B = Bottom Boot Block Flash

Product Version
0 = 0.13µm Flash technology, 70ns;
0.18µm RAM, 70ns speed

Package
ZAI = Stacked TFBGA67 12 x 8mm - 8x8 active ball array, 0.8mm pitch

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-Free and RoHS Package, Standard Packing
F = Lead-Free and RoHS Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to ’1’. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST-Microelectronics Sales Office nearest to you.

REVISION HISTORY

Table 12. Document Revision History

Date	Version	Revision Details
26-Nov-2003	1.0	First Issue
07-Dec-2003	2.0	Document status promoted from Target Specification to full Datasheet. TFBGA67 package fully compliant with the ST ECOPACK specification. Flash memory and PSRAM data updated to the revision 5.0 of the M58WR064F(T/B) datasheet and to the revision 6.0 of the M69AR024B datasheet.