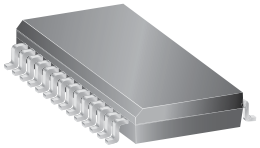
DABiC-IV 20-Bit Serial-Input Latched Source Driver

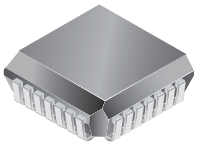
Features and Benefits

- Controlled output slew rate
- High-speed data storage
- 60 V minimum output break down
- High data-input rate
- PNP active pull-downs
- Low output-saturation voltages
- Low-power CMOS logic and latches
- Improved replacements for TL5812x, UCN5812x, and UCQ5812x

Package:



28-pin SOICW
(Package LW)



28-pin PLCC
(EP package)

Not to scale

Description

The A6812 device combines a 20-bit CMOS shift register, accompanying data latches and control circuitry with bipolar sourcing outputs ,and PNP active pull-downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The A6812 features an increased data-input rate (compared with the older UCN/UCQ5812-F) and a controlled output slew rate.

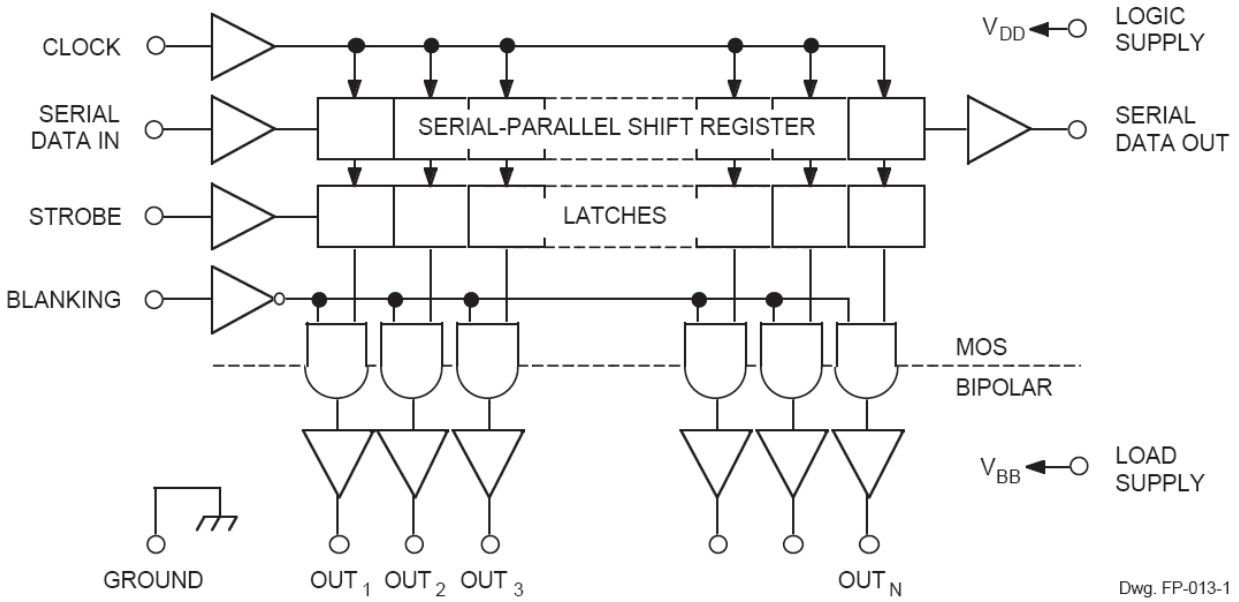
The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 or 5 V logic supply, they operate to at least 10 MHz.

A CMOS serial data output permits cascaded connections in applications requiring additional drive lines. Similar devices are available as the A6810 (10-bit) and A6818 (32-bit).

The A6812 output source drivers are NPN Darlingtons, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and/or microprocessors and to meet government emissions

Continued on the next page…

Functional Block Diagram



Description (continued)

regulations. For inter-digit blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The PNP active pull-downs sink at least 2.5 mA.

Three temperature ranges are available for optimum performance in commercial (suffix S-), industrial (suffix E-), or automotive (suffix K-) applications. Package styles are provided for surface-mount SOIC (suffix -LW), or minimum-area surface-mount PLCC (suffix -EP). Copper lead frames, low logic-power dissipation, and low output-saturation voltages allow these drivers to source 25 mA from all outputs continuously to more than 43°C (suffix -LW) or 61°C (suffix -EP).

Each package is available in a lead (Pb) free version, with 100% matte tin leadframe plating.

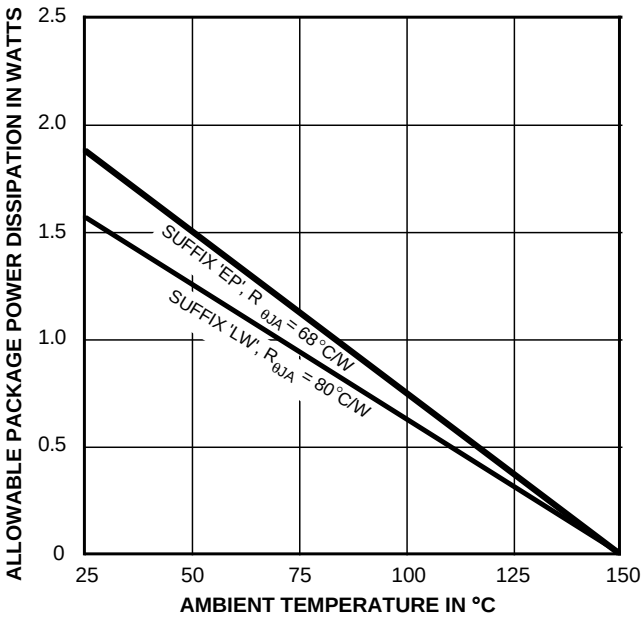
Selection Guide

Part Number	Pb-free	Packing	Package	Ambient Temperature, T_A (°C)
A6812EEP-T	Yes	38 pieces/tube	PLCC	–40 to 85
A6812EEPTR	–	800 pieces/13-in. reel		
A6812EEPTR-T	Yes			
A6812ELW-T	Yes	27 pieces/tube	SOIC-W	
A6812ELWTR	–	1000 pieces/13-in. reel		
A6812ELWTR-T	Yes			
A6812KLW-T	Yes	27 pieces/tube	SOIC-W	–40 to 125
A6812KLWTR	–	1000 pieces/13-in. reel		
A6812KLWTR-T	Yes			
A6812SEP-T	Yes	38 pieces/tube	PLCC	–20 to 85
A6812SEPTR	–	800 pieces/13-in. reel		
A6812SEPTR-T	Yes			
A6812SLW-T	Yes	27 pieces/tube	SOIC-W	
A6812SLWTR-T	Yes	1000 pieces/13-in. reel		

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	V_{DD}		7	V
Driver Supply Voltage	V_{BB}		60	V
Input Voltage Range	V_{IN}		–0.3 to V_{DD} + 0.3	V
Continuous Output Current Range	I_{OUT}		–40 to 15	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range K	–40 to 125	°C
		Range S	–20 to 85	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–65 to 125	°C

*Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.



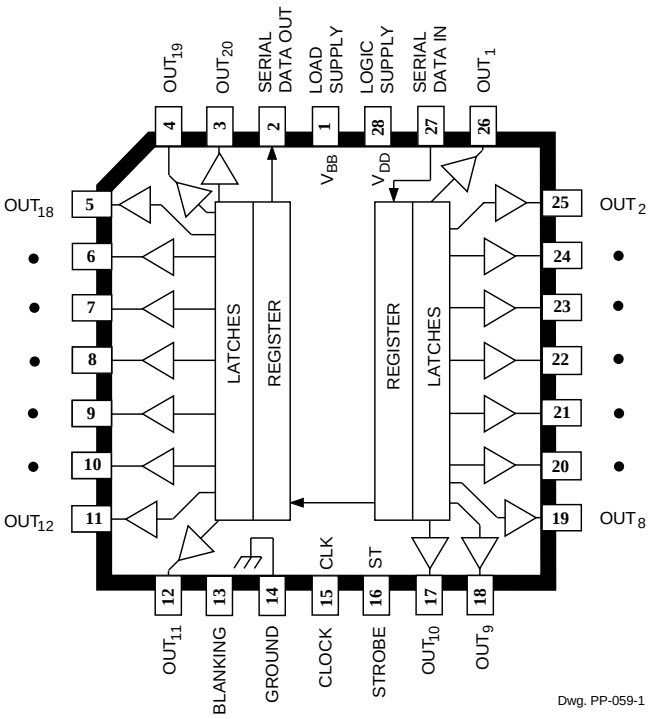
Dwg. GP-024-2

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package EP, 1-layer PCB with solder limited to mounting pads	68	°C/W
		Package LW, 1-layer PCB with solder limited to mounting pads	80	°C/W

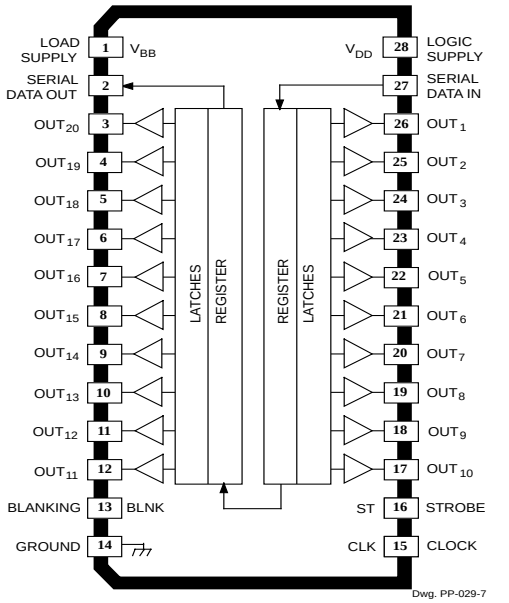
*Additional thermal information available on the Allegro website

EP Package



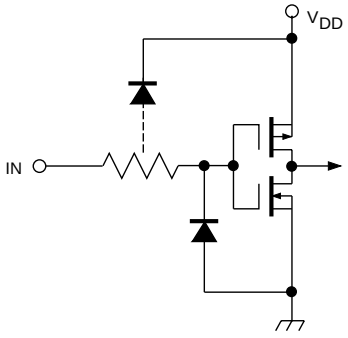
Dwg. PP-059-1

LW Package



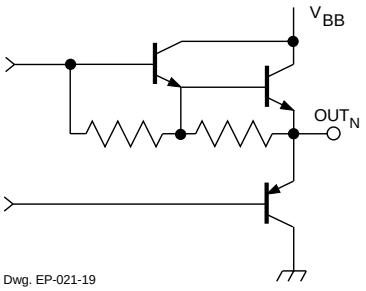
Dwg. PP-029-7

TYPICAL INPUT CIRCUIT



Dwg. EP-010-5

TYPICAL OUTPUT DRIVER



Dwg. EP-021-19

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	
I_N	⌐¬																					
H	⌐¬	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	¬⌐	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X		R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

ELECTRICAL CHARACTERISTICS at T_A = +25°C (A6812S-) or over operating temperature range (A6812E- or A6812K-), V_{BB} = 60 V; unless otherwise noted

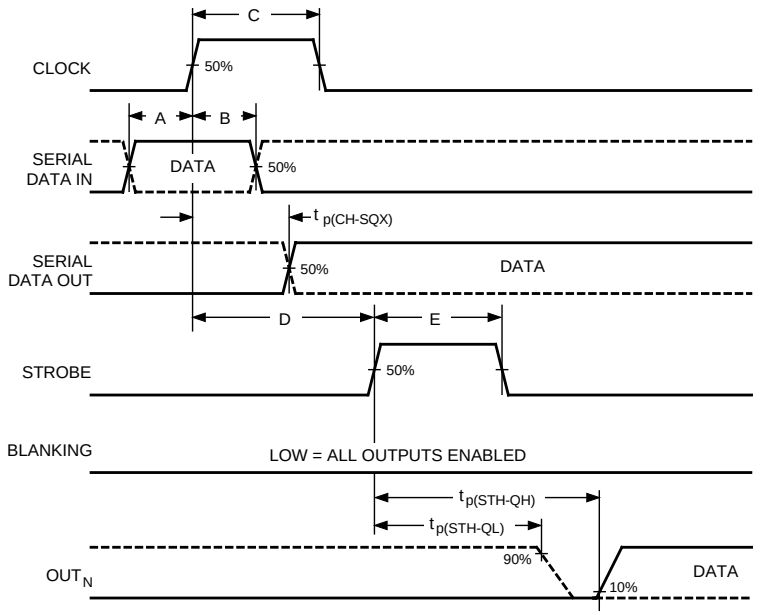
Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 3.3 V			Limits @ V_{DD} = 5 V			Units
			Mln.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V	—	<-0.1	-15	—	<-0.1	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA	57.5	58.3	—	57.5	58.3	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	$V_{IN(1)}$		2.2	—	—	3.3	—	—	V
	$V_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	<0.01	1.0	—	<0.01	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	<-0.01	-1.0	—	<-0.01	-1.0	µA
Input Clamp Voltage	V_{IK}	I_{IN} = -200 µA	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	2.8	3.05	—	4.5	4.75	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	f_c		10*	—	—	10*	—	—	MHz
Logic Supply Current	$I_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	$I_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	$I_{BB(1)}$	All Outputs High, No Load	—	3.0	6.0	—	3.0	6.0	mA
	$I_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	µA
Blanking-to-Output Delay	$t_{dis(BQ)}$	C_L = 30 pF, 50% to 50%	—	0.7	2.0	—	0.7	2.0	µs
	$t_{en(BQ)}$	C_L = 30 pF, 50% to 50%	—	1.8	3.0	—	1.8	3.0	µs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	R_L = 2.3 kΩ, C_L 30 pF	—	0.7	2.0	—	0.7	2.0	µs
	$t_{p(STH-QH)}$	R_L = 2.3 kΩ, C_L 30 pF	—	1.8	3.0	—	1.8	3.0	µs
Output Fall Time	t_f	R_L = 2.3 kΩ, C_L 30 pF	2.4	—	12	2.4	—	12	µs
Output Rise Time	t_r	R_L = 2.3 kΩ, C_L 30 pF	2.4	—	12	2.4	—	12	µs
Output Slew Rate	dV/dt	R_L = 2.3 kΩ, C_L 30 pF	4.0	—	20	4.0	—	20	V/µs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	I_{OUT} = ±200 µA	—	50	—	—	50	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

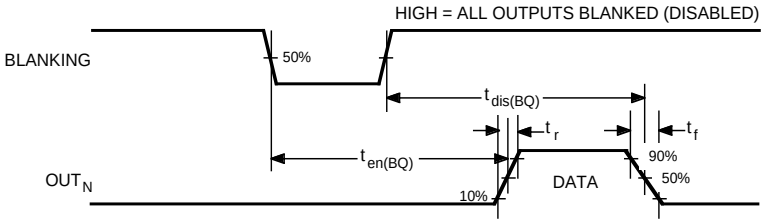
Typical data is is for design information only and is at T_A = +25°C.

* Operation at a clock frequency greater than the specified minimum is possible but not warranteed.

TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)



Dwg. WP-029



Dwg. WP-030A

A. Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ ..... **25 ns**
B. Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ ..... **25 ns**
C. Clock Pulse Width, $t_{w(CH)}$ ..... **50 ns**
D. Time Between Clock Activation and Strobe, $t_{su(C)}$ ..... **100 ns**
E. Strobe Pulse Width, $t_{w(STH)}$ ..... **50 ns**

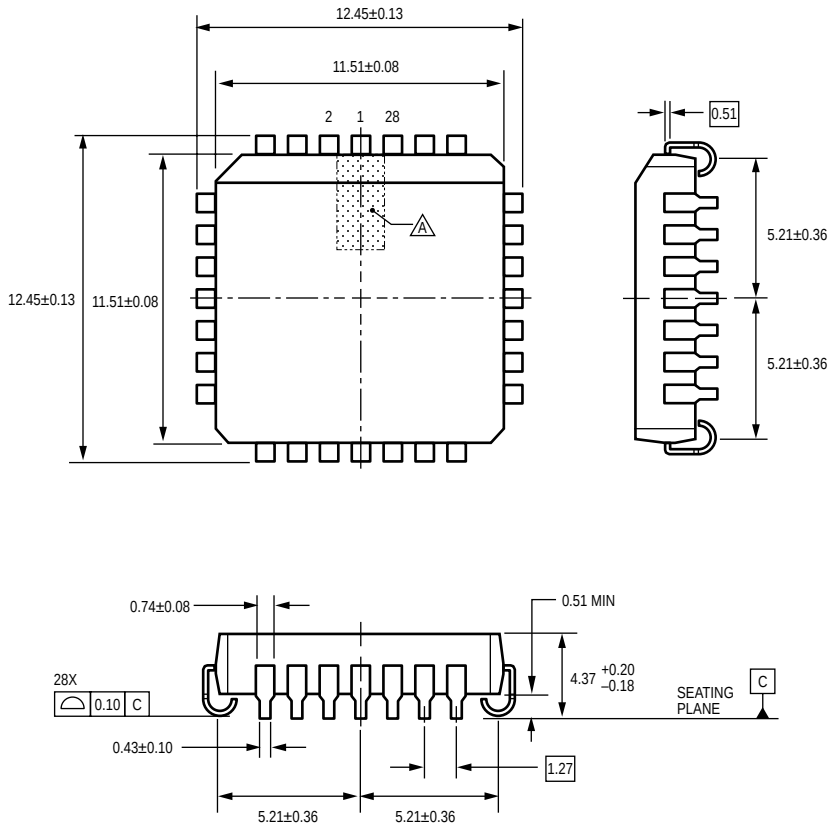
NOTE – Timing is representative of a 10 MHz clock. Higher speeds may be attainable with increased supply voltage; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

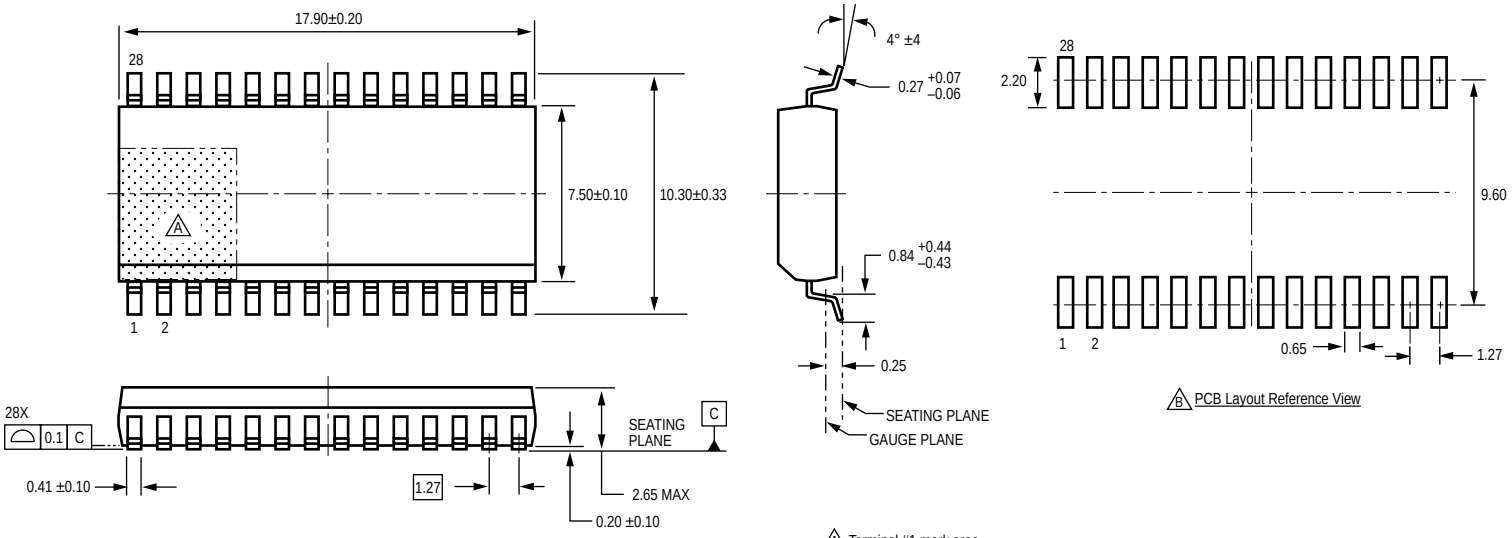
When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

EP Package, 28-Pin PLCC



For Reference Only
(reference JEDEC MS-018 AB)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

LW Package, 28-Pin SOICW



For Reference Only
(Reference JEDEC MS-013 AE)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-28M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

For the latest version of this document, visit our website:
www.allegromicro.com