

SONY

CXK58257AP/ASP/AM -70L/10L/12L
-70LL/10LL/12LL *

32768-word × 8-bit High Speed CMOS Static RAM

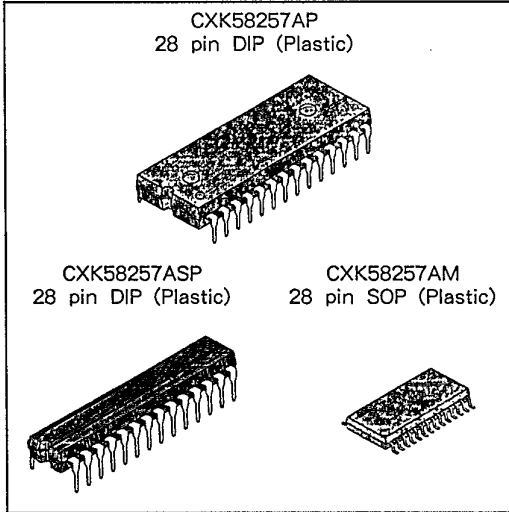
Description

CXK58257AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

* 300mil DIP covers only L-version.

Features

- Fast access time : (Access time)
CXK58257AP/ASP/AM-70L, 70LL 70ns(Max.)
CXK58257AP/ASP/AM-10L, 10LL 100ns(Max.)
CXK58257AP/ASP/AM-12L, 12LL 120ns(Max.)
- Low power operation :
CXK58257AP/AM-70LL, 10LL, 12LL ;
Standby : 1 μW (Typ.)
Operation : 15mW (Typ.)
CXK58257AP/ASP/AM-70L, 10L, 12L ;
Standby : 2.5 μW (Typ.)
Operation : 15mW (Typ.)
- Single +5V supply : +5V ± 10 %
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output :
three state output
- Directly TTL compatible :
All inputs and outputs



- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

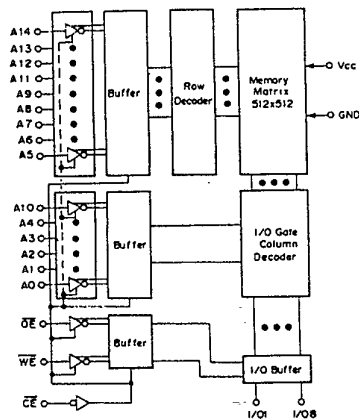
Function

32768-word × 8-bit static RAM

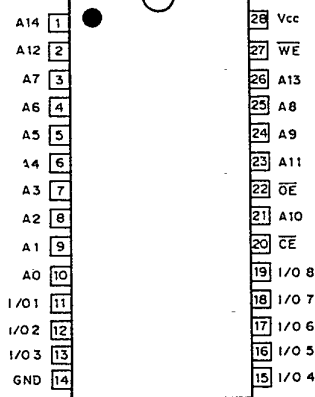
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

| Symbol | Description |
|--------------|---------------------|
| A0 to A14 | Address input |
| I/O1 to I/O8 | Data input/output |
| CE | Chip enable input |
| WE | Write enable input |
| OE | Output enable input |
| Vcc | + 5V power supply |
| GND | Ground |

E90447B46 - ST

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

| Item | Symbol | Rating | Unit |
|-----------------------------|---------------------|---------------------------------|----------|
| Supply voltage | V _{CC} | - 0.5 to + 7.0 | V |
| Input voltage | V _{IN} | - 0.5* to V _{CC} + 0.5 | V |
| Input and output voltage | V _{I/O} | - 0.5* to V _{CC} + 0.5 | V |
| Allowable power dissipation | P _D | CXK58257AP/ASP | 1.0 |
| | | CXK58257AM | 0.7 |
| Operating temperature | T _{opr} | 0 to + 70 | °C |
| Storage temperature | T _{stg} | - 55 to + 150 | °C |
| Soldering temperature | T _{solder} | 260 • 10 | °C • sec |

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

| \overline{CE} | \overline{OE} | \overline{WE} | Mode | I/O1 to I/O8 | V _{CC} Current |
|-----------------|-----------------|-----------------|----------------|--------------|-------------------------------------|
| H | x | x | Not selected | High Z | I _{SB1} , I _{SB2} |
| L | H | H | Output disable | High Z | I _{CC1} , I _{CC2} |
| L | L | H | Read | Data out | I _{CC1} , I _{CC2} |
| L | x | L | Write | Data in | I _{CC1} , I _{CC2} |

x : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70 °C, GND = 0V)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|--------------------|-----------------|--------|------|-----------------------|------|
| Supply voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Input high voltage | V _{IH} | 2.2 | — | V _{CC} + 0.3 | V |
| Input low voltage | V _{IL} | - 0.3* | — | 0.8 | V |

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

| Item | Symbol | Test conditions | - 70L/10L/12L | | | - 70LL/10LL/12LL | | | Unit | |
|--------------------------------|------------------|---|---------------|-------|------|------------------|-------|------|------|----|
| | | | Min. | Typ.* | Max. | Min. | Typ.* | Max. | | |
| Input leakage current | I _{LI} | V _{IN} = GND to V _{CC} | - 0.5 | — | 0.5 | - 0.5 | — | 0.5 | μA | |
| Output leakage current | I _{LO} | $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ V _{I/O} = GND to V _{CC} | - 0.5 | — | 0.5 | - 0.5 | — | 0.5 | μA | |
| Operating power supply current | I _{CC1} | $\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA | — | 3 | 10 | — | 3 | 10 | mA | |
| | | $\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC} - 0.2V$ | — | 1 | 5 | — | 1 | 5 | | |
| Average operating current | I _{CC2} | Cycle = Min, Duty = 100%, I _{OUT} = 0mA | 70L/70LL | — | 30 | 50 | — | 30 | 50 | mA |
| | | | 10L/10LL | — | 23 | 50 | — | 23 | 50 | |
| | | | 12L/12LL | — | 20 | 50 | — | 20 | 50 | |
| Standby current | I _{SB1} | $\overline{CE} \geq V_{CC} - 0.2V$ | 0 to 70°C | — | — | 25 | — | — | 5 | μA |
| | | | 0 to 40°C | — | — | 5 | — | — | 1 | |
| | | | 25°C | — | 0.5 | 2 | — | 0.2 | 0.5 | |
| | I _{SB2} | $\overline{CE} = V_{IH}$ | — | 0.4 | 2 | — | 0.4 | 2 | mA | |
| Output high voltage | V _{OH} | I _{OH} = - 1.0mA | 2.4 | — | — | 2.4 | — | — | V | |
| Output low voltage | V _{OL} | I _{OL} = 2.1mA | — | — | 0.4 | — | — | 0.4 | V | |

* V_{CC} = 5V, Ta = 25°C

I/O capacitance

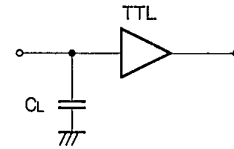
(Ta = 25°C, f = 1MHz)

| Item | Symbol | Test conditions | Min. | Max. | Unit |
|-------------------|------------------|-----------------------|------|------|------|
| Input capacitance | C _{IN} | V _{IN} = 0V | — | 6 | pF |
| I/O capacitance | C _{I/O} | V _{I/O} = 0V | — | 8 | pF |

Note) This parameter is sampled and is not 100% tested.

AC characteristics**● AC test conditions** $(V_{CC} = 5V \pm 10\%, T_a = 0 \text{ to } +70^\circ\text{C})$

| Item | Conditions | |
|----------------------------------|-------------------|-----------------------|
| Input pulse high level | $V_{IH} = 2.2V$ | |
| Input pulse low level | $V_{IL} = 0.8V$ | |
| Input rise time | $t_r = 5ns$ | |
| Input fall time | $t_f = 5ns$ | |
| Input and output reference level | 1.5V | |
| Output load conditions | 10L/10LL/12L/12LL | $C_L^* = 100pF, 1TTL$ |
| | 70L/70LL | $C_L^* = 30pF, 1TTL$ |

* C_L includes scope and jig capacitances.

• Read cycle

| Item | Symbol | -70L/70LL | | -10L/10LL | | -12L/12LL | | Unit |
|--|--------------------|-----------|------|-----------|------|-----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read cycle time | t _{RC} | 70 | — | 100 | — | 120 | — | ns |
| Address access time | t _{AA} | — | 70 | — | 100 | — | 120 | ns |
| Chip enable access time | t _{CO} | — | 70 | — | 100 | — | 120 | ns |
| Output enable to output valid | t _{OE} | — | 35 | — | 50 | — | 60 | ns |
| Output hold from address change | t _{OH} | 20 | — | 20 | — | 20 | — | ns |
| Chip enable to output in low Z (\overline{CE}) | t _{LZ} | 10 | — | 10 | — | 10 | — | ns |
| Output enable to output in low Z (\overline{OE}) | t _{OLZ} | 5 | — | 5 | — | 5 | — | ns |
| Chip disable to output in high Z (\overline{CE}) | t _{HZ} * | 0 | 30 | 0 | 30 | 0 | 30 | ns |
| Chip disable to output in high Z (\overline{OE}) | t _{OHZ} * | 0 | 30 | 0 | 30 | 0 | 30 | ns |

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

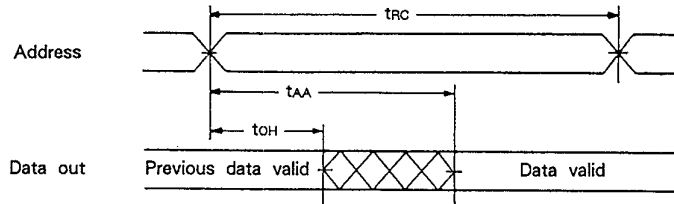
• Write cycle

| Item | Symbol | -70L/70LL | | -10L/10LL | | -12L/12LL | | Unit |
|---|--------------------|-----------|------|-----------|------|-----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write cycle time | t _{WC} | 70 | — | 100 | — | 120 | — | ns |
| Address valid to end of write | t _{AW} | 65 | — | 80 | — | 100 | — | ns |
| Chip enable to end of write | t _{CW} | 65 | — | 80 | — | 100 | — | ns |
| Data to write time overlap | t _{DW} | 30 | — | 35 | — | 40 | — | ns |
| Data hold from write time | t _{DH} | 0 | — | 0 | — | 0 | — | ns |
| Write pulse width | t _{WP} | 50 | — | 60 | — | 70 | — | ns |
| Address setup time | t _{AS} | 0 | — | 0 | — | 0 | — | ns |
| Write recovery time (\overline{WE}) | t _{WR} | 0 | — | 0 | — | 0 | — | ns |
| Write recovery time (\overline{CE}) | t _{WR1} | 0 | — | 0 | — | 0 | — | ns |
| Output active from end of write | t _{OW} | 10 | — | 10 | — | 10 | — | ns |
| Write to output in high Z | t _{WHZ} * | 0 | 25 | 0 | 25 | 0 | 25 | ns |

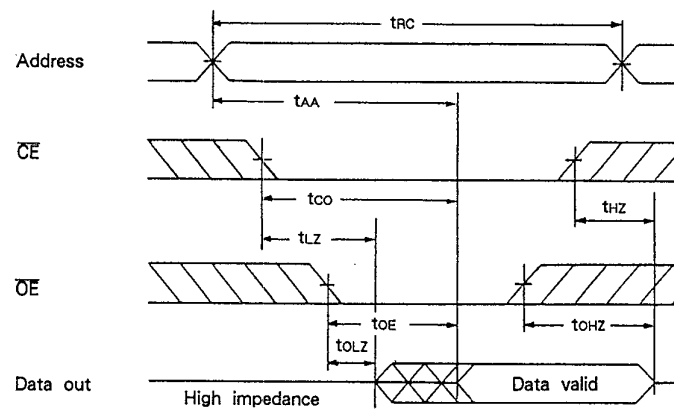
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

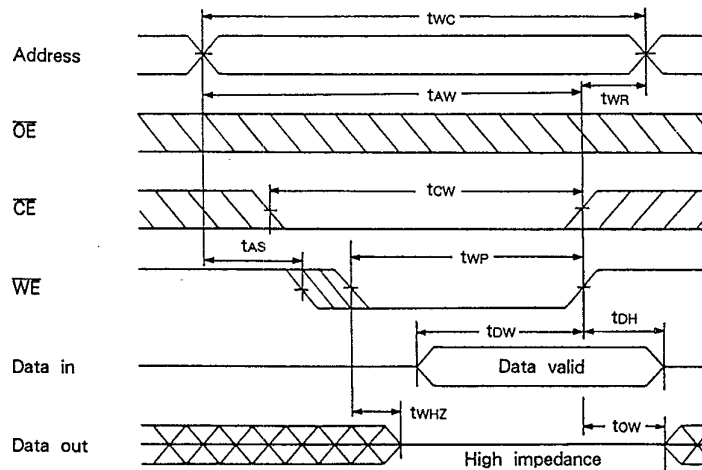
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



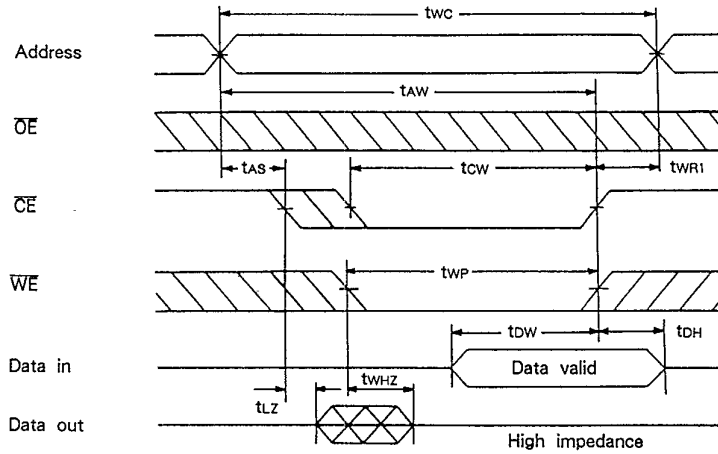
- Read cycle (2) : $\overline{WE} = V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

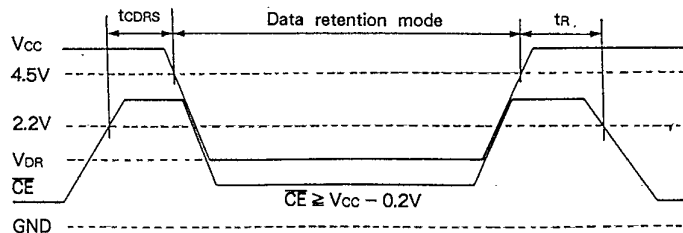
Data Retention Characteristics

($T_a = 0$ to 70°C)

| Item | Symbol | Test conditions | -70L/10L/12L | | | -70LL/10LL/12LL | | | Unit | |
|---------------------------|-------------|--|---------------------------------|------|------|-----------------|------|------|---------------|---------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Data retention voltage | V_{DR} | $\overline{CE} \geq V_{CC} - 0.2V$ | 2.0 | — | 5.5 | 2.0 | — | 5.5 | V | |
| Data retention current | I_{CCDR1} | $V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$ | $T_a = 0$ to 70°C | — | — | 10 | — | — | 3 | μA |
| | | | $T_a = 0$ to 40°C | — | — | 2 | — | — | 0.6 | |
| | | | 25°C | — | 0.25 | 1 | — | 0.1 | 0.3 | |
| | I_{CCDR2} | $V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \geq V_{CC} - 0.2V$ | — | 0.5 | 25 | — | 0.2 | 5 | μA | |
| Data retention setup time | t_{CDRS} | Chip disable to data retention mode | 0 | — | — | 0 | — | — | ns | |
| Recovery time | t_R | | t_{RC}^* | — | — | t_{RC}^* | — | — | ns | |

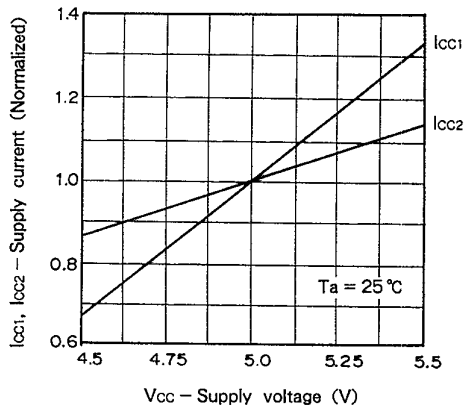
* t_{RC} : Read cycle time

Data retention waveform

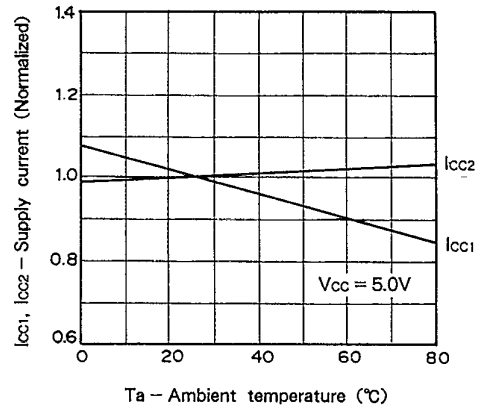


Example of Representative Characteristics

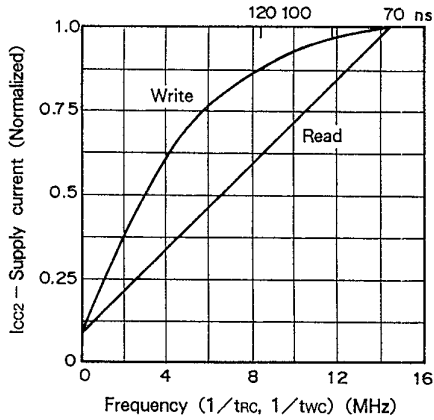
Supply current vs. Supply voltage



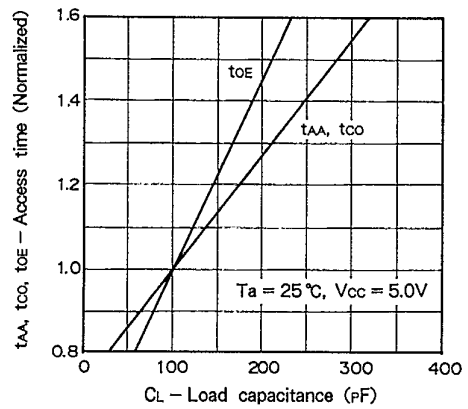
Supply current vs. Ambient temperature



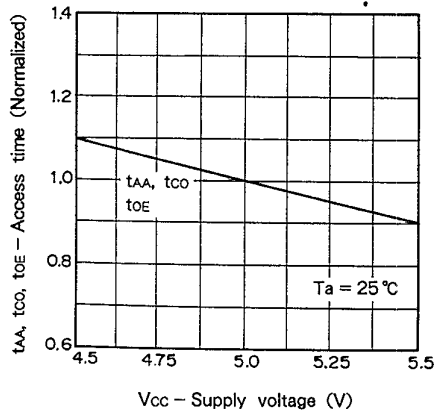
Supply current vs. Frequency



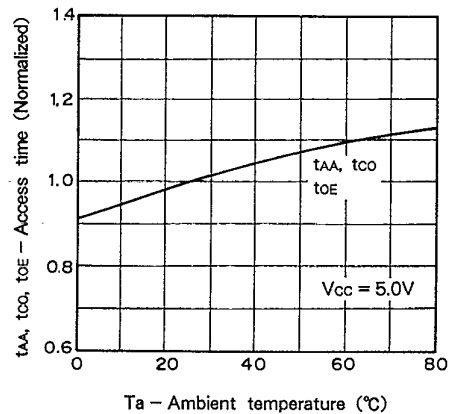
Access time vs. Load capacitance



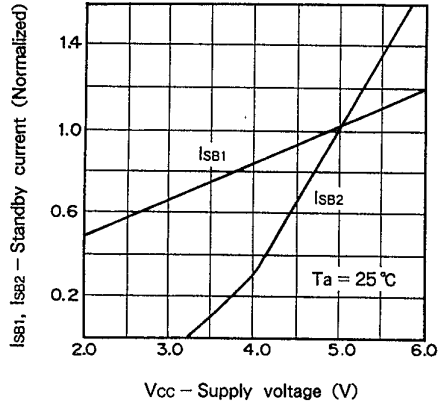
Access time vs. Supply voltage



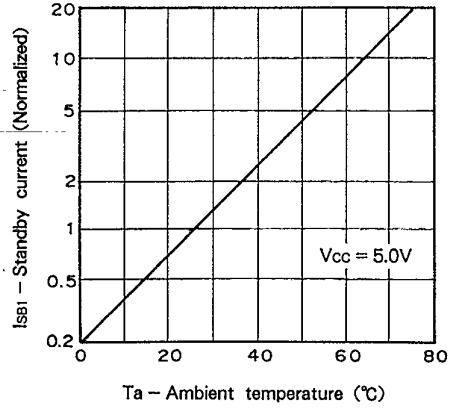
Access time vs. Ambient temperature



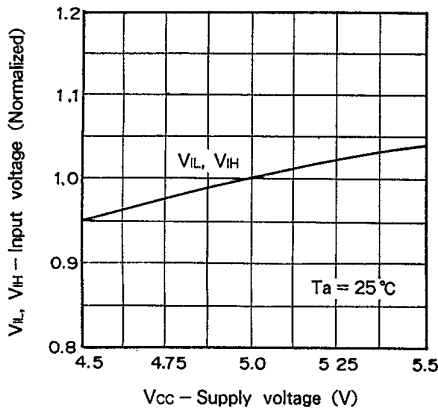
Standby current vs. Supply voltage



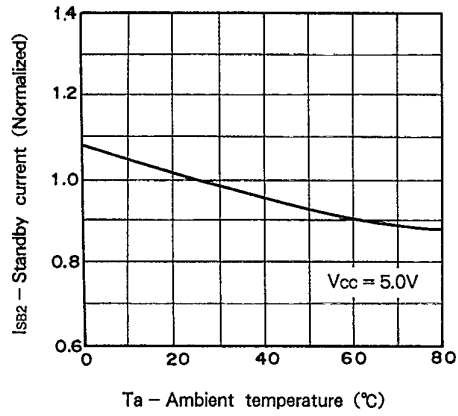
Standby current vs. Ambient temperature



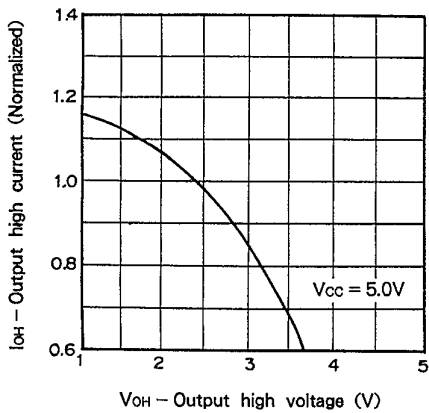
Input voltage level vs. Supply voltage



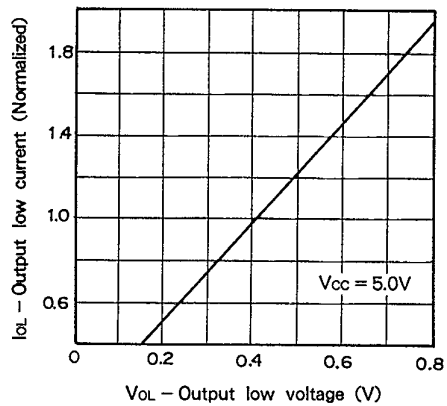
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

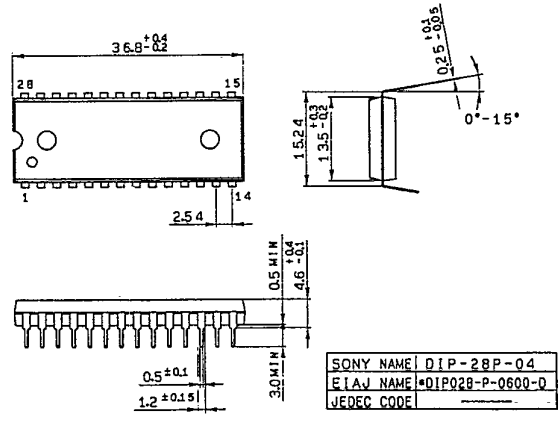


Output low current vs. Output low voltage

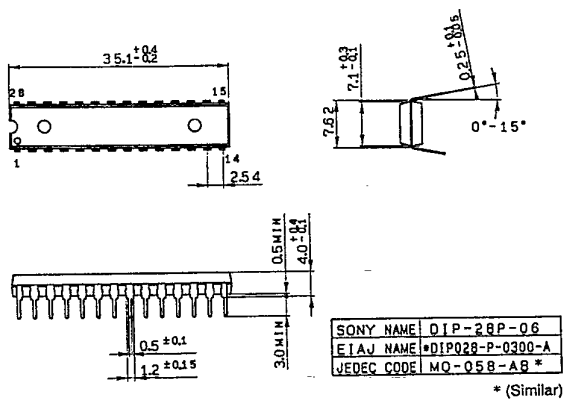


Package Outline Unit : mm

CXK58257AP 28pin DIP (Plastic) 600mil 4.2g



CXK58257ASP 28pin DIP (Plastic) 300mil 2.0g



CXK58257AM 28pin SOP (Plastic) 450mil 0.7g

