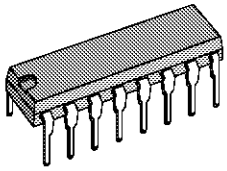
SGS-THOMSON MICROELECTRONICS

L584

MULTIFUNCTION INJECTION INTERFACE

PRELIMINARY DATA

- DRIVES ONE OR TWO EXTERNAL DARLINGTONS
- DUAL AND SINGLE LEVEL CURRENT CONTROL
- SWITCHMODE CURRENT REGULATION
- ADJUSTABLE HIGH LEVEL CURRENT DURATION
- WIDE SUPPLY RANGE (4.75 - 46V)
- TTL-COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- DUMP PROTECTION



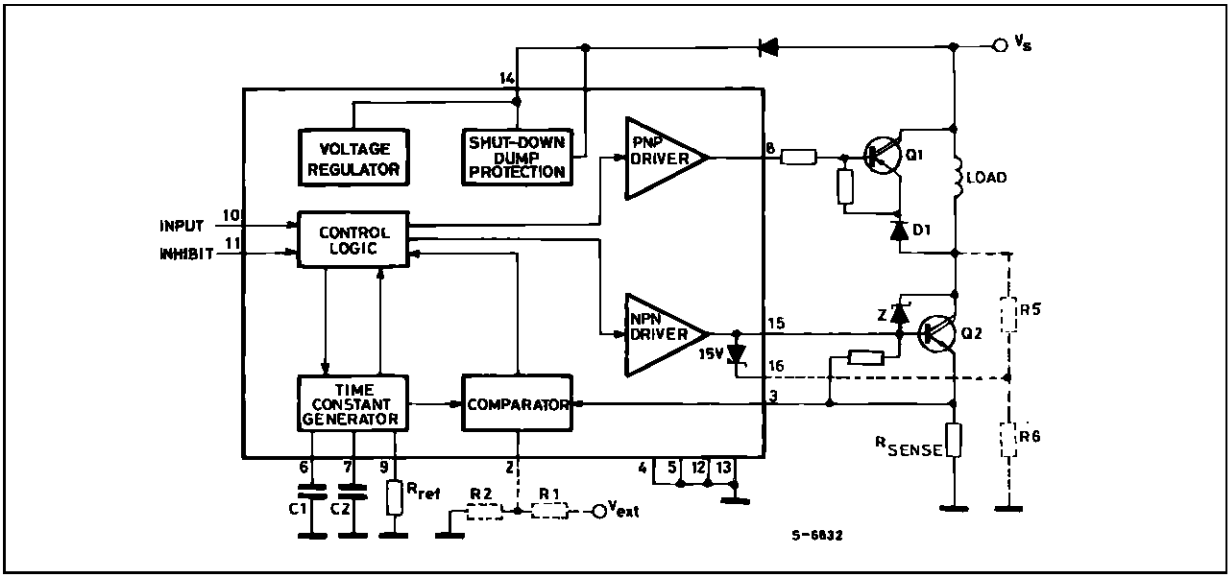
DIP16 (12 + 2 + 2)

ORDERING NUMBER : L584

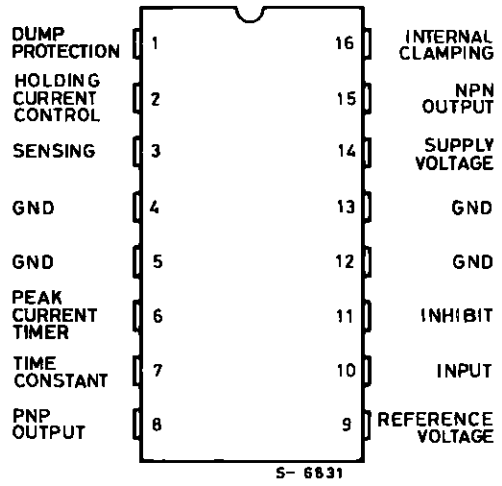
DESCRIPTION

The L584 is designed to drive injector solenoids in electronic fuel injection systems and generally inductive loads for automotive applications. The device is controlled by two logic inputs and features switchmode regulation of the load current driving an external darlington and an auxiliary one for the current recirculation. A key feature of the L584 is flexibility. It can be used with a variety of darlingtons to match the requirements of the load and it allows both simple and two level current control. Moreover, the drive waveshape can be adjusted by external components. Other features of the device include dump protection, thermal shutdown, a supply voltage range of 4.75 - 46V and TTL-compatible inputs. The L584 is supplied in a 16 lead Powerdip package which uses the four center pins to conduct heat to the PC board copper.

BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value
V_S	DC Supply Voltage (pin 1 open) Positive Transient Voltage (pin 1 connected to V_S, π_f fall time constant = 100ms) (5ms ≤ t_{rise} ≤ 10ms, R_{source} ≥ 0.5Ω)	– 0.2V min; +50V Max +60V Max
V_1	Input Voltage (pins 10, 11)	– 0.2V min; +7V Max
V_r	External Reference Voltage (pin 2)	– 0.2V min; +7V Max
V_{sens}	Sense Voltage (pin 3)	– 0.2V min; +7V Max
V_8	Max D.C. and Transient Voltage	50V
I_r	Reference Current (pin 9)	5mA Max
Tstg, Tj	Storage and Junction Temperature Range	–55 to 150°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	°C/W

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

N°	Name	Functions
1	Dump Protection	With pin 1 connected to pin 14 the device is protected against dump voltage ≤ 60V. The protectio.n operates at $V_S \geq 32V$ (typ.). If this protection is not used the pin must be left open
2	Holding Current Control	The voltage V_{set} applied to this pin sets the holding current level.
3	Sensing	Connection for load current sense resistor. Vazlue sets the peak and holding current levels. $I_P = 0.45/R_S$ (typ.); $I_h = V_{set}/R_s$. (see block diagram and fig. 4).
4	Ground	Ground Connection. With pins 5, 12 and 13 conducts heat to pc board copper.
5	Ground	See pin 4.
6	Peak Current Timer	A capacitor connected between this pin and ground sets the duration of the high level current (t_2 in fig. 4)
7	Discharge Time Constant	A capacitor connected between this pin and ground sets the duration of t_{off} (fig. 4). If grounded, the current switchmode control is suppressed.
8	PNP Driving Output	Current sink for external PNP darlington (for recirculation). $I_{dp} = 35$ Ir (typ).
9	Reference Voltage	A resistor connected between this pin and ground sets the internal current reference, I_r. The recommended value is 1.2kΩ giving Ir = 1mA (typ.).
10	Input	TTL-compatible Input. A high level on this pin activates the output, driving the load.
11	Inhibit	TTL-compatible Inhibit Input. A high level on this input disables the output stages and logic circutry, irrespective of the state of pin 10.
12, 13	Ground	See Pin 4.
14	Supply Voltage	Supply Voltage Input.
15	NPN Driving Output	Current Source for External NPN Darlington (load driver).$I_{dn} = 100$ I_r (typ.)
16	Internal Clamping	Internal Clamp Zener for Fast Turn-off.

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ELECTRICAL CHARACTERISTICS (V_S (Pin 14) = 14.4V; –40 ≤ Tj ≤ 105°C; R_{ref} = 1.20KΩ unless otherwise specified; refer to fig. 1)

Symbol	Parameter	Test Condiction	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage	Pin 1 Open	4.75		44	V
V_d	Dump Protection Threshold	Pin 1 = V_S	28		36	V
R_d	Dump Protection Input Resistance	Pin 1 to GND	18		50	kΩ
I_q	Quiescent Current	Pin 14			45	mA
V_i	Input Threshold Voltages	Pin 10, 11 Low High	 2.0		0.8	 V V
I_i	Input Current	Pin 10, 11 Low High	 –100		 –250	 µA µA
V_r	Reference Voltage	Pin 9	1.15		1.35	V
R_r	Reference Resistor Range	Pin 9 to GND $I_r = V_r/R_r$	1		3.3	kΩ
I_6	Peak Duration Control Current	Pin 6 $V_{pin\,6} \leq 1.8V$	$I_r/9.50$		$I_r/6.00$	A
V_{6th}	Peak Duration Control Comparator Threshold	Pin 6	1.20		1.6	V
V_{6SAT}	Pin 6 Saturation Voltage	Pin 6 (discharge state)			200	mV
I_7	Off Duration Control Current	Pin 7 $V_{pin\,7} \leq 1.8V$	$(I_{r\,min})/9.50$		$(I_{r\,max})/6.00$	A
V_{7th}	Off Duration Control Comparator Threshold	Pin 7	1.20		1.6	V
V_{7SAT}	Pin 7 Saturation Voltage	Pin 7 (discharge state)			200	mV
V_{spt}	Peak Current Threshold Voltage	Pin 3	400		500	mV
V_{set}	Holding Current Set Voltage Range	Pin 2	0		2	V
V_{set}	Holding Current Set Voltage Range	Pin 3, Peak Value, dV/dt ≤ 1V/s	V_{set} – 0.01		V_{set} + 0.01	V
I_3	Pin 3 Bias Current	$V_{pin\,3}$ = 600mV	–200			µA
V_{cl}	Recirculation Zener Clamping Voltage	Pin 16 to Pin 15 @ 200mA into Pin16	13.5		18.5	V
I_{dn}	NPN Driver Source Current	$V_{pin\,15}$ = 0V	$70 \times I_r$		$140 \times I_r$	A
I_{dp}	PNP Driver Sink Current	Vpin 8 ≥ 4.75V	$25 \times I_r$		$60 \times I_r$	A

APPLICATION INFORMATION

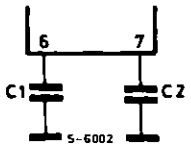
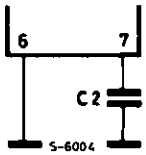
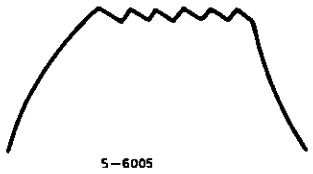
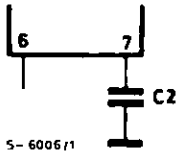
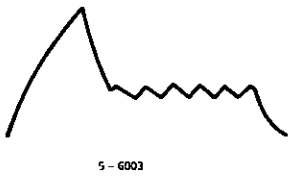
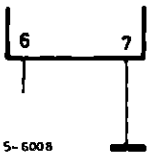
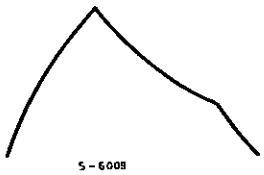
Controlled by a logic input and an inhibit input (both TTL compatible), the device drives the external darlington(s) to produce a load current waveform as shown in figure 4. This basic waveform shows that the device produces an initial high level current in order to ensure a fast opening, followed by a holding level current as long as the input is active. Both the peak and holding current are regulated by the L584's switchmode circuitry.

The duration of the high level current and the values of the peak and the holding currents can be adjusted by external components.

Moreover, by omitting C1, C2 or both it is possible to realize single-level current control, a transitory peak followed by a regulated holding current or a simple peak (figure 1).

The peak and holding current values are always re-

Figure 1 : Components Connected to Pins 6 and 7 Determine the Load Current Waveshape.

COMPONENTS ON PINS 6 AND 7	LOAD CURRENT WAVEFORM
	
	
	
	

ferred, in the following formula, to I_E, emitter current of the external darlington Q2,

$$I_E = I_{LOAD} + I_{dn}$$

because the sensing detection is on the darlington emitter (not directly on the load).

The peak current level I_p, is set by the sensing resistor, R_s, and is found from :

$$I_p = 0.45 / R_s \text{ (typ)}$$

The peak value of holding current level, I_h, is set by a voltage (V_{set}) applied to pin 2, giving :

$$I_{hp} = V_{setth} / R_s = (V_{set} \pm 10mV)/R_s$$

The peak to hold current ratio is fixed by V_{set} :

$$I_p / I_{hp} = 0.45 / V_{setth}$$

V_{set} is fixed by an external reference and a voltage divider (V_{ext}, R1, R2 in fig 2) :
$V_{set} = V_{ext} * R2 / (R1 + R2)$

Due to the particular darlington storage time and the device reaction time not very significant differences can be found between I_p and I_h values based on the previous formula and the real values seen in the applications.

If the holding current function is not used, pin 2 cannot be left floating and it must be connected to GND.

Figure 2 : Application Circuit Showing the Optional Components. In particular it illustrates how the holding current level is adjusted independently of the peak current (with R1, R2, V_{ext}) and how the internal zener clamp is connected. This circuit produces the waveforms shown in Fig. 4.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
12	BDV64	BDV65

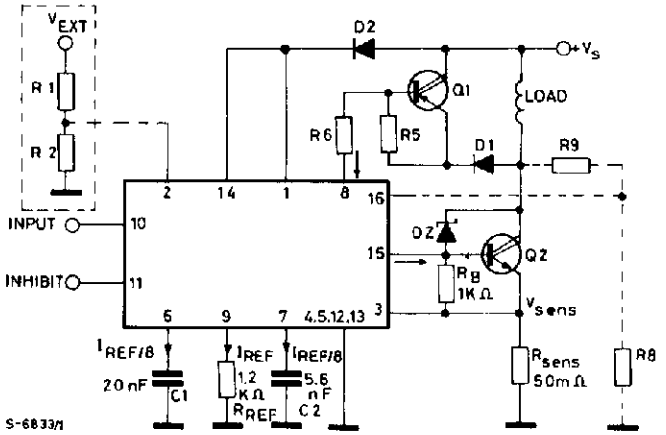
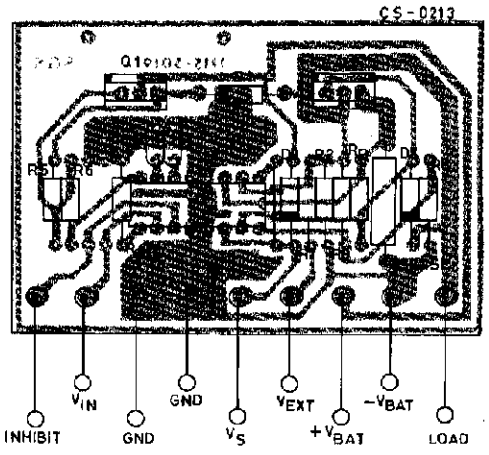


Figure 3 : P.C. Board and Components Layout of the Circuit of Fig. 2 (1 : 1 scale).



The drive current for the two darlingtons and the waveform time constants are all defined in turn by a resistor between pin 9 and ground.

The recommended value for I_r is 1mA which is obtained with a 1.2KΩ resistor. The darlington drive currents are given by :

PNP : $I_{dp} = 35\ I_r$ typ. NPN : $I_{dn} = 100\ I_r$ typ.

The duration of the high current level (t_2 in fig 4) is set by a capacitor connected between pin 6 and ground. This capacitor, C1 is related to the duration, t_2, by :

$$t_2 = C_1 \frac{V_{6th} - V_{6sat}}{I_6} = 12 \frac{C_1}{I_{ref}} \text{ (typ.)}$$

The discharge time constant (t_{off} in fig 4) is set by a capacitor C_2 between pin 7 and ground and is found from :

$$t_{off} = C2 \cdot \frac{V_{7th} - V_{7sat}}{I_7} = 12 \frac{C_r}{I_{ref}} \text{ (typ)}$$

Figure 4 : Waveforms of the Typical Application Circuit of Fig. 2.

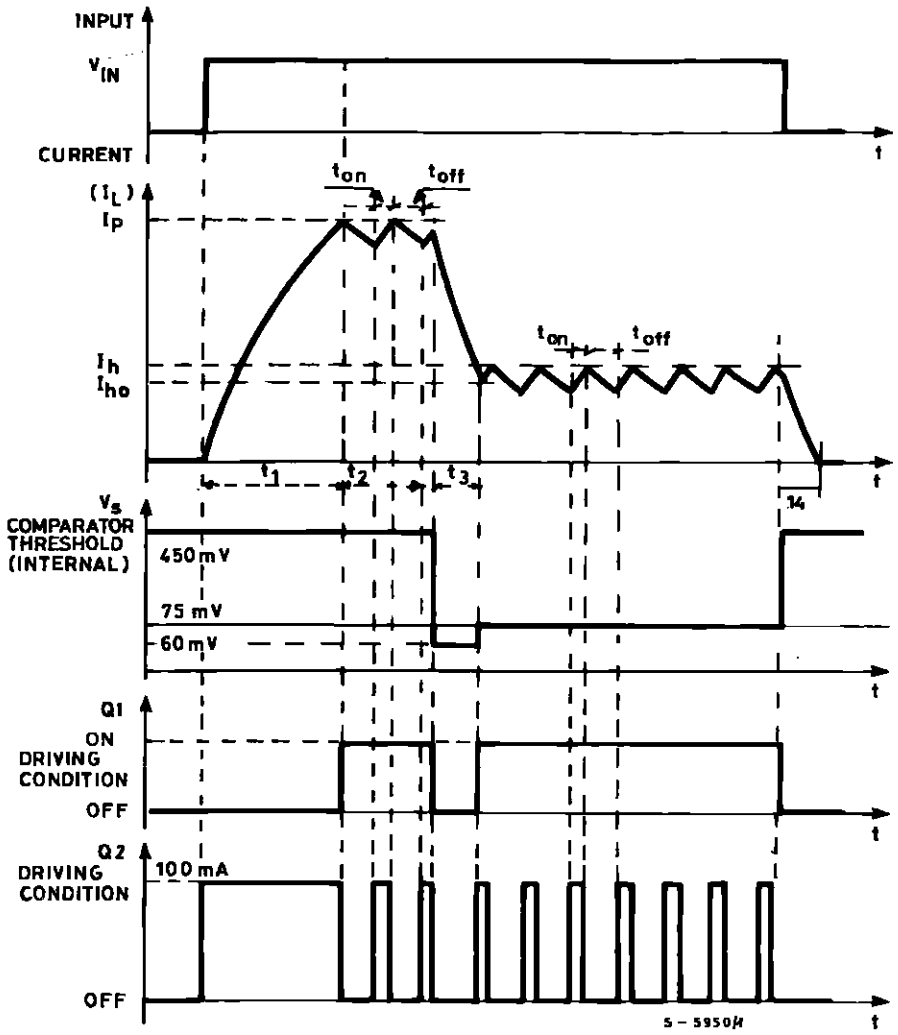
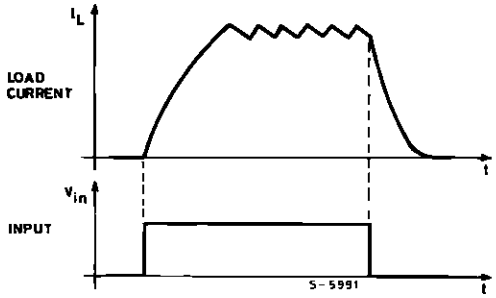


Figure 5 : When pin 6 is grounded, as shown here, the injector current is regulated at a single level.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



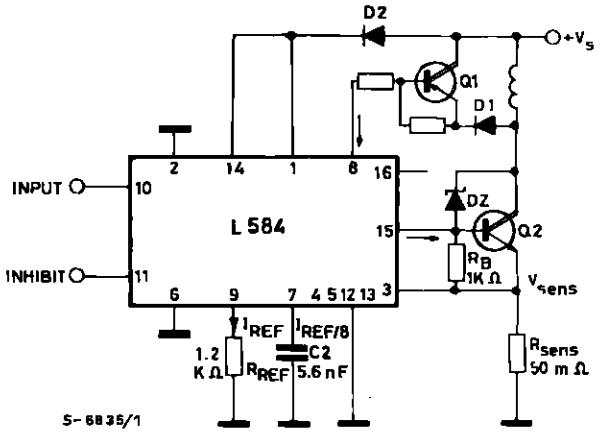
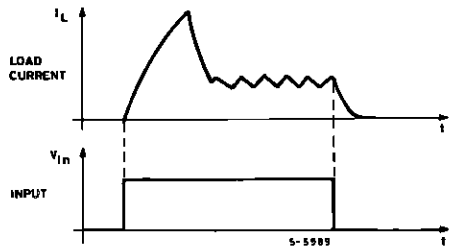


Figure 6 : In this application circuit, pin 6 is left open to give a single peak followed by a regulated holding current.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



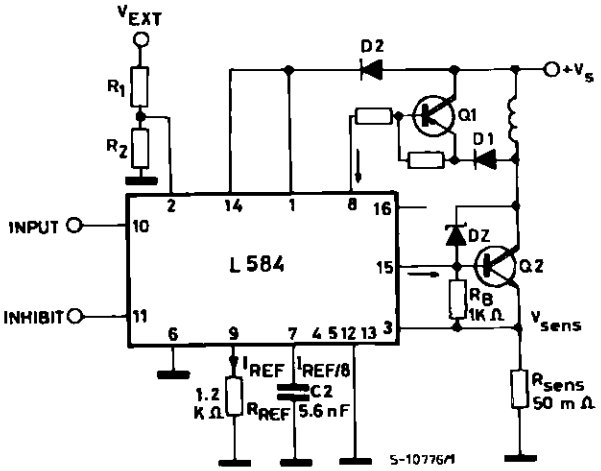
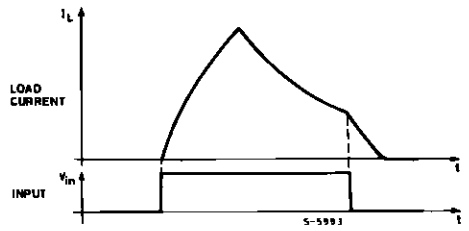


Figure 7 : Switchmode control of the current can be suppressed entirely by leaving pin 6 open and grounding pin 7. the peak current is still controlled.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



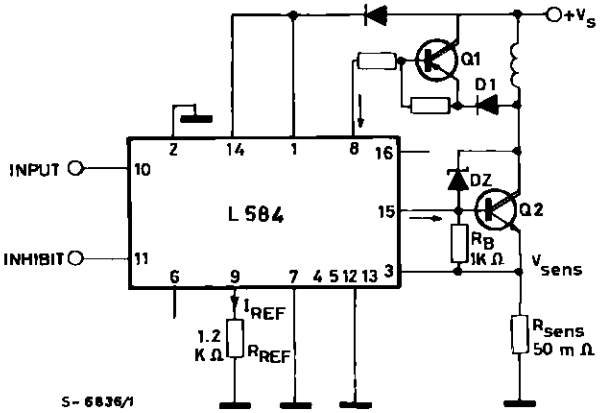
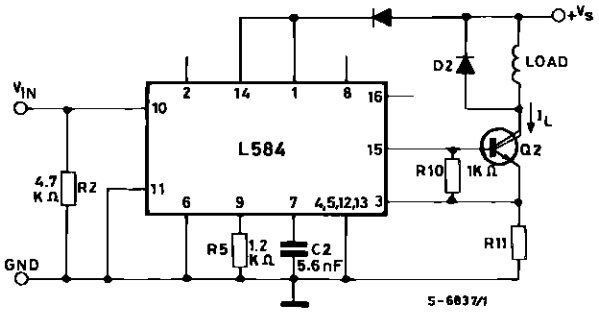
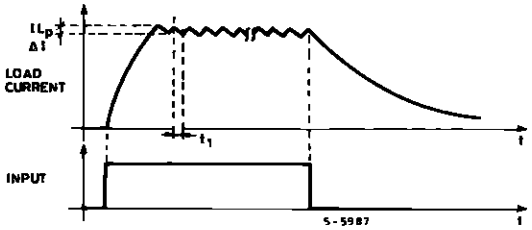


Figure 8 : Applications circuit using only one darlington with a single level of the injector current.





To have a very short off time when the L584 input goes LOW, an internal zener is available on pin 16. This zener is used with an external divider, R8, R9, as shown in figure 2. Suitable values can be found from :

$$V_{pin\ 16} \cong 15V + V_{BEQ2} + VRsense$$

$$V_{CQ2} \cong V_{pin\ 16} \cdot \frac{R9 + R8}{R8}$$

(V_{CQ2} is the voltage at the collector of Q2. V_{CQ2} max is 47V if the pin 8 is used for slow recirculation as in fig. 2).

To ensure stability, a small capacitor (about 200pF) must be connected between the base and collector of Q2 when pin 16 is used.

A different opportunity for a fast off time is based on the use of the external zener diode Dz. In this case also the maximum Dz voltage value is 47V.

LOAD DUMP PROTECTION

To protect the device against the positive load dump it is necessary to connect pin 1 to V_S. In this case, if V_S is higher than 32V, the device turns off Q_2 and turns on Q_1. The external resistor R_6 must be used (see application circuit) to avoid that pin 8 voltage exceeds 50V during load dump. R_6 must be :

$$R_6 > \frac{V_{DUMP} - V_8}{I_{dp}}$$

where V_{DUMP} is the dump voltage value and V_8 : $4.75V < V_8 < 47V$.

For this R_6 value, the minimum supply voltage V_{Smin} guaranteeing Q1 operation is given by :

$$V_{Smin} = R6\left(\frac{Ip}{B_{Q1}}(+2)\frac{V_{BEQ1}}{R_5}\right) + V_{8sat}$$

In relation to V_{Smin} it is no more verified $I_{dp} = 35\ I_{ref}$ (typ) even if the system correct operation is completely guaranteed.

The L584 application circuit suggested in these notes allows the use of inductive loads with the lowest possible series resistance (compatible with constructional requirements) and therefore reduces notably the power dissipation.

For example, an electronic injector driven from 14.4V which draws 2.4A has a series resistance of 6Ω and dissipates 34.56W. Using this circuit a injector with a 1Ω series resistance can be used and the power dissipation is :

$$P_d = R_L I_L^2 + V_D I_L (1 - \sigma) + V_{sat} \cdot IL\ \sigma + R_S\ I_L^2\ \sigma$$

where R_L = resistance of injector = 1Ω

V_D = drop across diode, $V_D \cong 1V$

V_{sat} = saturation voltage of Q2, ≅ 1V

R_S = R11 = 185mΩ

σ = duty cycle = 20%

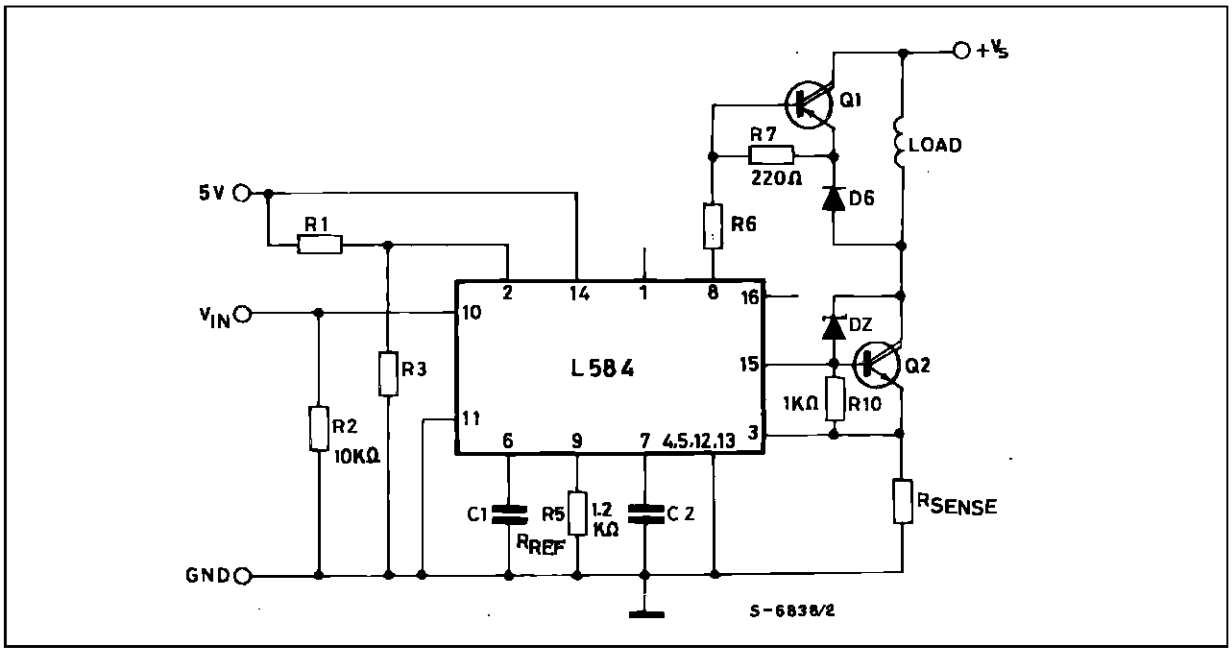
therefore :

$Pd \cong 5.76 + 1.92 + 0.48 + 0.21 = 8.37W$

This given two advantages : the size (and cost) of the injector is reduced and the drive current is reduced from 2.4A to about 0.4A.

The application circuit of figure 9 is very similar to figure 2 except that it shows the use of two supplies : one for the control circuit, one for the power stage.

Figure 9 : Application circuit showing how two separate supplies can be used.



In this application it is assumed that the 5V supply for L584 is taken from a logic supply, which is already protected, against load dump transients and vol-tage reversal.

Pin 1 must be left open, as shown in fig. 9, if V_S is always lower than 46V even during the voltage transients.

Note that t_{off} is also related to the required current ripple ΔI on the peak or on the holding current level by :

$$t_{off} = -\frac{L}{R} \ln \frac{(I_o - \Delta I)\, R_L + V_{off}}{I_o\, R_L + V_{off}}$$

Where : Io is the initial current value in OFF condition (equal to Ip or IH in accordance to the current level considered),

$$V_{OFF} = V_{DIODE} + V_{CEQ1}$$

R_L is the series resistance value of the inductance L :

Therefore C_2 can be dimensioned directly by :

$$C_2 = \frac{I_{REF}\, L}{12} \quad \frac{\ln}{R_L} \quad \frac{(I_o - \Delta I)\, R_L + V_{OFF}}{I_o\, R_L + V_{OFF}}$$

Note that t_{off} is the same for both the peak and holding current.

t_{on} time is given by :

$$t_{on} = \frac{L}{R} \ln \frac{V_{on} - R(I1 - \Delta I)}{V_{on} - RI1}$$

where : I1 is the final current value in ON condition (equal to I_p or I_H in accordance to the current level considered),

$$R = R_L + R_{SENSE}$$

$$V_{on} = V_S - V_{CE}satQ2$$

If the constant times are respectively

$$\frac{L}{R} > 20\ t_{off} \quad \text{and} \quad \frac{L}{R} > 20\ t_{on}$$

it is possible to consider a purely inductive load and therefore :

$$t_{off} = L\ \frac{\Delta I}{V_o}\ ;\ t_{on} = L\ \frac{\Delta I}{V_{on}}$$

DIP16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050