32,768 WORD x 8 BIT CMOS PSEUDO STATIC RAM

T-46-23-14

DESCRIPTION

The TC51832 Family is a 256K bit high-speed CMOS Pseudo-Static RAM organized as 32,768 words by 8 bits. The TC51832 Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC51832 Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC51832 Family is pin-compatable with the 256K bit static RAM. The TC51832P is offered in a standard 28 pin 0.6 inch and 0.3 inch width plastic DIP. The TC51832F is offered in a standard 28 pin 0.450 inch width small out-line plastic flat package.

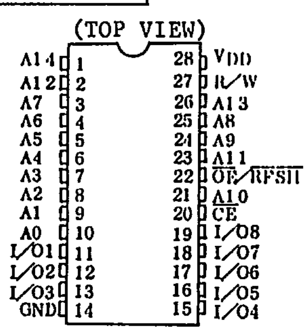
FEATURES

- Organization: 256K bit(32,768 word × 8 bit)
- Fast Access Time and Low Power Dissipation

	TC51832P Family		
	-85	-10	-12
t_{CEA} $\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	135ns	160ns	190ns
P_D -Operating- Max.	303mW	248mW	220mW
Self Refresh Current	1mA/100μA (-L)		

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs: TTL compatible
- 256 refresh cycle/4ms
- Pin Compatible: 256K SRAM TC55257
- Logic Compatible: SRAM R/W Pin
- 28 pin Standard Plastic PKG
  - P/PL : 600 mil DIP
  - SP/SPL: 300 mil DIP
  - F/FL : 450 mil SOP

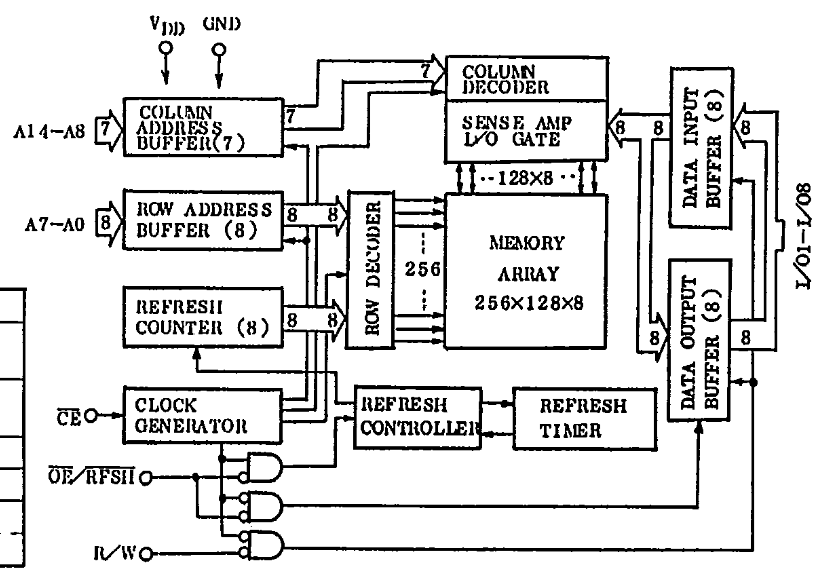
PIN CONNECTION



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable/ Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ∿ I/O8	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	-1.0∿7.0	V	1
V_{OUT}	Output Voltage	-1.0∿7.0	V	1
V_{DD}	Power Supply Voltage	-1.0∿7.0	V	1
T_{OPR}	Operating Temperature	0∿70	°C	1
T_{STG}	Storage Temperature	-55∿150	°C	1
T_{SOLDER}	Soldering Temperature·Time	260 · 10	°C·sec	1
P_D	Power Dissipation	600	mW	1
I_{OUT}	Short Circuit Output Current	50	mA	1

DC RECOMMENDED OPERATING CONDITIONS (Ta=0∿70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, Ta=0∿70°C)

SYMBOL	PARAMETER	PERIOD	MIN.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address Cycling: t_{RC}=t_{RC} MIN.	135ns	–	55	mA	3,4
		160ns	–	45		
		190ns	–	40		
I_{DDS1}	Standby Current 1 $\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{IH}	TC51832P/SP/F	–	2	mA	
		TC51832PL/SPL/FL	–	1		
I_{DDS2}	Standby Current 2 $\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{DD}-0.2V	TC51832P/SP/F	–	1	mA	
		TC51832PL/SPL/FL	–	100	μA	
I_{DDF}	Self Refresh Current $\overline{CE}$=V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$=0.2V	TC51832P/SP/F	–	1	mA	
		TC51832PL/SPL/FL	–	100	μA	
$I_{I(L)}$	Input Leakage Current 0V≦V_{IN}≦V_{DD}, All other inputs not under test=0V		-10	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, 0V≦V_{OUT}≦V_{DD}		-10	10	μA	
V_{OH}	Output High Level I_{OUT}=-5mA		2.4	–	V	
V_{OL}	Output Low Level I_{OUT}=4.2mA		–	0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD}=5V±10%, Ta=0∿70°C) (NOTES:5,6,7,8,9)

SYMBOL	PARAMETER	-85		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	200	-	240	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write Enable	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	-	70	-	85	-	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	85	-	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	12
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	12
t_{FC}	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
t_{FCE}	$\overline{RFSH}$ to $\overline{CE}$ Active Delay Time	160	-	190	-	225	-	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	13
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	13

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(Continued)

SYMBOL	PARAMETER	-85		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD}=5V, f=1MHz, Ta=25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A0∿A14)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE}/\overline{RFSH}$, R/W)	-	7	pF
C_{IO}	Input/Output Capacitance (I/O1∿I/O8)	-	7	pF

NOTE) This parameter is periodically sampled and is not 100% tested.

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NOTES:

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) IDDO depends on cycle rate.

4) IDDO depends on output loading. Specified values are obtained with the output open.

5) An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}/\overline{RFSH}$ are required after power-up, before proper device operation is achieved.

6) AC measurements assume t_T=5ns.

7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) The $\overline{OE}/\overline{RFSH}$ input operates as the output enable input ($\overline{OE}$) and refresh control input ($\overline{RFSH}$) under the condition of that $\overline{CE}=V_{IL}$ and $\overline{CE}=V_{IH}$, respectively.

10) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW}, t_{DSC}) and hold time (t_{DHW}, t_{DHC}).

12) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore all the address inputs must be valid during t_{ASC} and t_{AHC}.

13) Two refresh operation - auto refresh and self refresh are defined by the $\overline{OE}/\overline{RFSH}$ pulse width under the condition of $\overline{CE}=V_{IH}$.

    Auto refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\leq$ tFAP (max.)
    Self refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\geq$ tFAS (min.)

The following timing parameter must be kept for proper device operation after refresh

    Auto refresh: tFCE
    Self refresh: tFRS

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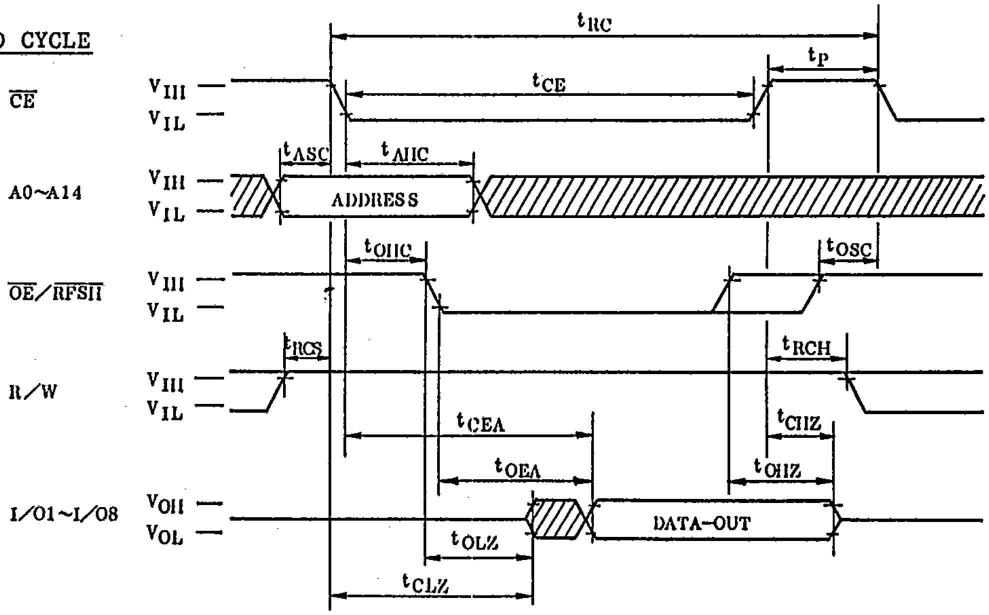
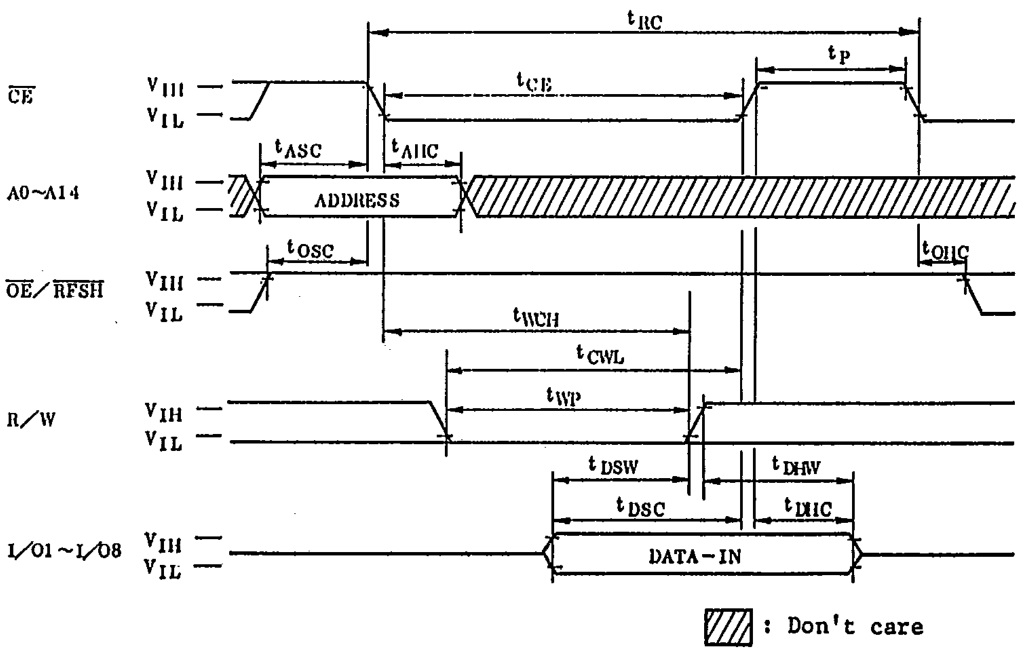
TIMING CHART

READ CYCLE



WRITE CYCLE



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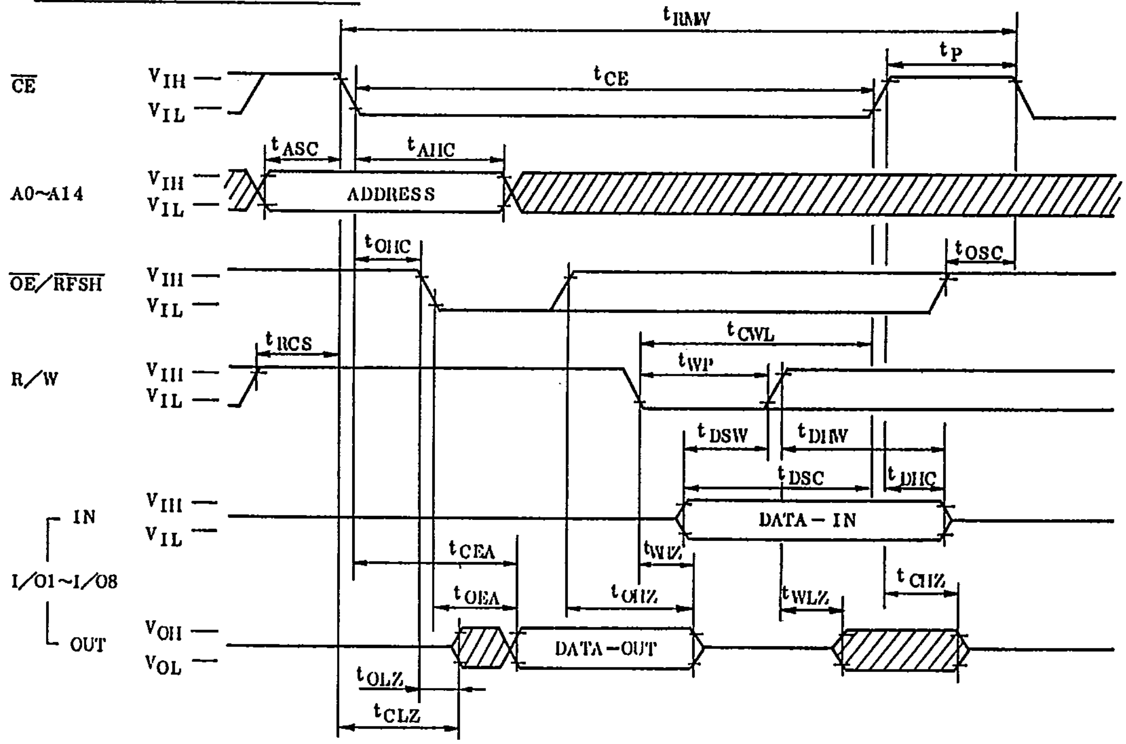
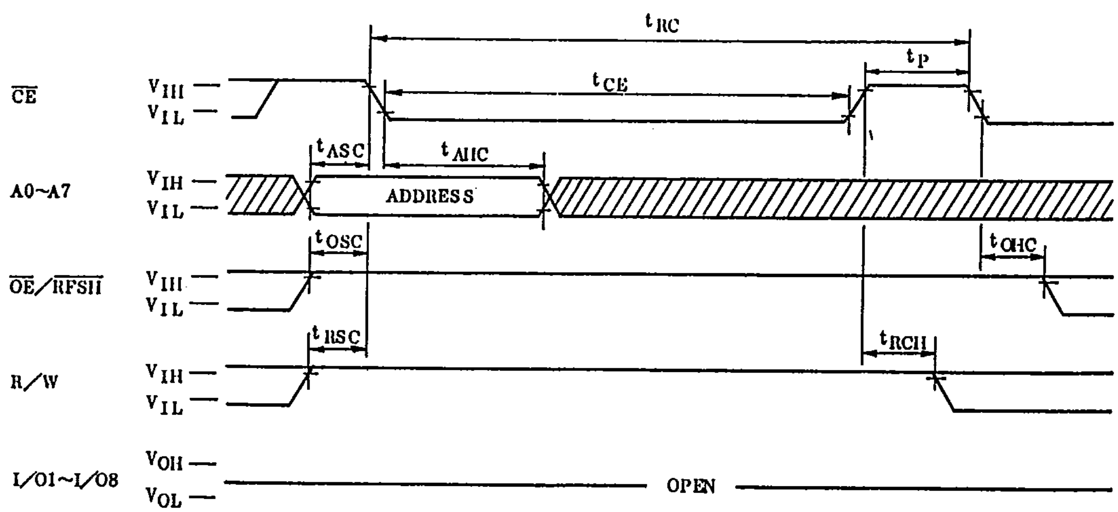
READ MODIFY WRITE CYCLE

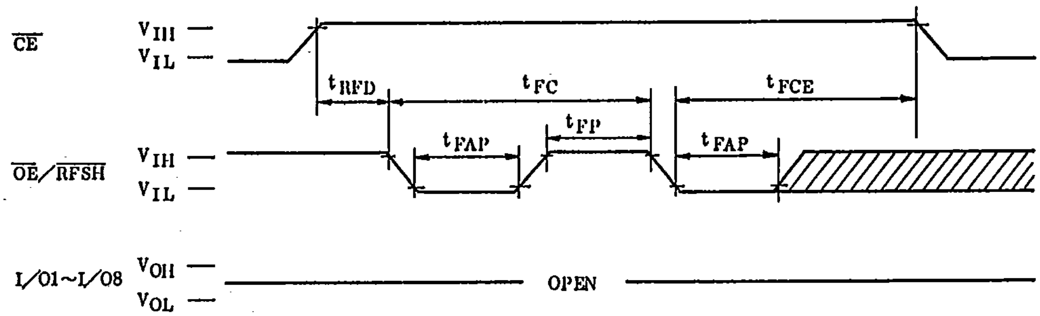


CE ONLY REFRESH CYCLE



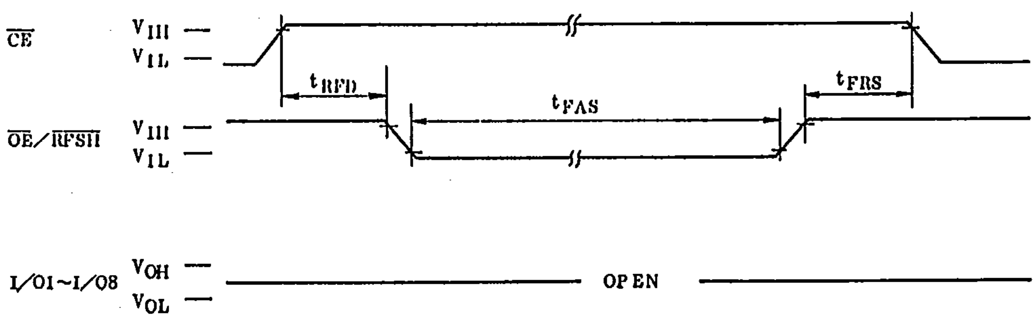
▨ : Don't care

AUTO REFRESH CYCLE



Note) A0∿A14, R/W=Don't care ▨: Don't care

SELF REFRESH CYCLE



Note) A0∿A14, R/W=Don't care

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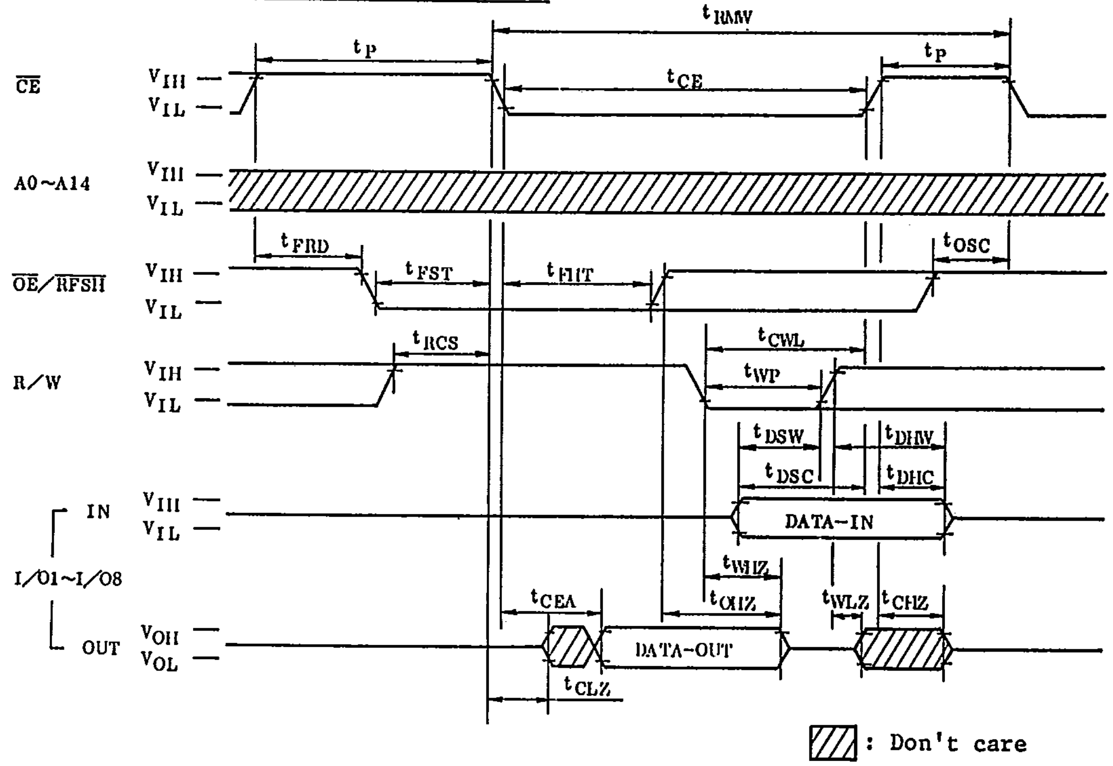
REFRESH COUNTER TEST CYCLE (READ WRITE)



REFRESH COUNTER TEST

The internal refresh operation of TC51832P family can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.

The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

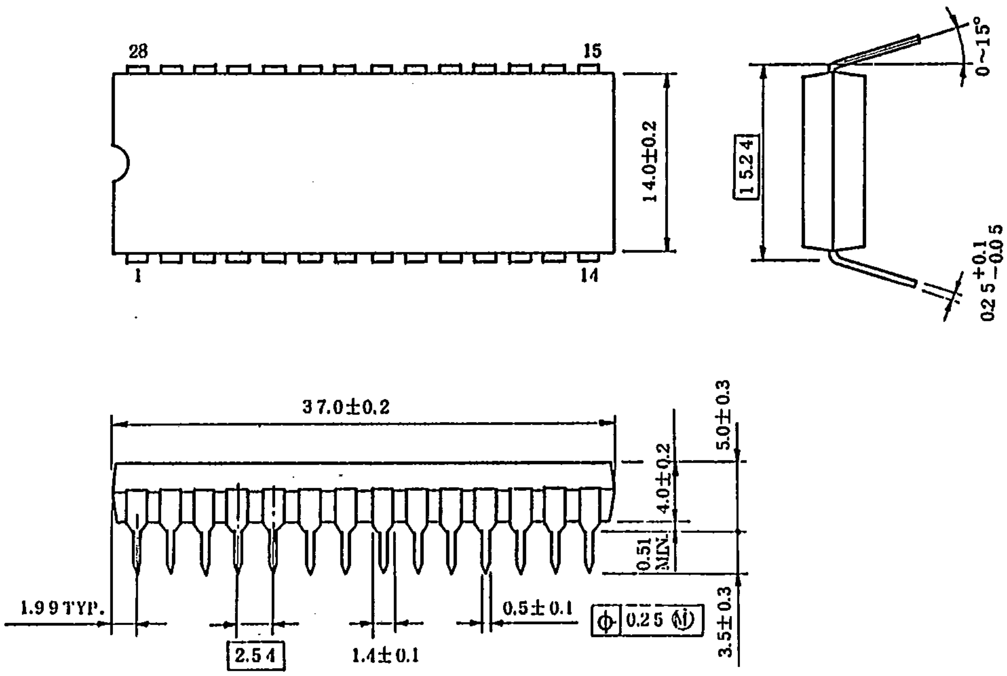
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS (DIP28-P-600)

Unit in mm



NOTES: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832P-85, TC51832PL-85
TC51832P-10, TC51832PL-10
TC51832P-12, TC51832PL-12

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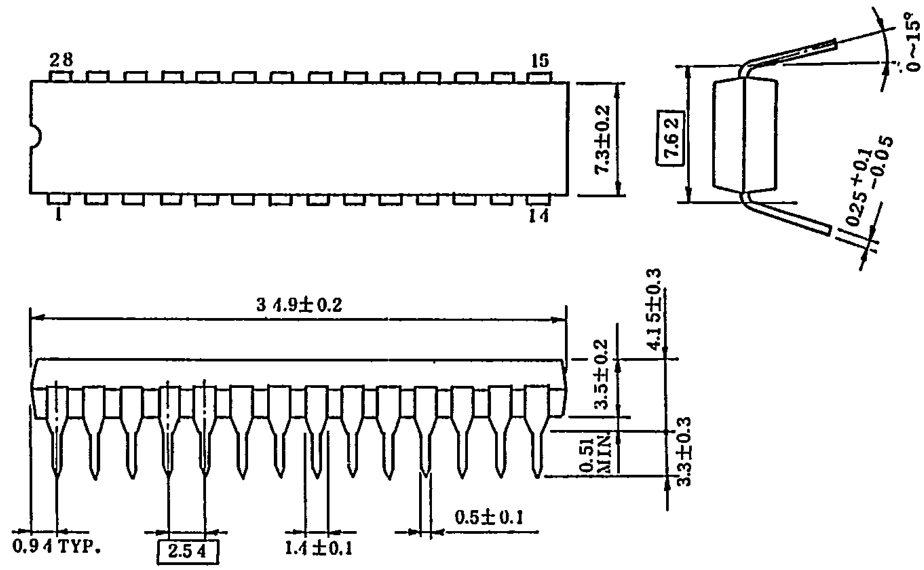
OUTLINE DRAWINGS (DIP28-P-300)

Unit in mm



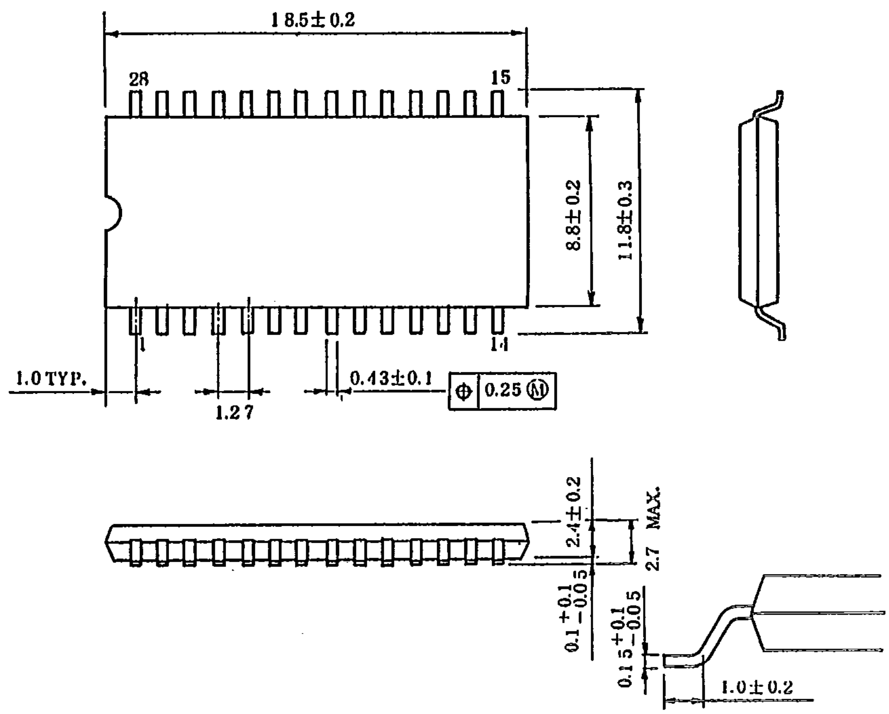
Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832SP-85, TC51832SPL-85
TC51832SP-10, TC51832SPL-10
TC51832SP-12, TC51832SPL-12

OUTLINE DRAWINGS (SOP28-P-450)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832F-85, TC51832FL-85
TC51832F-10, TC51832FL-10
TC51832F-12, TC51832FL-12