



SANYO Semiconductors DATA SHEET

LA6558 — Monolithic Llinear IC 6-CH Driver for Mini Disk and Compact Disk Applications

Overview

The LA6558 is a 6-channel driver developed for MD and CD players.

Features

- Power amplifier 6-channel built-in
- I_O max 700mA
- Level shift circuit built-in (BTL AMP)
- One mute circuit (output ON/OFF) built-in
- 3.3V power supply built-in (I_O max=300mA)
- 5V power supply built-in (I_O max=5mA)
- Overheat protection circuit (thermal shutdown) built-in

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC} max		14	V
Maximum output current	I_O max		0.7	A
Maximum input voltage	V_{INB}	Each CH for CH1 to CH6	13	V
Mute pin voltage	V_{MUTE}		13	V
Allowable operation	P_d max	Mounted on a board	2.00	W
		Independent IC	1.20	
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

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LA6558

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}		6 to 13	V

Electrical Characteristics at $S-V_{CC} = P-V_{CC} = 8\text{V}$, $V_{REF} = 1.65\text{V}$, $T_a = 25^\circ\text{C}$, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All Blocks						
No-load current drain ON	I_{CC-ON}	All AMPs output ON *1		30	50	mA
No-load current drain OFF	I_{CC-OFF}	All AMPs output OFF *1		10	20	mA
VREF input voltage range	V_{REF-IN}		0.5		$V_{CC}-1.5$	V
BTL AMP Block						
Output offset voltage	V_{OFF}	Voltage difference between output AMPs, each CH	-50		+50	mV
Input voltage range	V_{IN}		0		V_{CC}	V
Output voltage	V_O	Voltage between each V_{O+} and V_{O-} when $R_L=8\Omega$ *2	4	4.5		V
Closed-circuit voltage gain	VG	Input/output gain Input resistance 11k Ω		12		dB
Slew rate	SR	Multiply 2 between outputs. *3		1		V/ μs
MUTE ON voltage	$V_{MUTE-ON}$	Each MUTE *4			0.5	V
MUTE OFF voltage	$V_{MUTE-OFF}$	Each MUTE *4	2			V
Loading Block						
Voltage between outputs F	V_{OF}	$V_{IN+}=2\text{V}$, $V_{IN-}=0\text{V}$	2.5	2.9	3.3	V
Voltage between outputs R	V_{OR}	$V_{IN+}=0\text{V}$, $V_{IN-}=2\text{V}$	-3.3	-2.9	-2.5	V
Output voltage range F	V_{OMF}	$V_{IN+}=5\text{V}$, $V_{IN-}=0$	5.2	5.7		V
Output voltage range R	V_{OMR}	$V_{IN+}=0\text{V}$, $V_{IN-}=5\text{V}$		-5.7	-5.2	V
Output offset voltage	V_{OFF}	Voltage difference between outputs when brake is applied.	-50		+50	mV
Input current	I_{IN}	At $V_{IN}=3.3\text{V}$			500	μA
3.3VREG Block						
Output voltage	V_{O-REG1}	$I_O=100\text{mA}$	3.15	3.3	3.45	V
Line regulation	$\Delta V-LIN1$	$V_{CC}=6$ to 12V at $I_O=100\text{mA}$	-100		+100	mV
Load regulation	$\Delta V-LOAD1$	$I_O=0$ to 200mA	-100		+100	mV
5VREG Block						
Output voltage	V_{O-REG2}	$I_O=3\text{mA}$	4.75	5	5.25	V
Line regulation	$\Delta V-LIN1$	$I_O=3\text{mA}$, $V_{CC}=6$ to 12V		100		mV
Load regulation	$\Delta V-LOAD$	$I_O=1$ to 3mA		100		mV
O-RESET Block (Operating for Vref)						
H reset output voltage	V_{ORH}	10k Ω between V_{CC} -RESET	6.5			V
L reset output voltage	V_{ORL}	10k Ω between V_{CC} and RESET			0.5	V
O-RESET threshold voltage	V_{RT}		0.5	0.7	0.9	V
O-RESET hysteresis voltage	V_{hys}		50	100	200	mV

*1. $P-V_{CC}$ and $S-V_{CC}$ total current dissipation under no load.

*2. Voltage difference between both ends of the load(8 Ω). Output in the saturated condition.

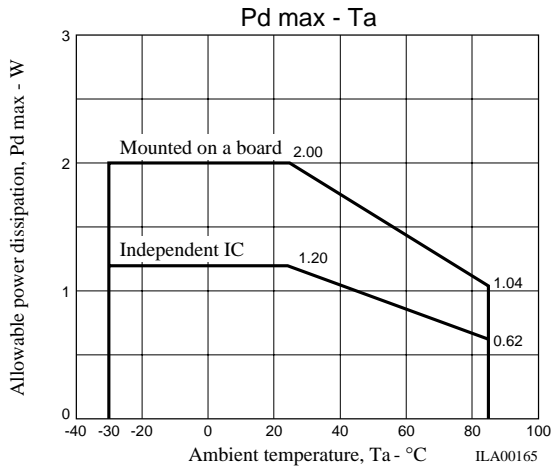
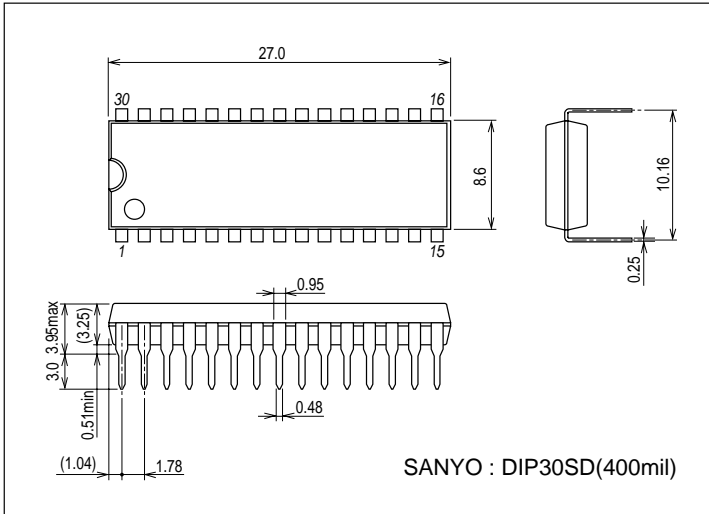
*3. These values are design guarantee values, and are not tested.

*4. Output is ON with IN-MUTE: [H] and OFF (HI impedance) with IN-MUTE: [L].

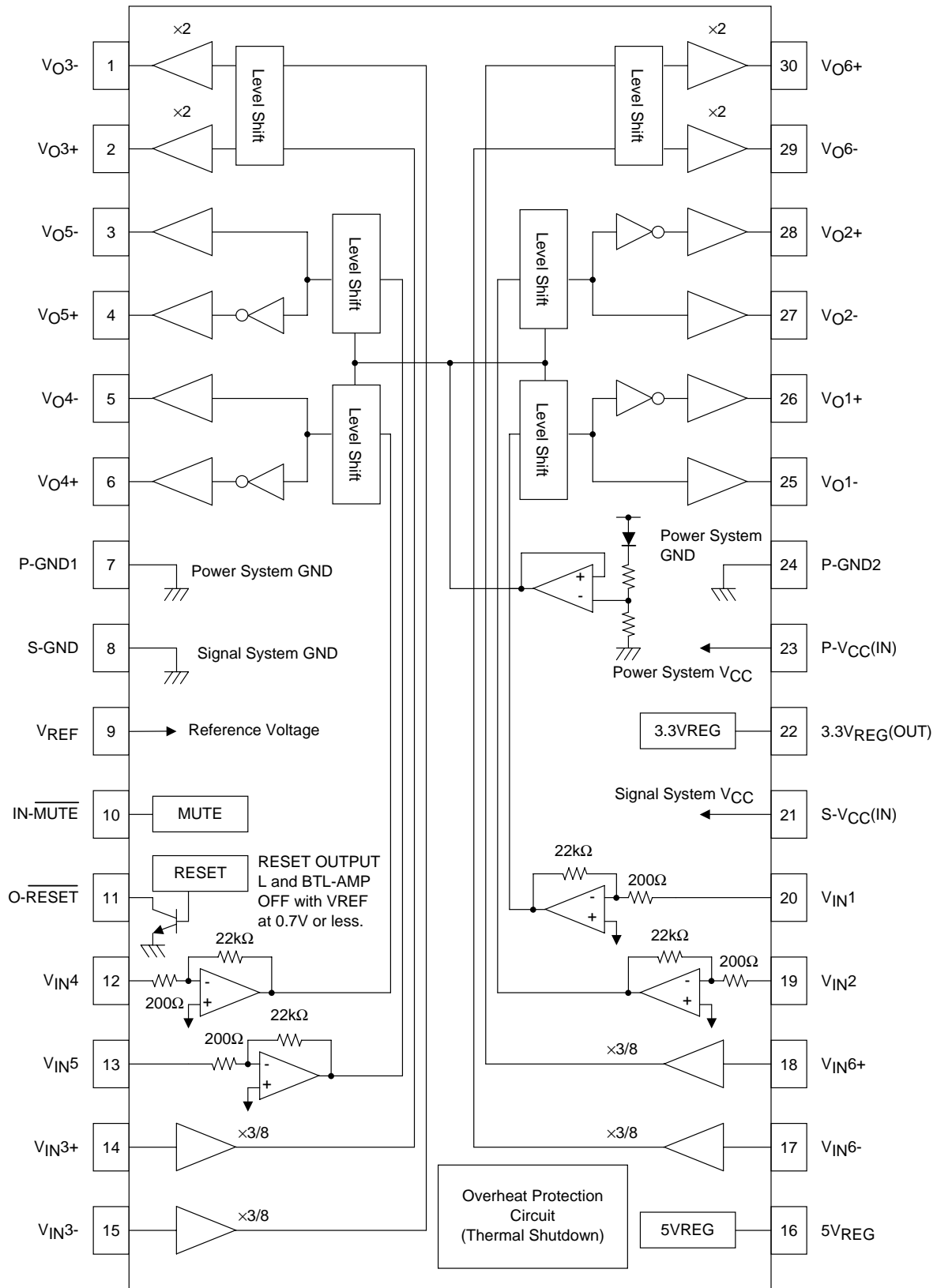
Package Dimensions

unit : mm (typ)

3196A



Block Diagram



Pin Functions

Pin No.	Pin Name	Description (functions)
1	V _{O3-}	Output for CH3 (-)
2	V _{O3+}	Output for CH3 (+)
3	V _{O5-}	Output for CH5 (-), inverted relative to input
4	V _{O5+}	Output for CH5 (+), not inverted relative to input
5	V _{O4-}	Output for CH4 (-), inverted relative to input
6	V _{O4+}	Output for CH4 (+), not inverted relative to input
7	P-GND1	Power system GND (CH3, 4, 5)
8	S-GND	Signal system GND
9	V _{REF}	Reference voltage input pin
10	IN-MUTE	Output ON/OFF for BTL AMP (CH1, 2, 4, and 5) and 3.3 V, 5 V _{REG} . ([H]: Output ON, [L]: Output OFF)
11	O-RESET	Reset output (Open collector)
12	V _{IN4}	Input for CH4
13	V _{IN5}	Input for CH5
14	V _{IN3+}	Input for CH3 (+)
15	V _{IN3-}	Input for CH3 (-)
16	5V _{REG}	5V Power output
17	V _{IN6-}	Input for CH6 (-)
18	V _{IN6+}	Input for CH6 (+)
19	V _{IN2}	Input for CH2
20	V _{IN1}	Input for CH1
21	S-V _{CC}	Signal system V _{CC}
22	3.3V _{REG}	3.3V Power output
23	P-V _{CC}	Power system power supply
24	P-GND2	Power system GND(CH1, 2, 6)
25	V _{O1-}	Output for CH1 (-), inverted relative to input
26	V _{O1+}	Output for CH1 (+), not inverted relative to input
27	V _{O2-}	Output for CH2 (-), inverted relative to input
28	V _{O2+}	Output for CH2 (+), not inverted relative to input
29	V _{O6-}	Output for CH6 (-)
30	V _{O6+}	Output for CH6 (+)

*1. Connect P-GND and S-GND externally and set both to the lowest potential (sub-straight).

*2. Connect S-V_{CC} and P-V_{CC} externally for use as power supplies.

Pin Description

Pin Name	Pin Name	Pin No	Description	Equivalent Circuit Diagram
Input (BTL AMP)	V _{IN1} V _{IN2} V _{IN4} V _{IN5}	20 19 12 13	Each input pin	<p>The diagram shows a differential pair of transistors. The input V_{IN} is connected to the bases of two transistors. The emitters are connected to a common point, which is also connected to a V_{ref} input. The collectors are connected to a common rail. The output is taken from the collector of one of the transistors.</p>
Output (BTL AMP)	V _{O1+} V _{O1-} V _{O2+} V _{O2-} V _{O4+} V _{O4-} V _{O5+} V _{O5-}	26 25 28 27 6 5 4 3	Each output	<p>The diagram shows a push-pull output stage. The output OUT is taken from the collector of a transistor. The emitter is connected to a common rail. The base is connected to a common rail. The collector is connected to a common rail. The output is taken from the collector of the transistor.</p>
Mute	IN-MUTE	10	Output ON/OFF. IN-MUTE: H output ON IN-MUTE: L output OFF	<p>The diagram shows a transistor with its base connected to the IN-MUTE input through a 100kΩ resistor. The emitter is connected to S-GND through a 100kΩ resistor. The collector is connected to VCC through a 100kΩ resistor. The output is taken from the collector.</p>
Reset	O-RESET	11	Open collector	<p>The diagram shows an open collector output stage. The output is taken from the collector of a transistor. The emitter is connected to ground. The base is connected to a common rail.</p>

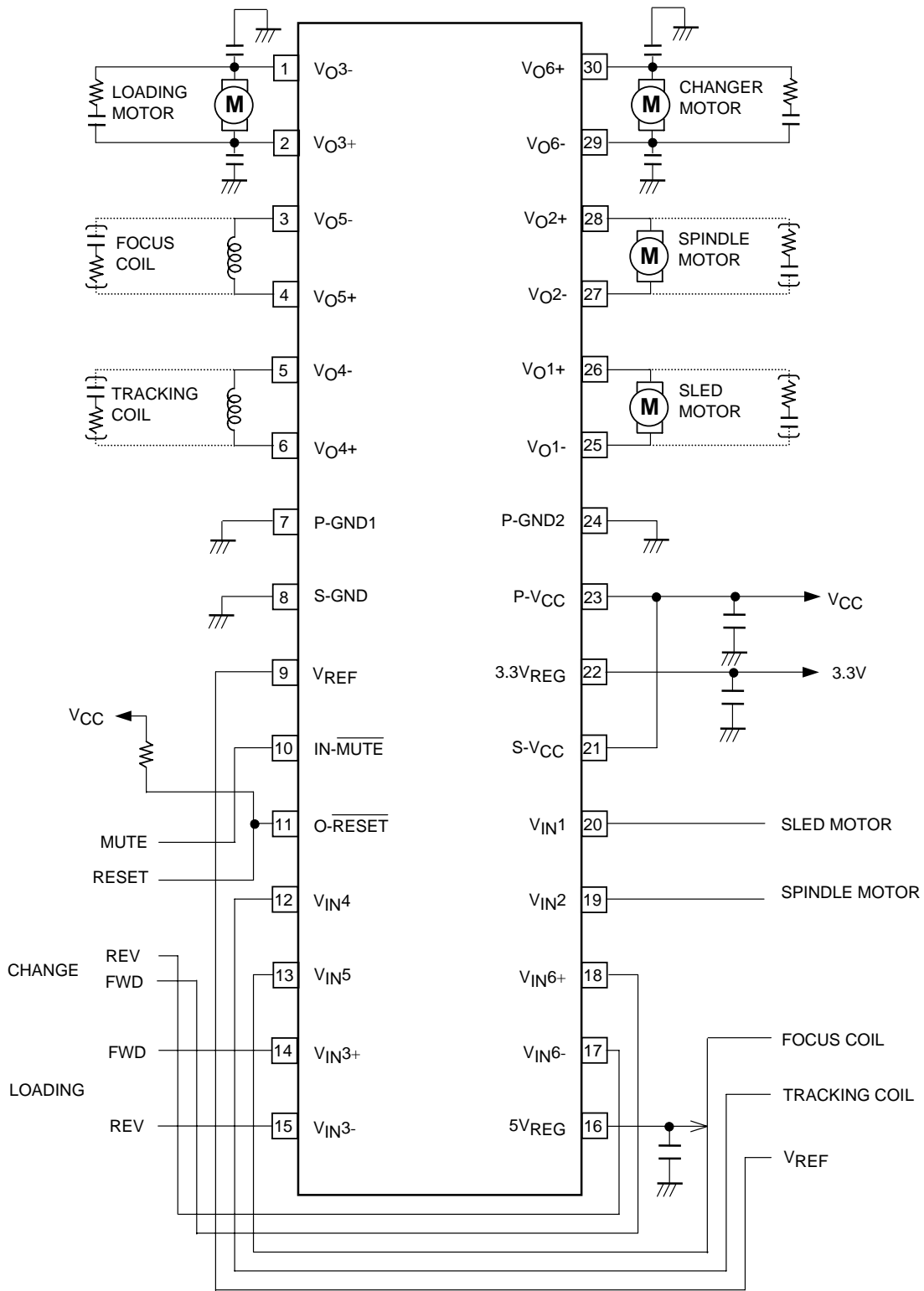
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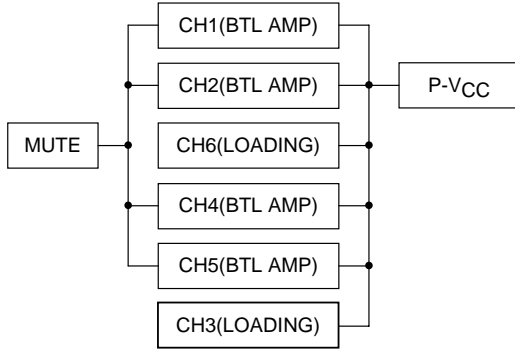
Pin Name	Pin Name	Pin No	Description	Equivalent Circuit Diagram
Input (Loading block)	V _{IN3-} V _{IN3+} V _{IN6-} V _{IN6+}	15 14 17 18	Each input pin	
Output (Loading block)	V _{O3+} V _{O3-} V _{O6+} V _{O6-}	2 1 30 29	Each output	
5V _{REG}	5V _{REG}	16	Output for 5V _{REG}	
3.3V _{REG}	3.3V _{REG}	22	Output for 3.3V _{REG}	

Sample Application Circuit



Note: When connecting a load to CH3 and CH6, set the output capacitor to 0.56 μ F or more and select the capacitor according to the setting. The capacitor to be used should be less in capacity fluctuation due to temperature.

Relation of MUTE and Power (P-VCC)



- * Connect S-VCC and P-VCC externally.
- * Connect P-GND and S-GND externally.

Various MUTE functions and output, 3.3V REG operation condition

	CH1, 2, 4, 5 (BTL-AMP)	CH3, 6 (LOADING)	3.3V _{REG} 5V _{REG}
With $\overline{\text{IN-MUTE}}$: L	OFF	-	OFF
With thermal shutdown operating	OFF	OFF	OFF
With V _{REF} lowering (0.7V or less)	OFF	-	-

- * (-) indicates no-operation for functions to which MUTE, thermal shutdown, and V_{REF} lowering correspond.
- * $\overline{\text{IN-MUTE}}$ operates for BTL-AMP (CH1, 2, 4, and 5) and 3.3V_{REF} and 5 V_{REF}.
- * V_{REF} lowering is effective for BTL-AMP only.

Operative for ((MUTE operation)) to BTL-AMP(CH1, 2, 4, 5) and 3.3V_{REF}, 5V_{REF}

IN-MUTE condition	BTL-AMP (CH1, 2, 4, 5)	3.3V _{REG} 5V _{REG}
H	ON	
L	OFF	

Operative for ((V_{REF} lowering)) to BTL-AMP

V _{REF} condition	BTL-AMP (CH1, 2, 4, 5)
V _{REF} > 0.7(V)	ON
V _{REF} < 0.7(V)	OFF

LOADING Block

V _{IN} ⁺ (FWD)	V _{IN} ⁻ (REV)	Loading output
L	L	Brake
	H	Reversed (V _O =-1.5×REV) *1
H	L	Forward (V _O = 1.5×FWD) *1
	H	(V _O =1.5×(VFO-VRE))

- * When the brake is applied, each “+” and “-” output voltage becomes V_{CC}/2.
- *1 FWD: V_{IN}6+, V_{IN}3+, REV: V_{IN}6-, V_{IN}3-.
- * L voltage is L<V_F(≈0.6V).
- * Gain of loading (CH3, 6) is 3.5dB(TYP).

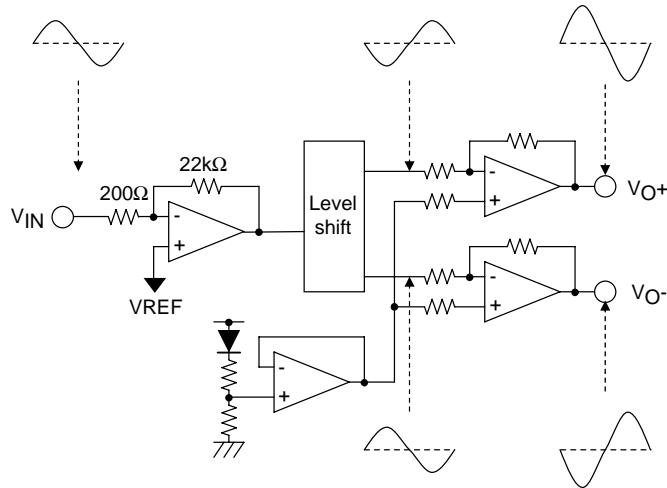
Reset function

IN-MUTE	V _{REF}	O-RESET
L	V _{REF} < 0.7V	L
	V _{REF} > 0.7V	L
H	V _{REF} < 0.7V	L
	V _{REF} > 0.7V	H

* O-RESET is an open collector output (NPN).

* O-RESET: L indicates that the NPN output is ON while O-RESET: H indicates that this output is OFF.

Relation of input and output (BTL-AMP)



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