



SANYO Semiconductors

DATA SHEET

LA6541 — Monolithic Linear IC For Compact Disk Four-Channel Bridge (BTL) Driver

Overview

The LA6541 is a 4-channel bridge (BTL) driver for CD players.

Functions

- Bridge-connection (BTL) power amplifier, 4 channels
- I_O max 700mA
- With muting function (Operable on all amplifier outputs of Amp 1 to Amp 8)
- 5.0V regulator built in (Output transistor connected externally)
- Reset circuit built in (Reset output delay time settable by using an external capacitor)
- Thermal shutdown circuit built in

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	P_d max	Specified substrate*	2.3	W
Maximum input voltage	V_{INB}		13	V
MUTE pin voltage	V_{MUTE}		13	V
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Substrate size : 114.3×76.1×1.5mm³, Material : glass epoxy.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Operating voltage	V_{CC}		5.6 to 13	V
Reset output source current	I_{ORH}		0 to 200	μA
Reset output sync current	I_{ORL}		0 to 2	mA

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LA6541

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 8.0\text{V}$, $V_{REF} = 2.5\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Overall						
No-load current drain 1	I_{CC1}	All amp outputs ON (MUTE HI)		20	40	mA
No-load current drain 2	I_{CC2}	All amp outputs OFF (MUTE LOW)		15	35	mA
Output offset voltage 1	V_{OF1}	Amp 1-2 (V_{O1} - V_{O2}), Amp 3-4 (V_{O3} - V_{O4})	-50		50	mV
Output offset voltage 2	V_{OF1}	Amp 5-6 (V_{O5} - V_{O6}), Amp 7-8 (V_{O7} - V_{O8})	-50		50	mV
Buffer input voltage range	I_{BIN}		1.5		$V_{CC}-1.5$	V
Input voltage rang	V_{IN}		1.0		$V_{CC}-1.5$	V
Output voltage source	V_{O1}	$R_L = 8.0\Omega$ *1	5.0	5.6		V
Output voltage sink	V_{O2}	$R_L = 8.0\Omega$ *2		1.8	2.4	V
Closed-circuit voltage gain	VG	Bridge amp		9		dB
Slew rate	SR			0.15		V/ μs
Mute ON voltage	VMUTE	*3		1.2		V
Power supply block (2SB632K used)						
Output voltage	V_{OUT1}	$I_O = 200\text{mA}$	4.75	5.0	5.25	V
Line regulation	ΔV_{OLN1}	$5.6\text{V} \leq V_{IN1} \leq 12\text{V}$		20	100	mV
Load regulation	ΔV_{OLD1}	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	150	mV
Reset block						
H reset output voltage	V_{ORH}	$I_{ORH} = 200\mu\text{A}$, Cd Pin open	4.73	4.98	5.23	V
L reset output voltage	V_{ORL}	$I_{ORL} = 2\text{mA}$, Cd-GND shorted		100	200	mV
Reset threshold voltage	V_{RT}	*4		4.3		V
Reset hysteresis voltage	V_{HYS}	*5	40	100	200	mV
Reset output delay time	td	Cd = $0.1\mu\text{F}$		10		ms

Note *1 : Voltage relative to GND when a load of 8Ω is connected across bridge amplifier outputs (source)

*2 : Voltage relative to GND when a load of 8Ω is connected across bridge amplifier outputs (sink)

*3 : MUTE HI supports all amplifier outputs ON ; MUTE LOW supports all amplifier outputs OFF.

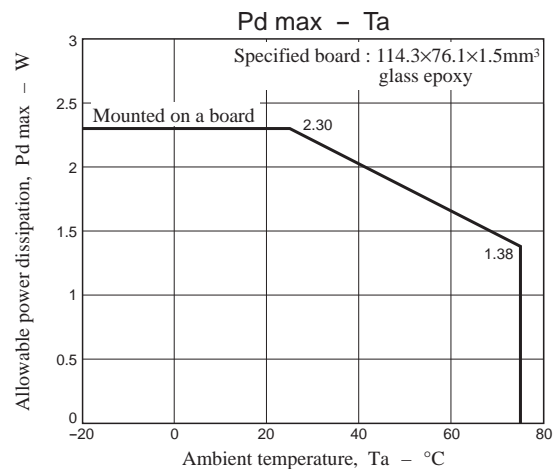
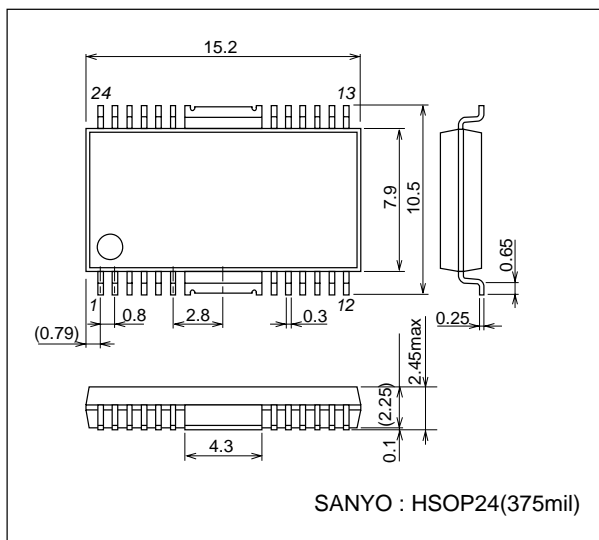
*4 : 5V supply voltage when the reset output is brought to LOW

*5 : Difference between 5V supply voltage when the reset output is brought to LOW and 5V supply voltage when the reset output is brought to HI

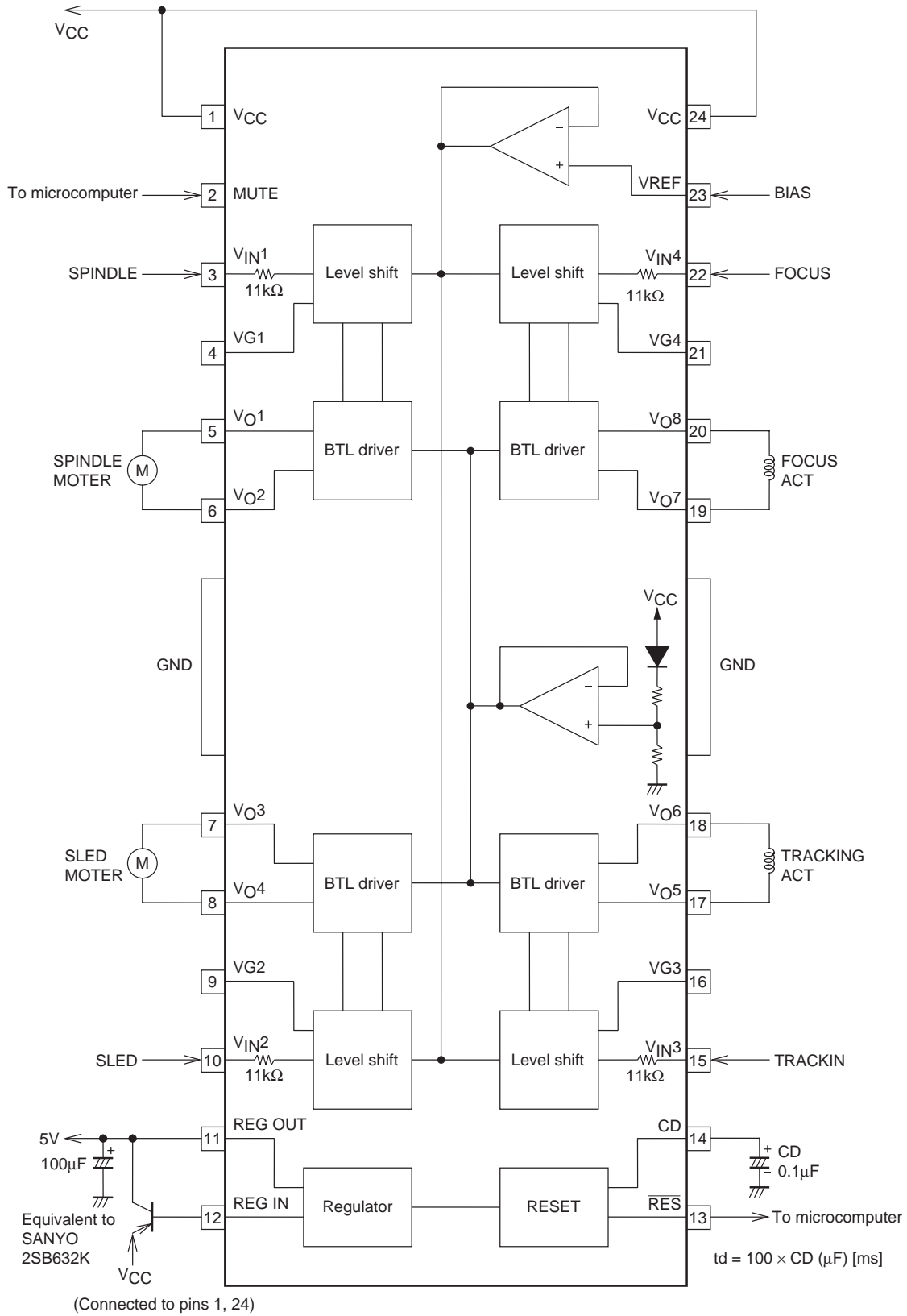
Package Dimensions

unit : mm (typ)

3227B



Block Diagram and Sample Application Circuit



LA6541

Pin Functions

Pin No.	Symbol	Pin descriptions
1	V _{CC}	Power supply (Shorted to pin 24)
2	MUTE	All BTL amplifier outputs ON/OFF
3	V _{IN1}	BTL AMP 1 input pin
4	VG1	BTL AMP 1 input pin (For gain adjustment)
5	V _{O1}	BTL AMP 1 input pin (Noninverting side)
6	V _{O2}	BTL AMP 1 input pin (Inverting side)
7	V _{O3}	BTL AMP 2 input pin (Inverting side)
8	V _{O4}	BTL AMP 2 input pin (Noninverting side)
9	VG2	BTL AMP 2 input pin (For gain adjustment)
10	V _{IN2}	BTL AMP 2 input pin
11	REG-OUT	External transistor collector (PNP) connection. 5V power supply output
12	REG-IN	External transistor (PNP) base connection
13	$\overline{\text{RES}}$	Reset output
14	CD	Reset output delay time setting (Capacitor connected externally)
15	V _{IN3}	BTL AMP 3 input pin
16	VG3	BTL AMP 3 input pin (For gain adjustment)
17	V _{O5}	BTL AMP 3 output pin (Noninverting side)
18	V _{O6}	BTL AMP 3 output pin (Inverting side)
19	V _{O7}	BTL AMP 4 output pin (Inverting side)
20	V _{O8}	BTL AMP 4 output pin (Noninverting side)
21	VG4	BTL AMP 4 output pin (For gain adjustment)
22	V _{IN4}	BTL AMP 4 output pin
23	VREF	Level shift circuit's reference voltage application
24	V _{CC}	Power supply (Shorted to pin 1)

Note : The Gnd (the lowest potential) must be located at the center of the pin assignment on the frame.

Pin Description

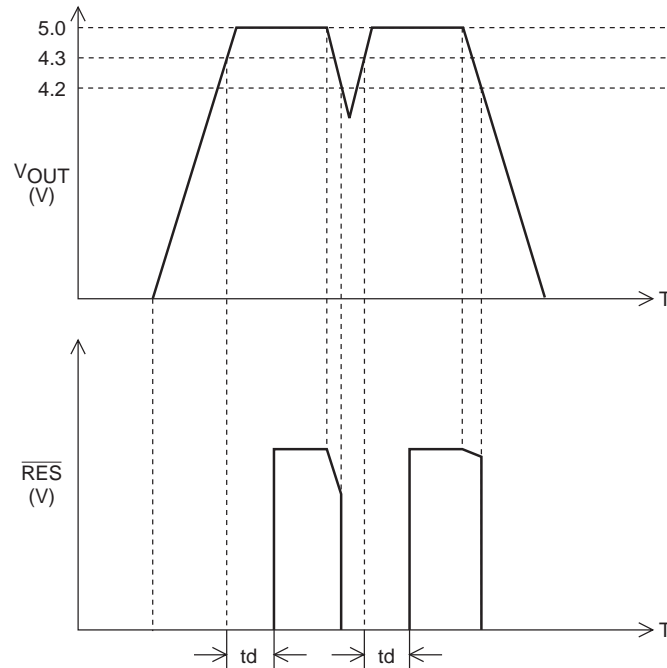
Pin No.	Symbol	Pin function	Description	Equivalent circuit
3 10 15 22 4 9 16 21	V_{IN1} V_{IN2} V_{IN3} V_{IN4} $VG1$ $VG2$ $VG3$ $VG4$	Input	Each input pin	
5, 6 7, 8 17, 18 19, 20	V_{O1}, V_{O2} V_{O3}, V_{O4} V_{O5}, V_{O6} V_{O7}, V_{O8}	Output	Each output pin	
2	MUTE	MUTE	MUTE	

Truth Table

Input	MUTE	CH1		CH2		CH3		CH4	
		V_{O1} (Amp 1)	V_{O2} (Amp 2)	V_{O3} (Amp 3)	V_{O4} (Amp 4)	V_{O5} (Amp 5)	V_{O6} (Amp 6)	V_{O7} (Amp 7)	V_{O8} (Amp 8)
H	H	H	L	L	H	H	L	L	H
	L	-	-	-	-	-	-	-	-
L	H	L	H	H	L	L	H	H	L
	L	-	-	-	-	-	-	-	-

* - : Amplifier output off

Reset operation



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