M66311P/FP

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

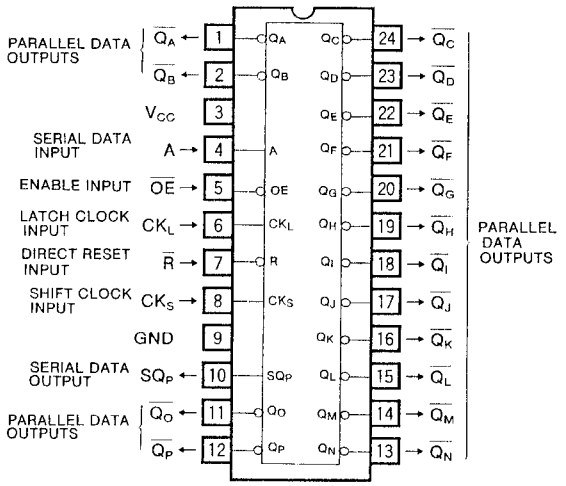
DESCRIPTION

M66311P/FP is a LED array driver having a 16bit serial-input and parallel output shiftregister function with direct coupled reset input and output latch function.
This product guarantees the output electric current of 24mA which is sufficient for anode common LED drive, capable of flowing 16bits continuously at the same time.
Parallel output is open drain output.
In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.
Furthermore, pin lay-out ensures the realization of an easy printed circuit.

FEATURES

- Anode common LED drive
- High output current
  all parallel output I_{OL}=24mA
  simultaneous lighting available
- Low power dissipation : 100μW/package (max)
  (V_{CC}=5V, Ta=25℃, quiescent state)
- High noise margin
  schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output
  (except serial data output)
- Wide operating temperature range
  : Ta=−40~+85℃
- Pin lay-out facilitates printed circuit wiring. (This lay-out facilitates cascade connection and LED connection.)

PIN CONFIGURATION (TOP VIEW)

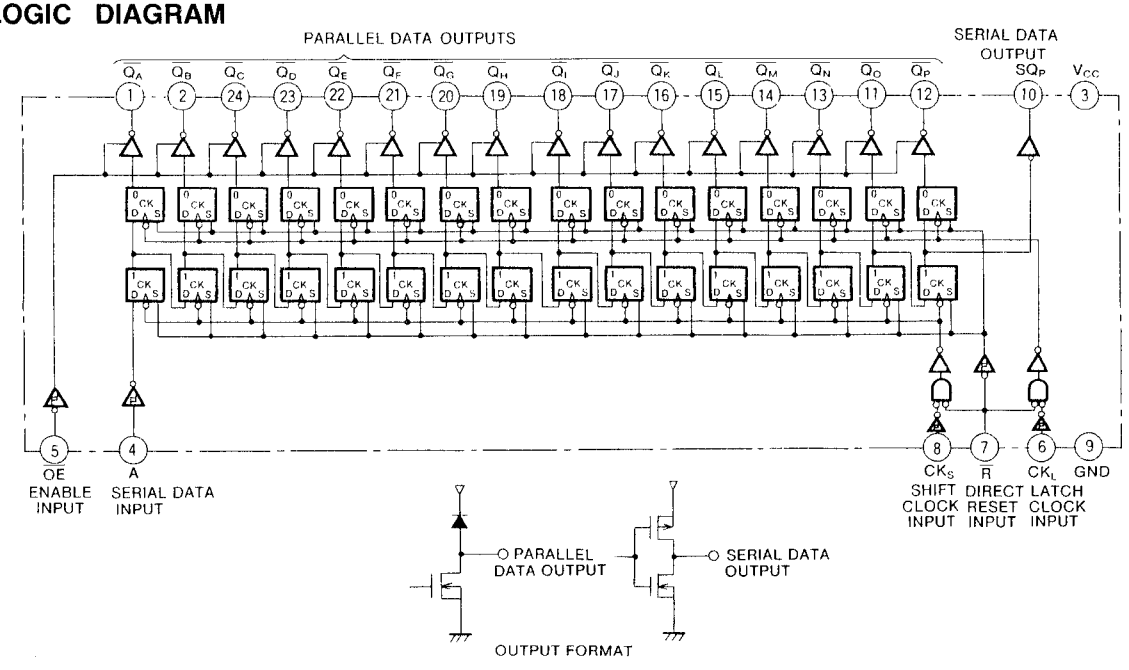


Outline 24P4D
24P2N-B

APPLICATION

LED array drive of BUTTON TELEPHONE
LED array drive of ERASER of a PPC copier
Other various LED modules

LOGIC DIAGRAM



16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

FUNCTIONAL DESCRIPTION

As M66311P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CKs and latch clock input CK_L are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shifting registers one by one when a pulse is impressed to CK_S. When A is "H", the signal of "L" shifts.

When the pulse is impressed to CK_L, the contents of the shifting register at that time are stored in a latching register, and they appear in the outputs from $\overline{Q_A}$~$\overline{Q_P}$.

Outputs from $\overline{Q_A}$~$\overline{Q_P}$ are open drain outputs.

To extend the number of bits, use the serial data output SQ_P which shows the output of the shifting register of the 16th bit.

If CK_S and CK_L are connected, the state of the shifting register with one clock delay is outputted to $\overline{Q_A}$~$\overline{Q_P}$.

When reset input $\overline{R}$ is changed to "L", $\overline{Q_A}$~$\overline{Q_P}$ and SQ_P are reset. In this case, shifting and latching registers are set.

If "H" is impressed to output enable input $\overline{OE}$, $\overline{Q_A}$ ~ $\overline{Q_P}$ reaches the high impedance state, but SQ_P does not reach the high impedance state. Furthermore, change in $\overline{OE}$ does not affect shift operation.

FUNCTION TABLE (Note : 1)

Operation mode		Input					PARALLEL DATA Output																Serial data output SQ_P	Remarks
		$\overline{R}$	CK_S	CK_L	A	$\overline{OE}$	$\overline{Q_A}$	$\overline{Q_B}$	$\overline{Q_C}$	$\overline{Q_D}$	$\overline{Q_E}$	$\overline{Q_F}$	$\overline{Q_G}$	$\overline{Q_H}$	$\overline{Q_I}$	$\overline{Q_J}$	$\overline{Q_K}$	$\overline{Q_L}$	$\overline{Q_M}$	$\overline{Q_N}$	$\overline{Q_O}$	$\overline{Q_P}$		
Reset		L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	—
Shift latch operation	Shift t1	H	↑	X	H	L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	$\overline{Q_C}^0$	$\overline{Q_D}^0$	$\overline{Q_E}^0$	$\overline{Q_F}^0$	$\overline{Q_G}^0$	$\overline{Q_H}^0$	$\overline{Q_I}^0$	$\overline{Q_J}^0$	$\overline{Q_K}^0$	$\overline{Q_L}^0$	$\overline{Q_M}^0$	$\overline{Q_N}^0$	$\overline{Q_O}^0$	$\overline{Q_P}^0$	$q_O{}^0$	Output lighting "H"
	Latch t2	H	X	↑	X	L	L	$q_A{}^0$	$q_B{}^0$	$q_C{}^0$	$q_D{}^0$	$q_E{}^0$	$q_F{}^0$	$q_G{}^0$	$q_H{}^0$	$q_I{}^0$	$q_J{}^0$	$q_K{}^0$	$q_L{}^0$	$q_M{}^0$	$q_N{}^0$	$q_O{}^0$	$q_O{}^0$	
	Shift t1	H	↑	X	L	L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	$\overline{Q_C}^0$	$\overline{Q_D}^0$	$\overline{Q_E}^0$	$\overline{Q_F}^0$	$\overline{Q_G}^0$	$\overline{Q_H}^0$	$\overline{Q_I}^0$	$\overline{Q_J}^0$	$\overline{Q_K}^0$	$\overline{Q_L}^0$	$\overline{Q_M}^0$	$\overline{Q_N}^0$	$\overline{Q_O}^0$	$\overline{Q_P}^0$	$q_O{}^0$	Output lights-out "L"
	Latch t2	H	X	↑	X	L	Z	$q_A{}^0$	$q_B{}^0$	$q_C{}^0$	$q_D{}^0$	$q_E{}^0$	$q_F{}^0$	$q_G{}^0$	$q_H{}^0$	$q_I{}^0$	$q_J{}^0$	$q_K{}^0$	$q_L{}^0$	$q_M{}^0$	$q_N{}^0$	$q_O{}^0$	$q_O{}^0$	
Output disable		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_P	—

Note 1 : ↑ : Change from low-level to high-level
$\overline{Q}^0$: Output state $\overline{Q}$ before CK_L changed
X : Irrelevant
q^0 : Contents of shift register before CK_S changed
q : Contents of shift register
t_1, t_2 : t_2 is set after t_1 is set
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (Ta=−40~+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7.0	V
V_I	Input voltage			−0.5~V_{CC}+0.5	V
V_O	Output voltage			−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current per output pin	$\overline{Q_A}$~$\overline{Q_P}$		50	mA
		SQ_P		±25	
I_{CC}	Supply/GND current		V_{CC}, GND	−20, +410	mA
P_d	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			−65~+150	℃

Note 2 : M66311FP ; T_a=−40~+70℃, T_a=70~85℃ are derated at −6mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Topr	Operating temperature range	−40		+85	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				T_a=25℃			T_a=−40~+85℃		
				Min	Typ	Max	Min	Max	
V_{T+}	Positive-going threshold voltage	V_O=0.1V, V_{CC}−0.1V $\|I_O\|$=20μA		0.35×V_{CC}		0.7×V_{CC}	0.35×V_{CC}	0.7×V_{CC}	V
V_{T-}	Negative-going threshold voltage	V_O=0.1V, V_{CC}−0.1V $\|I_O\|$=20μA		0.2×V_{CC}		0.55×V_{CC}	0.2×V_{CC}	0.55×V_{CC}	V
V_{OL}	Low-level output voltage $\overline{Q_A}$~$\overline{Q_P}$	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=24mA			0.44		0.53	
		Note3	I_{OL}=40mA			0.73		0.94	
V_{OH}	High-level output voltage SQ_P	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH}=−4mA	3.83			3.66		
V_{OL}	Low-level output voltage SQ_P	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=4mA			0.44		0.53	
I_{IH}	High-level input current	V_I=V_{CC}, V_{CC}=5.5V				0.5		5.0	μA
I_{IL}	Low-level input current	V_I=GND, V_{CC}=5.5V				−0.5		−5.0	μA
I_O	Maximum output leakage current $\overline{Q_A}$~$\overline{Q_P}$	V_I=V_{T+}, V_{T-} V_{CC}=5.5V	V_O=V_{CC}			1.0		10.0	μA
			V_O=GND			−1.0		−10.0	
I_{CC}	Quiescent supply current	V_I=V_{CC}, GND, V_{CC}=5.5V				20.0		200.0	μA

Note 3 : M66311 is used under the condition of an output current I_{OL}=40mA, the number of simultaneous drive outputs is restricted as shown in the Duty Cycle−I_{OL} of Standard characteristics.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V)

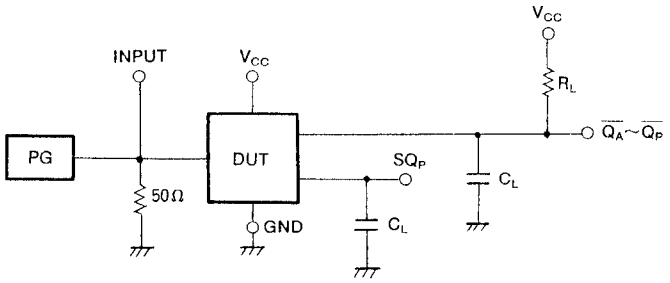
Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40∼+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L=50pF R_L= 1 kΩ (Note 5)	5			4		MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_S-SQ_P)				100		130	ns
t_{PHL}					100		130	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$-SQ_P)				100		130	ns
t_{PLZ}	Low-level to high-level output propagation time ($\overline{R}$-$\overline{Q_A}$∼$\overline{Q_P}$)				150		200	ns
t_{PZL}	Low-level to high-level and high-level to low-level output propagation time (CK_L−$\overline{Q_A}$∼$\overline{Q_P}$)				100		130	ns
t_{PLZ}					150		200	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$−$\overline{Q_A}$∼$\overline{Q_P}$)				100		130	ns
t_{PLZ}					150		200	ns
C_I	Input Capacitance				10		10	pF
C_O	Output Capacitance	$\overline{OE}$=V_{CC}			15		15	pF
C_{PD}	Power dissipation Capacitance (Note 4)			5				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D=C_{PD}\cdot V_{CC}^2\cdot f_I+I_{CC}\cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC}= 5 V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_w	CK_S, CK_L, $\overline{R}$ pulse width	(Note 5)	100			130		ns
t_{su}	A setup time with respect to CK_S		100			130		ns
t_{su}	CK_S setup time with respect to CK_L		100			130		ns
t_h	A hold time with respect to CK_S		10			15		ns
t_{rec}	$\overline{R}$, recovery time with respect to CK_S, CK_L		50			70		ns

Note 5 : Test Circuit

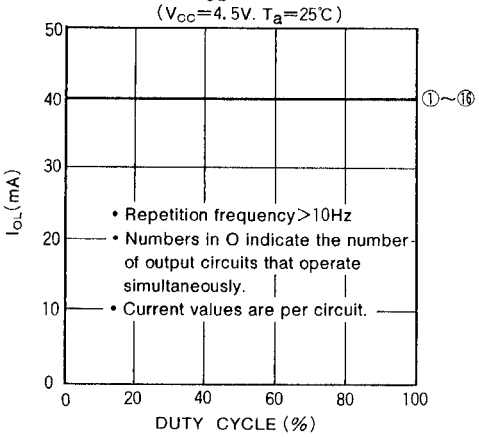


(1) The pulse generator (PG) has the following characteristics (10%∼90%) : tr =6ns, tf=6ns

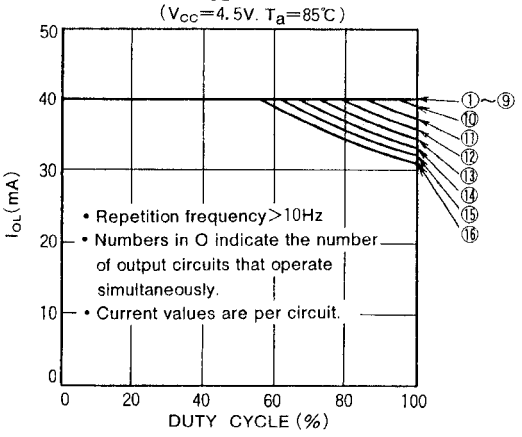
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TYPICAL CHARACTERISTICS

DUTY CYCLE–I_{OL} CHARACTERISTICS
(V_{CC}=4.5V, T_a=25℃)



DUTY CYCLE–I_{OL} CHARACTERISTICS
(V_{CC}=4.5V, T_a=85℃)



TIMING DIAGRAM