CY7C401/CY7C403
CY7C402/CY7C404

64 x 4 Cascadable FIFO
64 x 5 Cascadable FIFO

Features

- **64 x 4 (CY7C401 and CY7C403)**
  64 x 5 (CY7C402 and CY7C404)
  High-speed first-in first-out memory (FIFO)
- **Processed with high-speed CMOS for optimum speed/power**
- **25-MHz data rates**
- **50-ns bubble-through time—25 MHz**
- **Expandable in word width and/or length**
- **5-volt power supply ± 10% tolerance, both commercial and military**
- **Independent asynchronous inputs and outputs**
- **TTL-compatible interface**
- **Output enable function available on CY7C403 and CY7C404**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Pin compatible with MMI 67401A/67402A**

Functional Description

The CY7C401 and CY7C403 are asynchronous first-in first-out (FIFOs) organized as 64 four-bit words. The CY7C402 and CY7C404 are similar FIFOs organized as 64 five-bit words. Both the CY7C403 and CY7C404 have an output enable (OE) function.

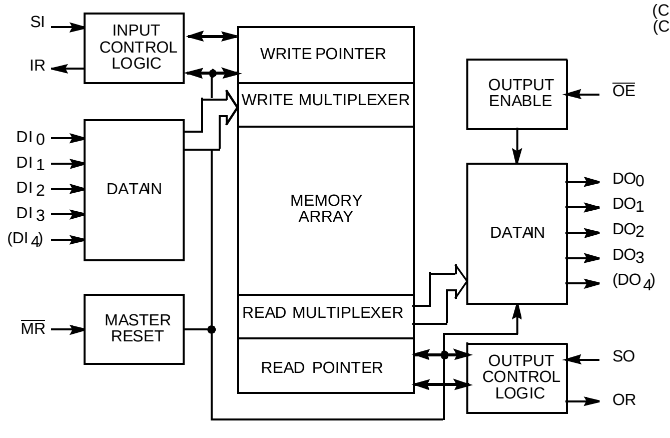
The devices accept 4- or 5-bit words at the data input (DI_0 – DI_n) under the control of the shift in (SI) input. The stored words stack up at the output (DO_0 – DO_n) in the order they were entered. A read command on the shift out (SO) input causes the next to last word to move to the output and all data shifts down once in the stack. The input ready (IR) signal acts as a flag to indicate when the input is ready to accept new data (HIGH), to indicate when the FIFO is full (LOW), and to provide a signal for a cascading. The output ready (OR) signal is a flag to indicate the output contains valid data (HIGH), to indicate the FIFO is empty (LOW), and to provide a signal for cascading.

Parallel expansion for wider words is accomplished by logically ANDing the IR and OR signals to form composite signals.

Serial expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The IR pin of the receiving device is connected to the SO pin of the sending device, and the OR pin of the sending device is connected to the SI pin of the receiving device.

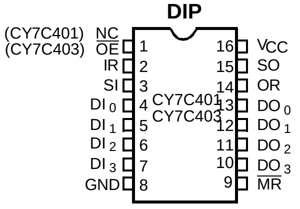
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The 25-MHz operation makes these FIFOs ideal for high-speed communication and controller applications.

Logic Block Diagram

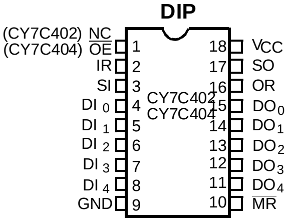

SI
IR
INPUT CONTROL LOGIC
WRITE POINTER
WRITE MULTIPLEXER
OUTPUT ENABLE
OE
DI 0
DI 1
DI 2
DI 3
(DI 4)
DATAIN
MEMORY ARRAY
DATAIN
DO0
DO1
DO2
DO3
(DO 4)
MR
MASTER RESET
READ MULTIPLEXER
READ POINTER
OUTPUT CONTROL LOGIC
SO
OR

C401–1

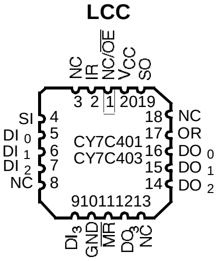
Pin Configurations


DIP
(CY7C401) NC
(CY7C403) OE
IR
SI
DI 0
DI 1
DI 2
DI 3
GND
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
SO
OR
DO 0
DO 1
DO 2
DO 3
MR
CY7C401
CY7C403

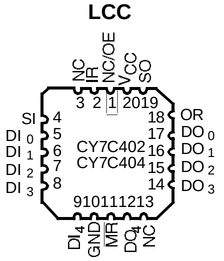
C401–2


DIP
(CY7C402) NC
(CY7C404) OE
IR
SI
DI 0
DI 1
DI 2
DI 3
DI 4
GND
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
VCC
SO
OR
DO0
DO1
DO2
DO3
DO4
MR
CY7C402
CY7C404

C401–4


LCC
NC
IR
NC/OE
VCC
SO
3 2 1 20 19
SI 4
DI 0 5
DI 1 6
DI 2 7
NC 8
18 NC
17 OR
16 DO 0
15 DO 1
14 DO 2
CY7C401
CY7C403
9 10 11 12 13
DI3
GND
MR
DO3
NC

C401–3


LCC
NC
IR
NC/OE
VCC
SO
3 2 1 20 19
SI 4
DI 0 5
DI 1 6
DI 2 7
DI 3 8
18 OR
17 DO 0
16 DO 1
15 DO 2
14 DO 3
CY7C402
CY7C404
9 10 11 12 13
DI4
GND
MR
DO4
NC

C401–5

Selection Guide

		7C401/2–5	7C40X–10	7C40X–15	7C40X–25
Operating Frequency (MHz)		5	10	15	25
Maximum Operating Current (mA)	Commercial	75	75	75	75
	Military		90	90	90

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March 1986 – Revised April 1995

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	–0.5V to +7.0V
DC Input Voltage	–3.0V to +7.0V
Power Dissipation	1.0W
Output Current, into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	–55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[2]

				7C40X–10, 15, 25		
Parameter	**Description**	**Test Conditions**		**Min.**	**Max.**	**Unit**
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	6.0	V
V_{IL}	Input LOW Voltage			–3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	µA
V_{CD}[3]	Input Diode Clamp Voltage[3]					
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5V Output Disabled (CY7C403 and CY7C404)		–50	+50	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		75	mA
			Military		90	mA

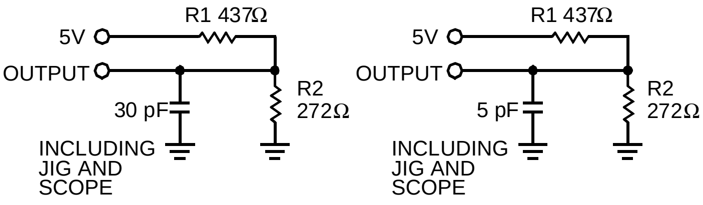
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

1. T_A is the “instant on” case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to –3V dc input levels and –5V undershoot pulses of less than 10 ns (measured at 50% output).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



(a) (b)

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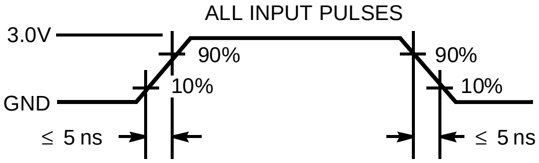

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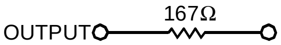
Equivalent to: THÉVENIN EQUIVALENT



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Switching Characteristics Over the Operating Range[2, 6]

Parameter	Description	Test Conditions	7C401–5 7C402–5		7C40X–10		7C40X–15		7C40X–25[7]		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 8		5		10		15		25	MHz
t_{PHSI}	SI HIGH Time		20		20		20		11		ns
t_{PLSI}	SO LOW Time		45		30		25		20		ns
t_{SSI}	Data Set-Up to SI	Note 9	0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 9	60		40		30		20		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			75		40		35		21/22	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			75		45		40		28/30	ns
t_{PHSO}	SO HIGH Time		20		20		20		11		ns
t_{PLSO}	SO LOW Time		45		25		25		20		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			75		40		35		19/21	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			80		55		40		34/37	ns
t_{SOR}	Data Set-Up to OR HIGH		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		ns
t_{BT}	Bubble-Through Time			200	10	95	10	65	10	50/60	ns
t_{SIR}	Data Set-Up to IR	Note 10	5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 10	30		30		30		20		ns
t_{PIR}	Input Ready Pulse HIGH		20		20		20		15		ns
t_{POR}	Output Ready Pulse HIGH		20		20		20		15		ns
t_{PMR}	MR Pulse Width		40		30		25		25		ns
t_{DSI}	MR HIGH to SI HIGH		40		35		25		10		ns
t_{DOR}	MR LOW to OR LOW			85		40		35		35	ns
t_{DIR}	MR LOW to IR HIGH			85		40		35		35	ns
t_{LZMR}	MR LOW to Output LOW	Note 11		50		40		35		25	ns
t_{OOE}	Output Valid from OE LOW			—		35		30		20	ns
t_{HZOE}	Output High Z from OE HIGH	Note 12		—		30		25		15	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Loads and Waveforms.
7. Commercial/Military
8. $I/f_O > t_{PHSI} + t_{DHIR}$, $I/f_O > t_{PHSO} + t_{DHOR}$
9. t_{SSI} and t_{HSI} apply when memory is not full.
10. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
11. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.
12. HIGH-Z transitions are referenced to the steady-state V_{OH} –500 mV and V_{OL} +500 mV levels on the output. t_{HZOE} is tested with 5-pF load capacitance as in part (b) of AC Test Loads and Waveforms.

Operational Description

Concept

Unlike traditional FIFOs, these devices are designed using a dual-port memory, read and write pointer, and control logic. The read and write pointers are incremented by the SO and SI respectively. The availability of an empty space to shift in data is indicated by the IR signal, while the presence of data at the output is indicated by the OR signal. The conventional concept of bubble-through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an OR signal. The output enable ($\overline{OE}$) signal provides the capability to OR tie multiple FIFOs together on a common bus.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset (MR) signal. This causes the FIFO to enter an empty condition signified by the OR signal being LOW at the same time the IR signal is HIGH. In this condition, the data outputs ($DO_0 – DO_n$) will be in a LOW state.

Shifting Data In

Data is shifted in on the rising edge of the SI signal. This loads input data into the first word location of the FIFO. On the falling edge of the SI signal, the write pointer is moved to the next word position and the IR signal goes HIGH, indicating the readiness to accept new data. If the FIFO is full, the IR will remain LOW until a word of data is shifted out.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of the SO signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the OR signal will go HIGH. If data is not present, the OR signal will stay LOW indicating the FIFO is empty. Upon the rising edge of SO, the OR signal goes LOW. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

Bubble-Through

Two bubble-through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the OR flag goes HIGH, indicating valid data at the output.

The second bubble-through condition occurs when the device is full. Shifting data out creates an empty location that propagates to the input. After a delay, the IR flag goes HIGH. If the SI signal is HIGH at this time, data on the input will be shifted in.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

When this violation occurs, the operation of the FIFO is unpredictable. It must then be reset, and all data is lost.

Application of the 7C403–25/7C404–25 at 25 MHz

Application of the CY7C403 or CY7C404 Cypress CMOS FIFOs requires knowledge of characteristics that are not easily specified in a datasheet, but which are necessary for reliable operation under all conditions, so we will specify them here.

When an empty FIFO is filled with initial information at maximum “shift in” SI frequency, followed by immediate shifting out of the data also at maximum “shift out” SO frequency, the designer must be aware of a window of time which follows the initial rising edge of the OR signal, during which time the SO signal is not recognized. This condition exists only at high-speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full-frequency operation, but rather delays the full 25-MHz operation until after the window has passed.

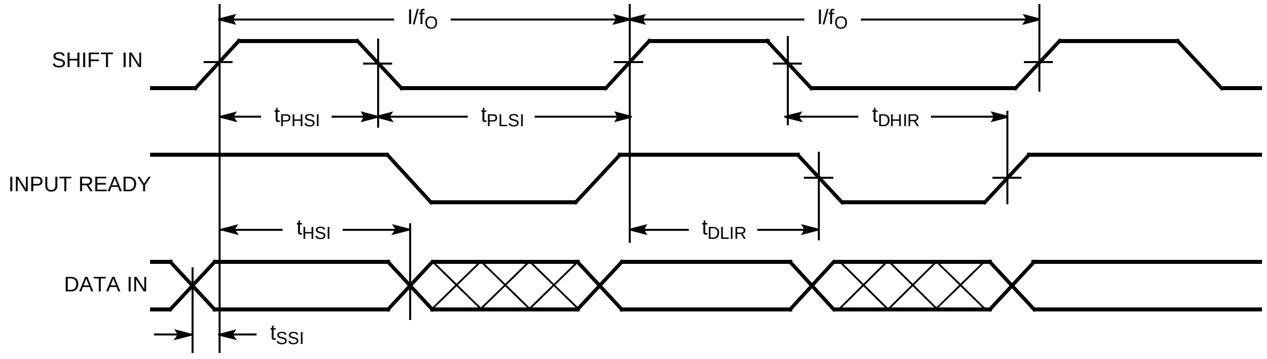
There are several implementation techniques for managing the window so that all SO signals are recognized:

1. The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay of 40 ns “initiated by the SI signal only when the FIFO is empty” to inhibit or gate the SO activity. However, this requires that the SO operation be at least temporarily synchronized with the input SI operation. In synchronous applications this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is more than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Cypress FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO 40 ns from the rising edge of the initial OR signal. This however involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from an empty condition and therefore requires the knowledge of IR and SI conditions as well as SO.
4. Handshaking with the OR signal is a third method of avoiding the window in question. With this technique the rising edge of SO, or the fact that SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This ensures that the SO pulse that is initiated in the window will be automatically extended long enough to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the SO signal is most appropriate because data is guaranteed to be stable prior to and after the SO leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

Any of the above solutions will ensure the correct operation of a Cypress FIFO at 25 MHz. The specific implementation is left to the designer and is dependent on the specific application needs.

Switching Waveforms

Data In Timing Diagram


I/f$_O$
I/f$_O$
SHIFT IN
t_{PHSI}
t_{PLSI}
t_{DHIR}
INPUT READY
t_{HSI}
t_{DLIR}
DATA IN
t_{SSI}

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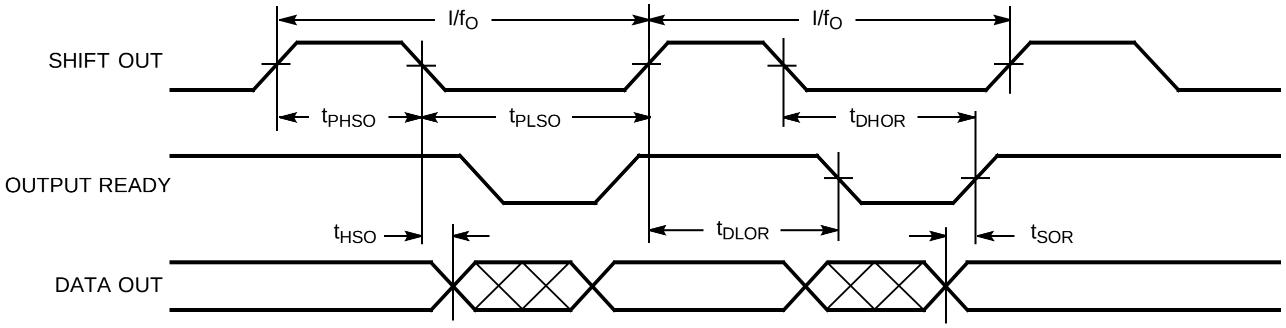
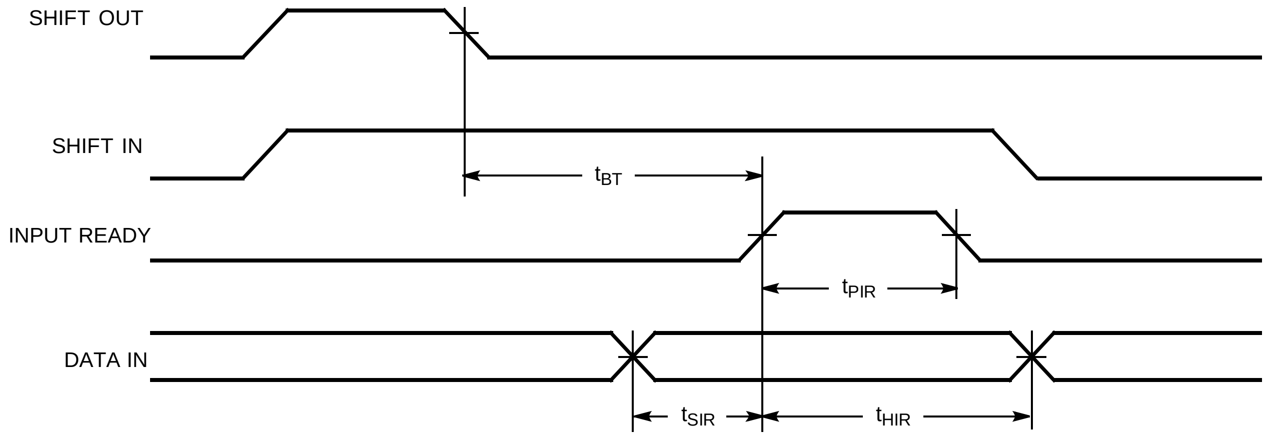
Data Out Timing Diagram


I/f$_O$
I/f$_O$
SHIFT OUT
t_{PHSO}
t_{PLSO}
t_{DHOR}
OUTPUT READY
t_{HSO}
t_{DLOR}
t_{SOR}
DATA OUT

C401–10

Bubble Through, Data Out To Data In Diagram


SHIFT OUT
SHIFT IN
t_{BT}
INPUT READY
t_{PIR}
DATA IN
t_{SIR}
t_{HIR}

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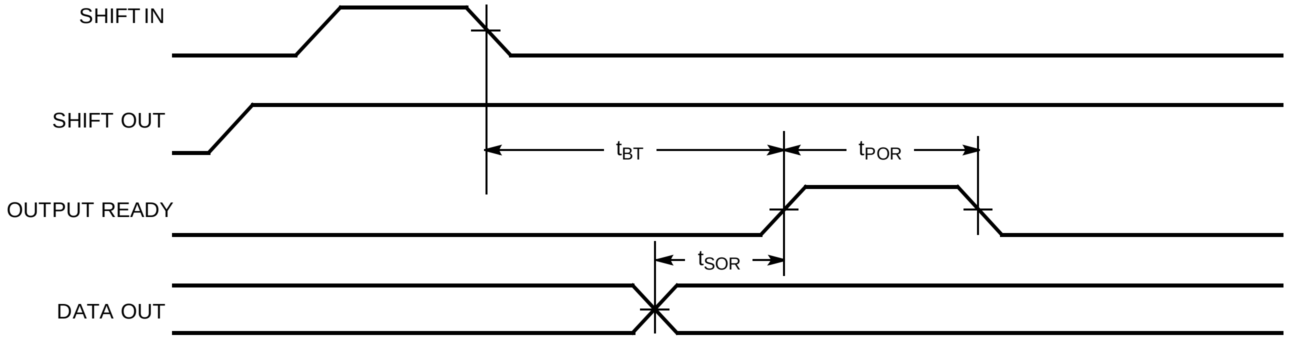
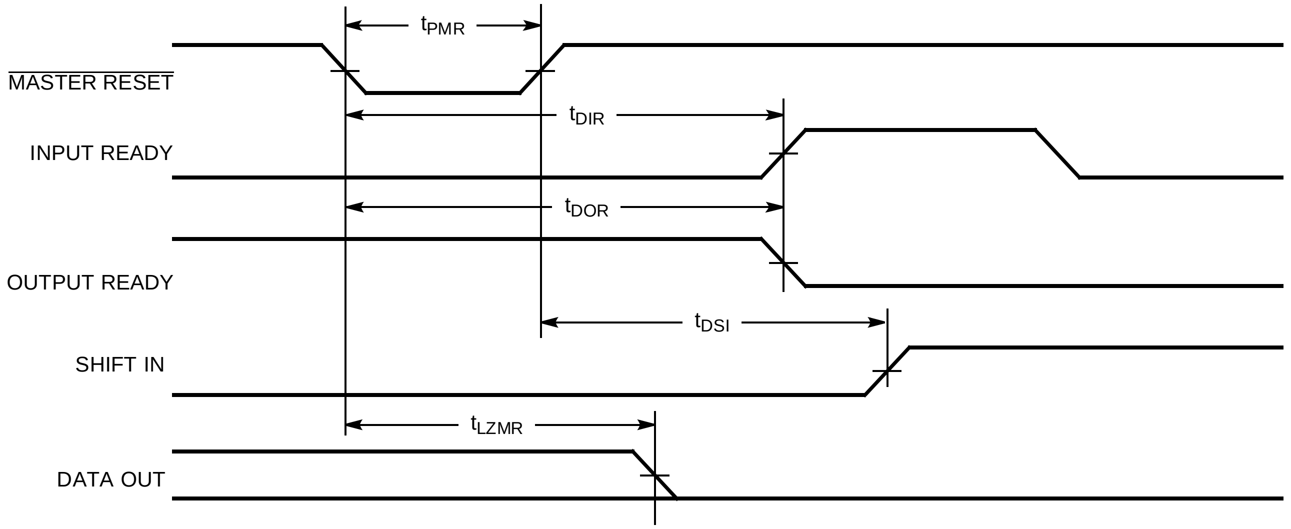
Switching Waveforms (continued)

Bubble Through, Data In To Data Out Diagram


SHIFT IN
SHIFT OUT
OUTPUT READY
DATA OUT
t_{BT}
t_{POR}
t_{SOR}

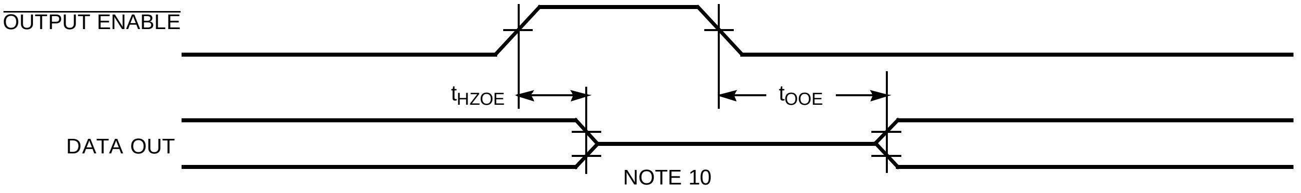
C401–12

Master Reset Timing Diagram


$\overline{\text{MASTER RESET}}$
INPUT READY
OUTPUT READY
SHIFT IN
DATA OUT
t_{PMR}
t_{DIR}
t_{DOR}
t_{DSI}
t_{LZMR}

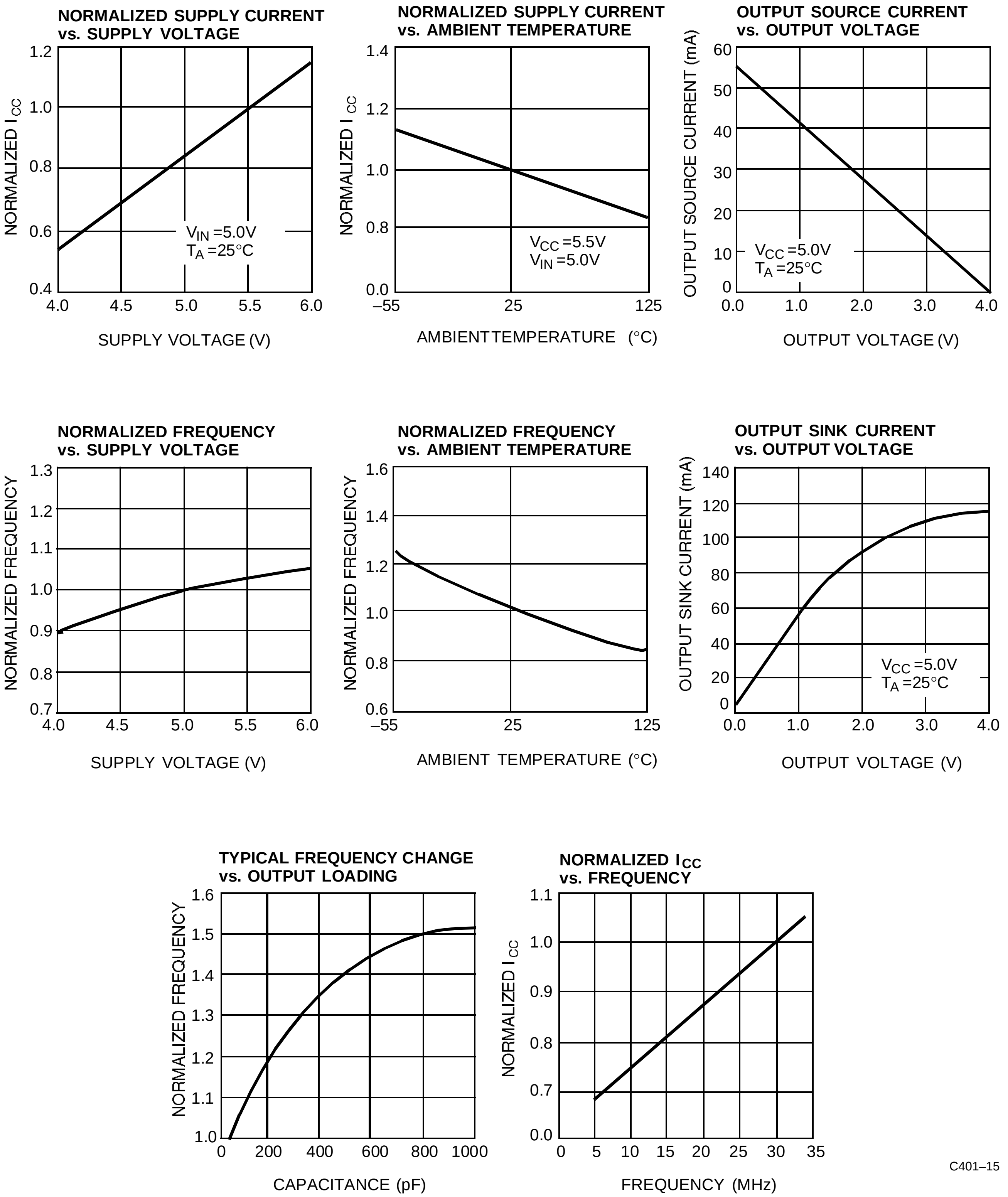
C401–13

Output Enable Timing Diagram


$\overline{\text{OUTPUT ENABLE}}$
DATA OUT
t_{HZOE}
t_{OOE}
NOTE 10

C401–14

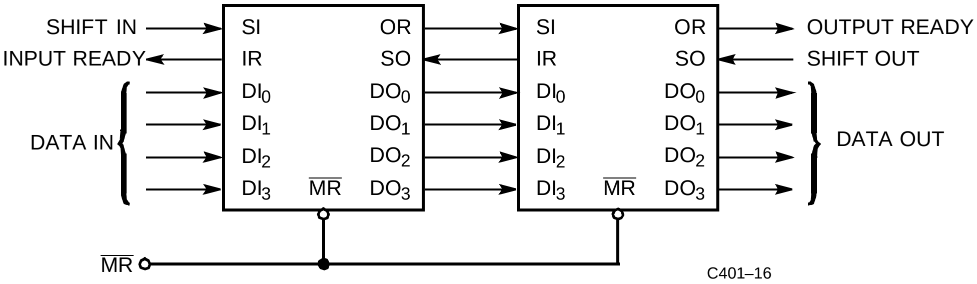
Typical DC and AC Characteristics



C401–15

FIFO Expansion[13, 14, 15, 16, 17]

128 x 4 Application[18]


SHIFT IN
INPUT READY
DATA IN
SI
IR
DI0
DI1
DI2
DI3
MR
OR
SO
DO0
DO1
DO2
DO3
OUTPUT READY
SHIFT OUT
DATA OUT
MR
C401–16

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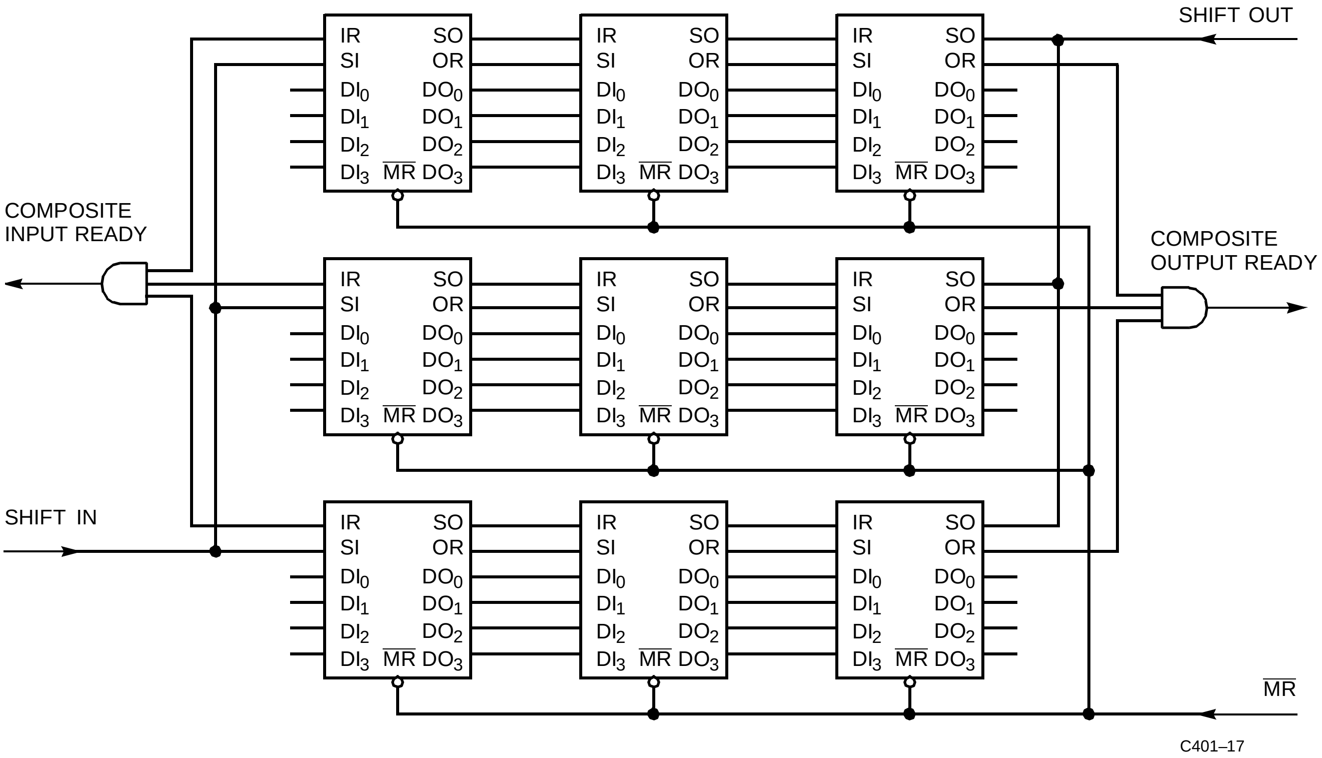
192 x 12 Application[19]


SHIFT OUT
COMPOSITE INPUT READY
COMPOSITE OUTPUT READY
SHIFT IN
MR
IR
SI
DI0
DI1
DI2
DI3
MR
SO
OR
DO0
DO1
DO2
DO3
C401–17

Notes:

13. When the memory is empty, the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
14. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data, and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid, stable data on the outputs.
15. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
16. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH, then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
17. All Cypress FIFOs will cascade with other Cypress FIFOs. However, hey may not cascade with pin-compatible FIFOs from other manufacturers.
18. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
19. FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite input and output ready flags. This need is due to the variation of delays of the FIFOs.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
5	CY7C401–5PC	P1	16-Lead (300-Mil) Molded DIP	Commercial
10	CY7C401–10DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–10PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–10DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C401–15DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–15PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–15DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C401–25DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–25PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–25DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
5	CY7C402–5PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
10	CY7C402–10DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–10PC	P3	20-Pin Square Leadless Chip Carrier	
	CY7C402–10DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C402–15DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–15PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C402–15DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C402–25DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–25PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C402–25DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information (continued)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C403–10DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–10PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–10DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C403–15DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–15PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–15DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C403–25DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–25PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–25DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C404–10DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–10PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–10DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C404–15DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–15PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–15DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C404–25DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–25PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–25DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–25LMB	L61	20-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
f_O	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{SSI}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{DLIR}	7, 8, 9, 10, 11
t_{DHIR}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{DLOR}	7, 8, 9, 10, 11
t_{DHOR}	7, 8, 9, 10, 11
t_{SOR}	7, 8, 9, 10, 11
t_{HSO}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{SIR}	7, 8, 9, 10, 11
t_{HIR}	7, 8, 9, 10, 11
t_{PIR}	7, 8, 9, 10, 11
t_{POR}	7, 8, 9, 10, 11
t_{PMR}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11
t_{LZMR}	7, 8, 9, 10, 11
t_{OOE}	7, 8, 9, 10, 11
t_{HZOE}	7, 8, 9, 10, 11

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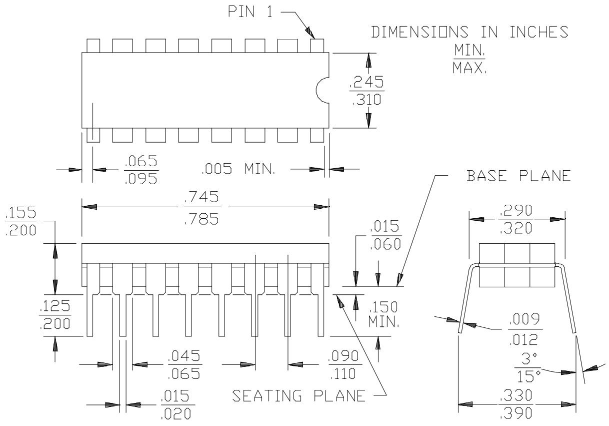
Package Diagrams

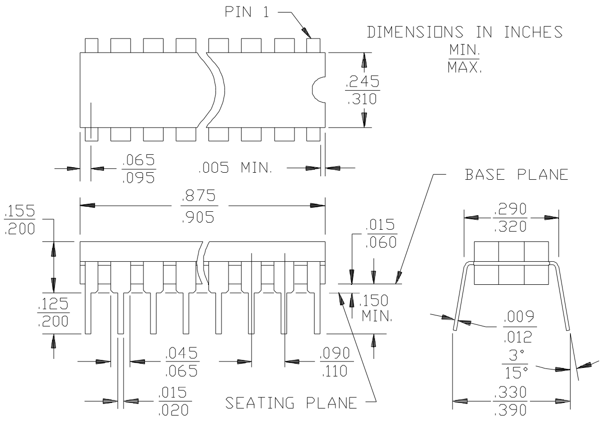
16-Lead (300-Mil) CerDIP D2

MIL-STD-1835 D-2 Config.A


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
.245
.310
.065
.095
.005 MIN.
BASE PLANE
.745
.785
.155
.200
.015
.060
.290
.320
.125
.200
.150
MIN.
.009
.012
3°
15°
.045
.065
.090
.110
.015
.020
SEATING PLANE
.330
.390

18-Lead (300-Mil) CerDIP D4

MIL-STD-1835 D-8 Config.A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DIMENSIONS IN INCHES
MIN.
MAX.
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.310
.065
.095
.005 MIN.
BASE PLANE
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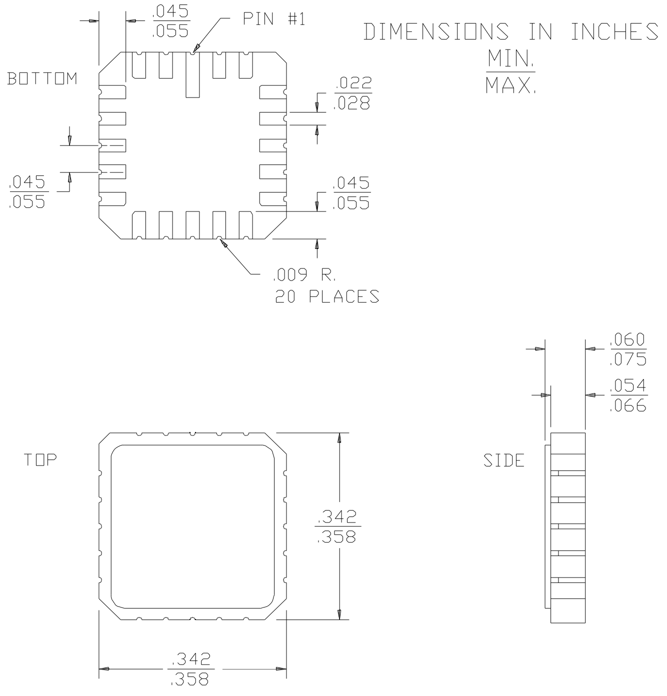
.905
.155
.200
.015
.060
.290
.320
.125
.200
.150
MIN.
.009
.012
3°
15°
.045
.065
.090
.110
.015
.020
SEATING PLANE
.330
.390

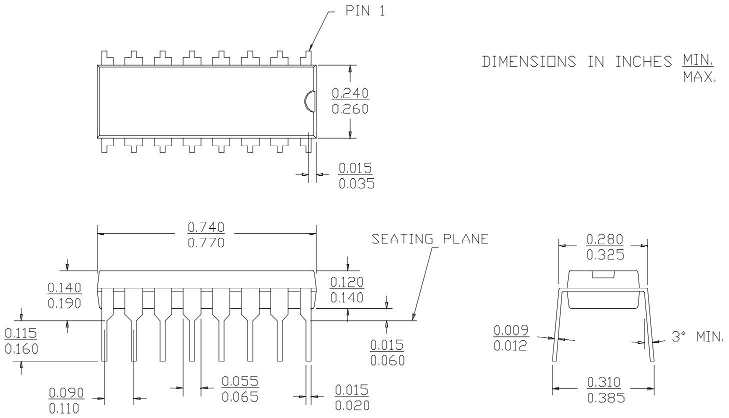
20-Pin Square Leadless Chip Carrier L61

MIL-STD-1835 C–2A

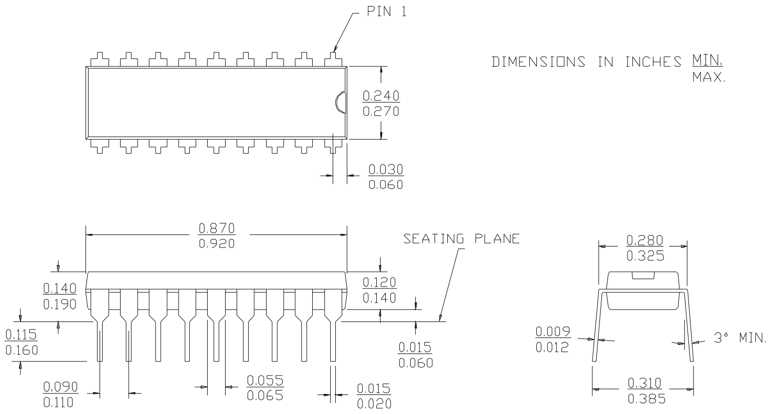

.045
.055
PIN #1
DIMENSIONS IN INCHES
MIN.
MAX.
BOTTOM
.022
.028
.045
.055
.045
.055
.009 R.
20 PLACES
.060
.075
.054
.066
TOP
SIDE
.342
.358
.342
.358

Package Diagrams (continued)

16-Lead (300-Mil) Molded DIP P1


PIN 1
DIMENSIONS IN INCHES MIN. MAX.
0.240 0.260
0.015 0.035
0.740 0.770
SEATING PLANE
0.140 0.190
0.120 0.140
0.115 0.160
0.015 0.060
0.090 0.110
0.055 0.065
0.015 0.020
0.280 0.325
0.009 0.012
3° MIN.
0.310 0.385

18-Lead (300-Mil) Molded DIP P3


PIN 1
DIMENSIONS IN INCHES MIN. MAX.
0.240 0.270
0.030 0.060
0.870 0.920
SEATING PLANE
0.140 0.190
0.120 0.140
0.115 0.160
0.015 0.060
0.090 0.110
0.055 0.065
0.015 0.020
0.280 0.325
0.009 0.012
3° MIN.
0.310 0.385

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