MC14408
MC14409

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

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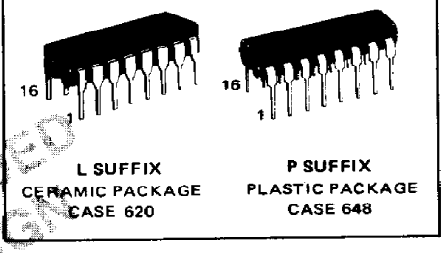
BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

The MC14408 and the MC14409 are devices designed to convert a four bit binary input code to a number of serial output pulses corresponding to the value of the input code.

The devices can be used in telephone pulse dialing applications when combined with their companion device, the MC14419 (2-of-8 keypad-to-binary code converter). The devices have been partitioned to allow convenient addition of RAM memory and controls for repertoire dialing applications.

The MC14408 and MC14409 perform identical functions with the exception of the signal output at the DRO (Dial Rotating Output). In the MC14408, DRO remains high during continuous outpulsing of all digits and in the MC14409 DRO is low between each digit pulse burst.

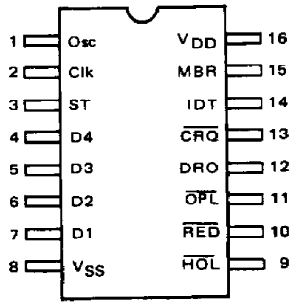
- On-Chip Oscillator
- Diode Protection on All Inputs
- Dialing of Numbers Up to 16 Digits Long
- Memory Storage (FIFO) and Re-Dialing (single pin) of Last Telephone Number
- Hold Interrupt Control for Additional Interdigit Delays (such as a Wait for Intermediate Dial Tones)
- Selectable Dialing Rate (10 pps or 20 pps)
- Selectable Interdigit Time (300 or 800 ms @ 10 pps; 150 or 400 ms @ 20 pps)
- Selectable Make-Break Ratio (61% or 67%)
- Buffered Outputs Compatible with Discrete Transistor Driver Interface, One Low-power Schottky TTL Load or Two Low-power TTL Loads Over the Rated Temperature Range.
- Low Power Dissipation — I_{DD} (operating with oscillator) = 470 μA typ @ V_{DD} = 5.0 Vdc, f_{Osc} = 16 kHz, C_L = 50 pF



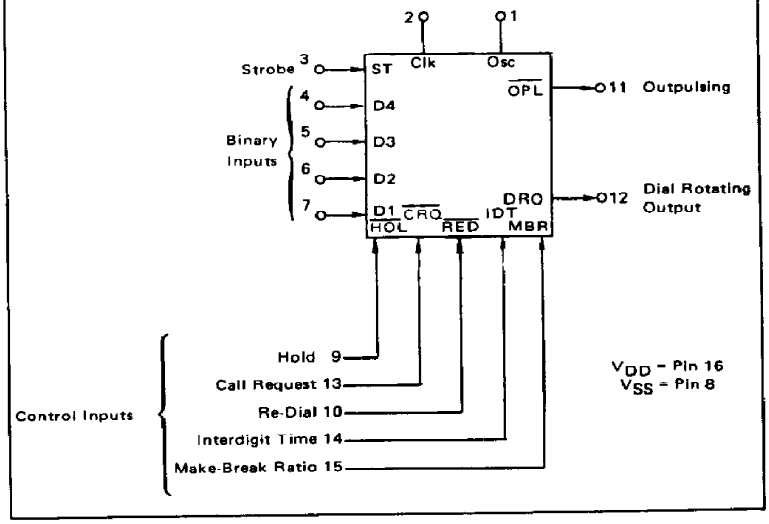
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Noise Immunity ($\Delta V_{out} \leq$ 0.5 Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
($\Delta V_{out} \leq$ 0.5 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.80	-1.7	–	-0.60	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.20	–	-0.16	-0.36	–	-0.12	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
Input Current	I_{in}	6.0	–	0.3	–	±0.00001	±0.30	–	1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	12	–	5.0	12	–	12	pF
Operating Supply Current	I_{DD}	3	–	250	–	160	200	–	200	µAdc
f_{cl} = 16 kHz (operating		5	–	700	–	470	550	–	550	
with Osc)		6	–	1250	–	740	1000	–	1000	

FIGURE 1
TIMING DIAGRAM — DATA AND STROBE INPUTS

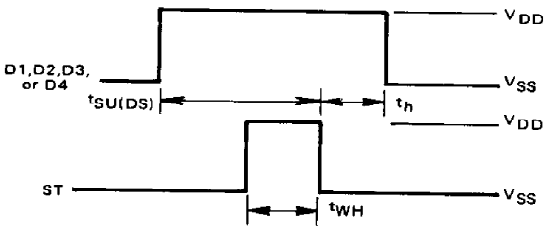
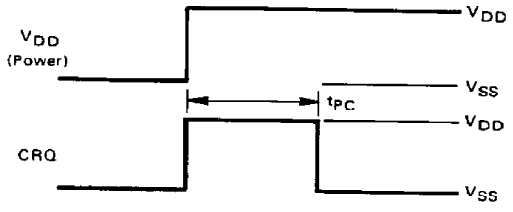


FIGURE 2
TIMING DIAGRAM — CALL REQUEST



If power is turned off after each call, CRQ must stay high after power is applied (for a duration of t_{PC}) to ensure no spurious outpulsing. For this use the redial function is invalid.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time** t_{TLH} = (3.0 ns/pF) C_L + 30 ns	t_{TLH}	5.0	–	180	400	ns
Output Fall Time** t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	ns
Power Up to Call Request Pause	t_{PC}	3 to 6	$48/f_{cl}$*	–	–	ms
Call Request to First Strobe Pulse	t_{CS}	3 to 6	$48/f_{cl}$*	–	–	ms
Strobe to Strobe Separation Time	t_{SS}	3 to 6	$48/f_{cl}$*	–	–	ms
Strobe Pulse Width	t_{WH}	3 to 6	1.0	–	–	µs
Strobe to Data Hold Time	t_h	3 to 5	–	150	400	ns
Clock Frequency***	f_{cl}	3 to 6	12.5	16	100	kHz
Percent Break to Make Ratio (MBR = 0) (MBR = 1)	%MB	3 to 6	 – –	 61 67	 – –	%
Outpulsing Rate (f_{OPL} = *f_{cl}/1.6) f_{cl} = 16 kHz f_{cl} = 32 kHz	f_{OPL}	3 to 6	 – –	 10 20	 – –	pps
Interdigit Time t_{ID} = (5 x IDT + 3)/f_{OPL} IDT = 0 f_{OPL} = 10 pps f_{OPL} = 20 pps IDT = 1 f_{OPL} = 10 pps f_{OPL} = 20 pps	t_{ID}	3 to 6	 – – – –	 300 150 800 400	 – – – –	ms
Strobe to Output Time Initial Outpulsing Stream IDT = 0 f_{OPL} = 10 pps f_{OPL} = 20 pps IDT = 1 f_{OPL} = 10 pps f_{OPL} = 20 pps Continued Outpulsing Stream IDT = 0 or 1 f_{OPL} = 10 pps f_{OPL} = 20 pps	t_{SOI} t_{SOC}	3 to 6 3 to 6	 300 150 800 400 100 50	 – – – – – –	 400 200 900 450 200 100	ms ms
Hold to Outpulse Time IDT = 0 or 1 f_{OPL} = 10 pps f_{OPL} = 20 pps	t_{HOL}	3 to 6	 100 50	 – –	 200 100	ms
Dial Rotating Overlap Time . f_{OPL} = 10 pps f_{OPL} = 20 pps	t_{DRO}	3 to 6	 – –	 100 50	 – –	ms
Data to Strobe Setup Time (f_{cl} = 16 kHz)	$t_{SU(DS)}$	3 to 6	1.5	–	–	µs
Re-dial Pulse Width (f_{cl} = 16 kHz)	–	3 to 6	–	200	–	ms

*f_{cl} in kHz

**The formula given is for the typical characteristics only.

*** Minimum clock pulse width = 1.0 µs.

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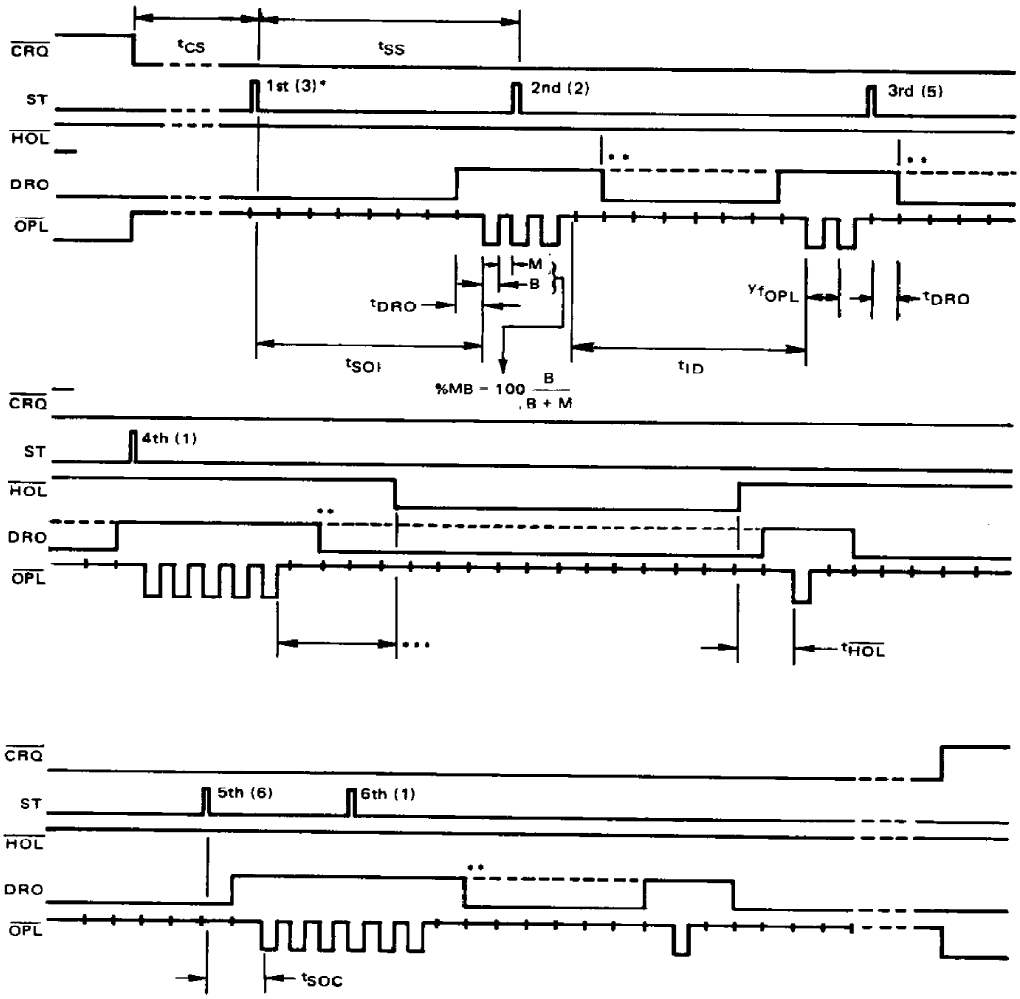
FIGURE 3
PHONE DIALER SYSTEM TIMING DIAGRAM



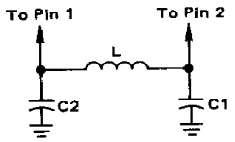
Notes:

(*)1st, 2nd, 3rd, etc., denotes Strobe pulse sequence — i.e., which digit in the phone number is being dialed. The number in parentheses denotes the numerical value of the digit being dialed. The examples define the various voltage — level and timing requirements, not a complete phone number.

(**)For the MC14408 the DRO signal will remain high provided digits remain in the memory, or a digit for continuing outpulsing is strobed in before the anticipated falling edge of the most significant digit in the memory. (i.e., [200 % MB] ms after the most significant outpulsing edge). The time from Strobe to DRO can be 0 to 100 ms.

(***)For the HOL signal to hold a next digit (e.g. the 4th, etc.,) the HOL falling edge must not appear after [t_{ID}-%MB + 100] ms the last outpulsing edge of the previous digit.

FIGURE 4
COMPONENT SELECTION FOR OSCILLATOR/CLOCK FREQUENCY



$f_{cl} = \frac{7.118}{\sqrt{LC}}$ where f_{cl} in kHz, L in mH,
C = C1 = C2 in µF

$\%f_{cl} = -0.5\,[\%C + \%L] \pm 3.0$ where $\%f_{cl}$, %C, %L are the frequency capacitor, and inductor tolerances in percent. The ±3.0% accounts for supply voltage and ambient temperature variations.

EXAMPLE

L	%L	C=C1=C2	%C	f_{cl}	$\%f_{cl}$	OUTPULSING RATE $f_{OPL} = f_{cl}/1.6$
5.0 mH	±5.0	0.04 µF	±5.0	≈16 kHz	±8.0	≈10 pps
5.0 mH	±5.0	0.01 µF	±5.0	≈32 kHz	±8.0	≈20 pps

FIGURE 5
TRUTH TABLE

INPUTS							OUTPUTS	
$\overline{CRQ}$	D4 D3 D2 D1	ST	$\overline{RED}$	$\overline{ROL}$	IDT	MBR	$\overline{OPL}$	DRO †
1	X X X X	X	X	X	X	X	0	0
0	X X X X	0	1	1	X	X	1 (Steady State)	0 (Steady State)
0	X X X X (nth Digit)	⊓	1	1	X	X	Number of pulses (1/1 of nth digit = binary combination of D4, D3, D2, D1. *	1 During outpulsing 0 Otherwise
0	X X X X	0	⊔	1	X	X	Digits of number in memory re-sent.	1 During outpulsing 0 Otherwise
0	X X X X	X	1	0	X	X	1 After conclusion of digit being outpulsed.	0 After conclusion of digit being outpulsed
X	X X X X	X	X	X	0 1	X	300 ms Interdigit time 800 ms Interdigit time	f_{cl} = 16 kHz
X	X X X X	X	X	X	X	0 1	61% (≈1.6:1) Make-Break Ratio 67% (≈2:1) Make-Break Ratio	

X = Don't Care
* With the exception of 0000 which will give 10 pulses.
† Refer to timing diagram Figure 3.

FIGURE 6
MEMORY CLEAR

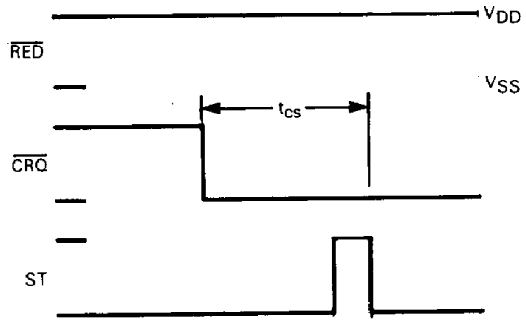
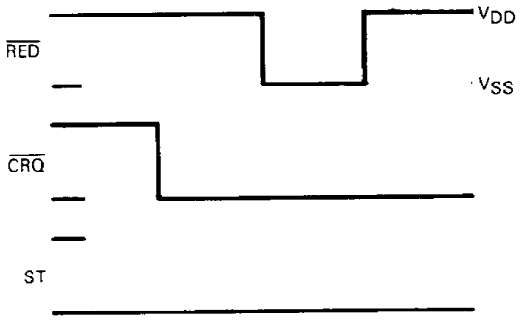


FIGURE 7
REDIAL SEQUENCE



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DEVICE OPERATION

OSCILLATOR (Osc, Pin 1)

This pin is an input to the internal oscillator and feedback connection for the L-C π-network. An external clock signal, if desired can be applied to Osc.

CLOCK (Clk, Pin 2)

This pin is an output from the internal oscillator and feedback connection for the L-C π-network and provides the system clock for the MC14419 bounce eliminator circuitry.

STROBE INPUT (ST, Pin 3)

This Strobe input, when high (ST = V_{DD}), signifies that the data at the D1, D2, D3, and D4 inputs is valid, and enters the 4-bit number into the internal FIFO (First-In, First-Out) memory for subsequent outpulsing. The first strobe pulse after a call is requested (CRQ = low) clears the memory of any previous number and enters the first digit of the new number. Successive strobe pulses will store up to a maximum of 16 digits in the internal FIFO memory, which ignores all digits entered in excess of that amount until a new call is requested.

DATA INPUTS (D4, D3, D2, D1, Pins 4, 5, 6, 7)

These pins are the Data inputs to the internal memory. A binary coded digit number entered will result in an equivalent number of pulses at the $\overline{OPL}$ (outpulsing) output, except for the code 0000, which will outpulse 10 pulses.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 8)

This pin is the negative power supply connection. Normally this pin is system ground.

HOLD ($\overline{HOL}$, Pin 9)

When taken low ($\overline{HOL}$ = V_{SS}), the Hold input disables the outpulsing at the completion of the digit being outpulsed. When taken high, outpulsing resumes. This feature can be used in multi-dial-tone phone systems to provide longer interdigit pauses when necessary.

RE-DIAL ($\overline{RED}$, Pin 10)

The Re-Dial input, when taken low ($\overline{RED} = V_{SS}$) automatically outpulses the digits entered into memory after the last time a call was requested. (See Redial Sequence Diagram Figure 6.)

OUTPULSING ($\overline{OPL}$, Pin 11)

The Outpulsing output sends out bursts of pulses equivalent to the digits of the telephone number stored in the memory. The duty cycle and interdigit time of the digit pulse bursts are controlled, respectively by the MBR (Pin 15) and IDT (Pin 14).

DIAL ROTATING OUTPUT (DRO, Pin 12)

The Dial Rotating (also known as "Off Normal") Output provides a signal which indicates that digit pulse bursts are being sent. In the MC14409, DRO goes high (V_{DD}) at the beginning of the first digit pulse burst and goes low (V_{SS}) between succeeding consecutive digit pulse bursts. In the MC14408, however, DRO goes high at the beginning of the first digit pulse burst and remains high until the last digit pulse burst of the telephone number has been sent (see Timing Diagram, Figure 3).

CALL REQUEST ($\overline{CRQ}$, Pin 13)

The Call Request input when taken low ($\overline{CRQ} = V_{SS}$) resets internal counters and prepares the internal logic to either accept new digit inputs to be dialed, or to re-dial (see RED, Pin 10) the digits stored in the memory. The Relationship Between Memory Clear and Redial is shown in Figure 7.

INTERDIGIT TIME (IDT, Pin 14)

The Interdigit Timing input determines the length of time between consecutive digit pulse bursts. See the Interdigit Time (t_{ID}) in the switching characteristics for the length of time.

MAKE-BREAK RATIO (MBR, Pin 15)

The Make-to-Break Ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output. For MBR = V_{DD}, duty cycle = 67% low, 33% high; and for MBR = V_{SS}, duty cycle = 61% low, 39% high.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

This pin is the package positive power supply pin.

FIGURE 8 — KEYPAD TO PULSE DIALER FLOW DIAGRAM

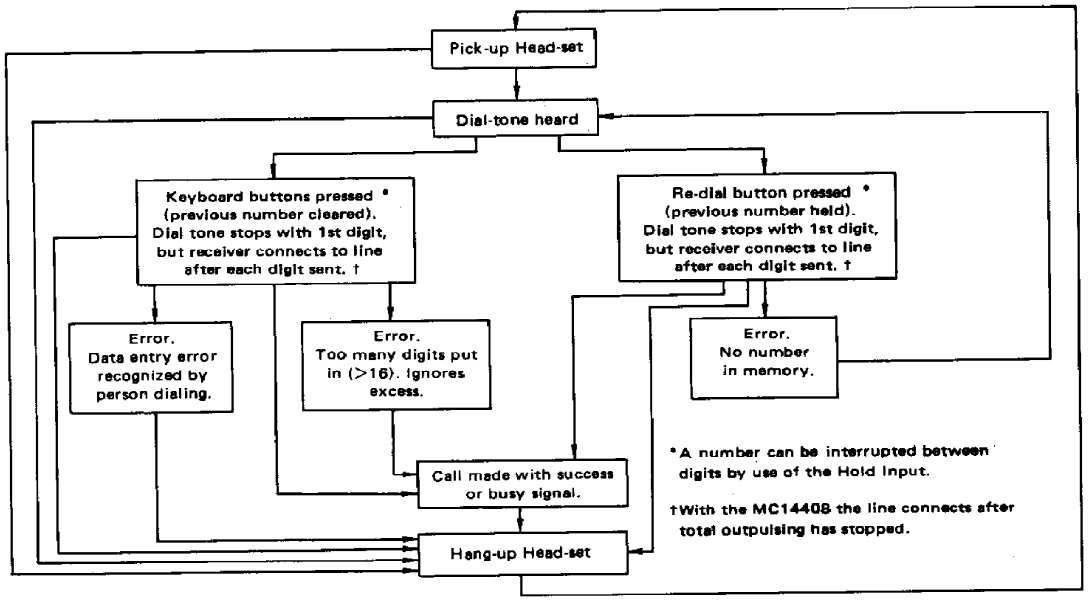

FIGURE 9 — PHONE DIALER SYSTEM

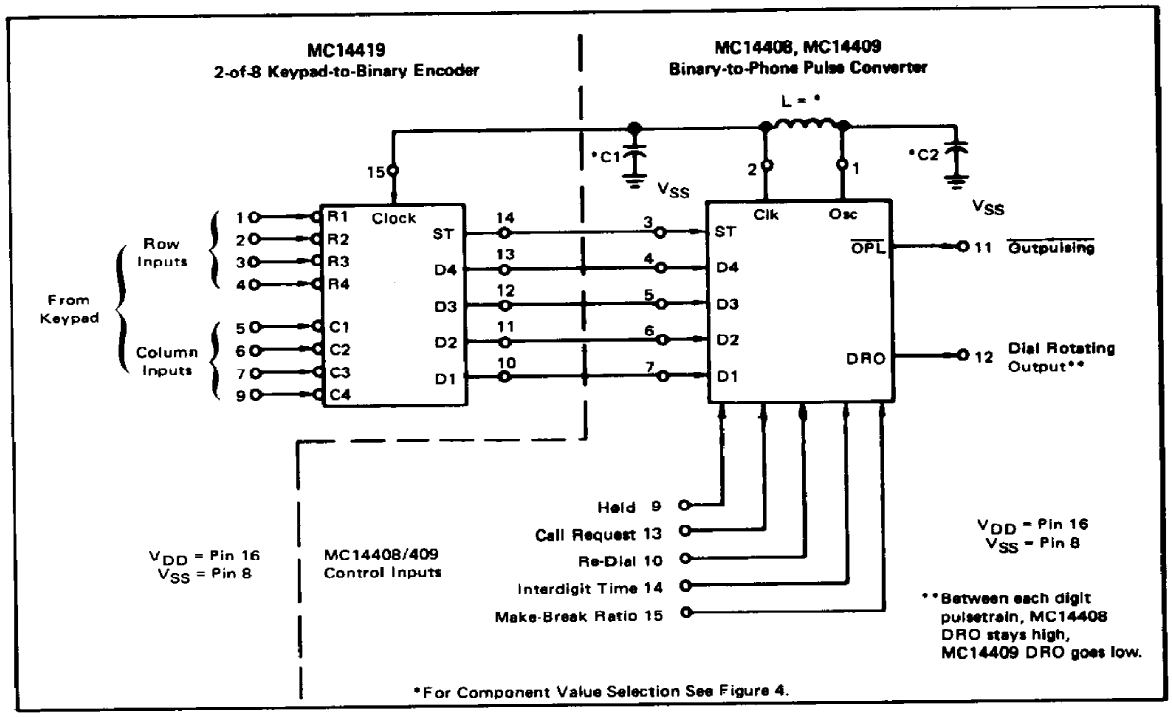

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FIGURE 10 — STANDARD K-500 TELEPHONE

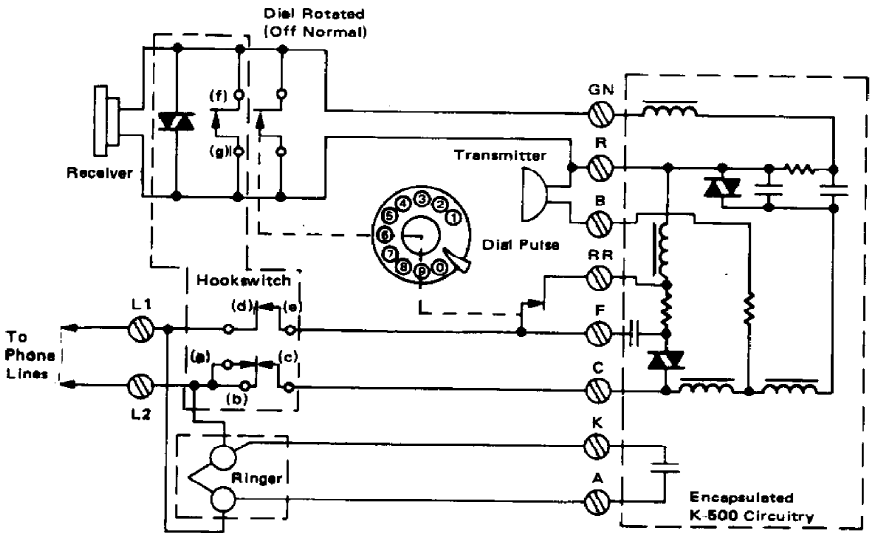

FIGURE 11 — MODIFIED K-500 TELEPHONE