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MOTOROLA

MC34115

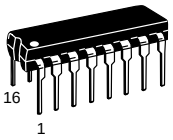
Continuously Variable Slope Delta Modulator/Demodulator

Providing a simplified approach to digital speech encoding/decoding, the MC34115 CVSD is designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding functions.

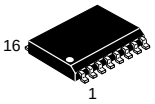
- Encode and Decode Functions Selectable with a Digital Input
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ Reference Provided On–Chip)
- 3–Bit Algorithm

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

SEMICONDUCTOR TECHNICAL DATA

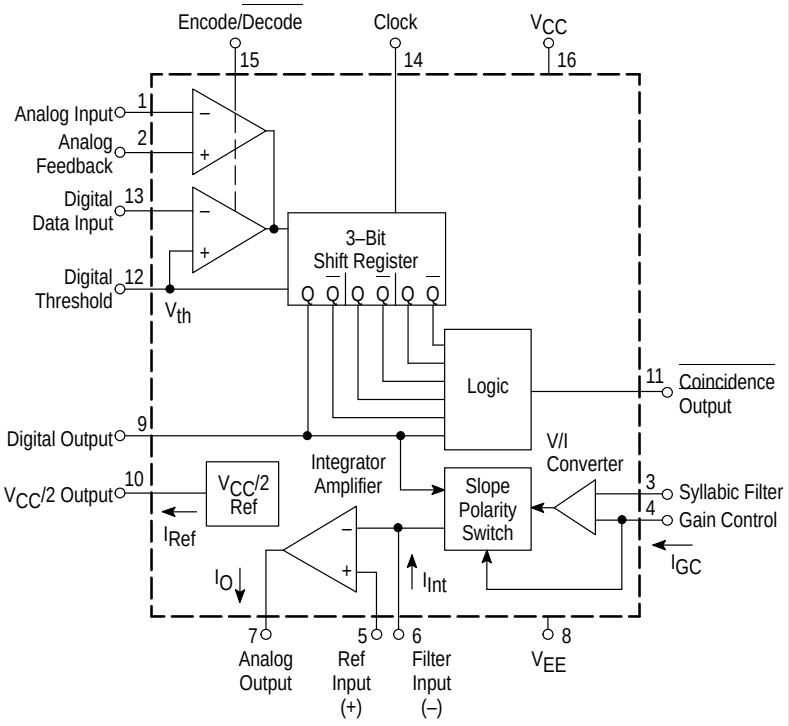


P SUFFIX
PLASTIC PACKAGE
CASE 648



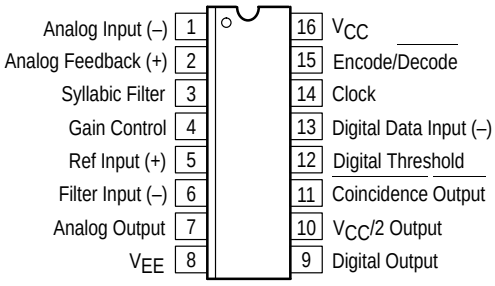
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

CVSD Block Diagram



This device contains 144 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34115P	T_A = 0° to +70°C	Plastic DIP
MC34115DW		SO–16L

MAXIMUM RATINGS (All voltages referenced to V_{EE}, T_A = 25°C, unless otherwise noted.) (Note 2)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{th}	–0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/Decode)	V_{Logic}	–0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	–0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	–0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	–0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(ref)}$	V_{CC}/2 – 1.0 to V_{CC}	Vdc
V_{CC}/2 Output Current	I_{ref}	–25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0° to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range (Figure 1)	V_{CC}	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}				mA
V_{CC} = 5.0 V		–	4.6	7.5	
V_{CC} = 15 V		–	7.0	12	
Clock Rate	SR	–	16 k	–	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.002	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) 4.75 V ≤ V_{CC} ≤ 16.5 V	V_I	1.3	–	V_{CC} – 1.3	Vdc
Analog Output Range (Pin 7) 4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ±5.0 mA	V_O	1.3	–	V_{CC} – 1.3	Vdc
Input Bias Currents (Figure 3)	I_{IB}				µA
Comparator in Active Region					
Analog Input (I1)		–	0.5	2.5	
Analog Feedback (I2)		–	0.5	2.5	
Syllabic Filter Input (I3)		–	0.06	0.5	
Reference Input (I5)		–	–0.06	–0.5	
Input Offset Current	I_{IO}				µA
Comparator in Active Region					
Analog Input/Analog Feedback |I1 – I2| (Figure 3)		–	0.15	0.8	
Integrator Amplifier |I5 – I6| (Figure 4)		–	0.02	0.2	
Input Offset Voltage V/I Converter (Pins 3 and 4) (Figure 5)	V_{IO}	–	2.0	10	mV
Transconductance	gm				mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	–	
Integrator Amplifier, 0 to +5.0 mA Load		1.0	10	–	

NOTES: 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.
2. Devices should not be operated at these values. The “Electrical Characteristics” provide conditions for actual device operation.
3. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 16 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one–half of the change in integrator output voltage during one clock cycle (ramp step size).

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0° to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times (Note 1)					µs
Clock Trigger to Digital Output	t_{PLH}	–	1.0	3.0	
C_L = 25 pF to Gnd	t_{PHL}	–	0.8	3.0	
Clock Trigger to Coincidence Output	t_{PLH}	–	1.0	3.5	
C_L = 25 pF to Gnd, R_L = 4.0 kΩ to V_{CC}	t_{PHL}	–	0.8	2.5	
Coincidence Output Voltage – Low Logic Stage ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	–	0.12	0.25	Vdc
Coincidence Output Leakage Current – High Logic State (V_{OH} = 15 V)	$I_{OH(Con)}$	–	0.01	0.5	µA
Applied Digital Threshold Voltage Range (Pin 12)	V_{th}	1.2	–	V_{CC} – 2.0	Vdc
Digital Threshold Input Current	$I_{I(th)}$				µA
1.2 V ≤ V_{th} ≤ V_{CC} – 2.0 V					
V_{IL} Applied to Pins 13, 14 and 15		–	–	5.0	
V_{IH} Applied to Pins 13, 14 and 15		–	–10	–50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	–	–	mA
V_{CC}/2 Generator Maximum Output Current (Source Only)	I_{ref}	–10	–	–	mA
V_{CC}/2 Generator Output Impedance (0 to –10 mA)	z_{ref}	–	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance (4.75 V ≤ V_{CC} ≤ 16.5 V)	εr	–	–	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)					Vdc
Low Logic State	V_{IL}	V_{EE}	–	V_{th} – 0.4	
High Logic State	V_{IH}	V_{th} + 0.4	–	16.5	
Dynamic Total Loop Offset Voltage (Note 3) (Figures 3, 4 and 5)	ΣV_{offset}				mV
I_{GC} = 33 µA, V_{CC} = 12 V					
T_A = 25°C		–	±2.5	±7.0	
0°C ≤ T_A ≤ +70°C		–	±3.0	±10	
I_{GC} = 33 µA, V_{CC} = 5.0 V					
T_A = 25°C		–	±4.0	±8.0	
0°C ≤ T_A ≤ +70°C		–	±4.5	±12	
Digital Output Voltage (Pin 9)					Vdc
I_{OL} = 3.6 mA	V_{OL}	–	0.1	0.4	
I_{OH} = –0.35 mA	V_{OH}	V_{CC} – 1.0	V_{CC} – 0.2	–	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	3.2	–	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int} \rvert$				
I_{GC} = 12 µA		8.0	10	12	µA
I_{GC} = 1.5 mA		1.4	1.5	1.6	mA
I_{GC} = 3.0 mA		2.75	3.0	3.25	mA
Dynamic Integrating Current Match (Figure 6) (I_{GC} = 1.5 mA)	$V_{O(Ave)}$	–	±100	±300	mV
Input Current – High Logic State (V_{IH} = 16.5 V)	I_{IH}				µA
Digital Data Input		–	–	5.0	
Clock Input		–	–	5.0	
Encode/Decode Input		–	–	5.0	
Input Current – Low Logic State (V_{IL} = 0 V)	I_{IL}				µA
Digital Data Input		–10	–	–	
Clock Input		–360	–	–	
Encode/Decode Input		–36	–	–	
Clock Input, V_{IL} = 0.4 V		–72	–	–	

NOTES: 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.
2. Devices should not be operated at these values. The “Electrical Characteristics” provide conditions for actual device operation.
3. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 16 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one–half of the change in integrator output voltage during one clock cycle (ramp step size).

DEFINITION AND FUNCTION OF PINS

Pin 1 – Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 – Analog Feedback

This is the noninverting input to the analog signal comparator. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit, Pin 2 is not used and may be tied to $V_{CC}/2$ at Pin 10 or ground.

The analog input comparator has bias currents of 2.5 μA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 – Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6.0 ms to 50 ms are used in voice codecs.

Pin 4 – Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V–I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x–axis) and the integrating current, I_{Int} (y–axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 – Reference Input

This pin is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit, it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 – Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should typically be between 8.0 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 – Analog Output

This is the integrator op amp output. It is capable of driving a 600 Ω load referenced to $V_{CC}/2$ to +6.0 dBm and can otherwise be treated as an op amp output. Pins 5, 6 and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 – V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 – Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and noninverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 – $V_{CC}/2$ Output

An internal low impedance mid–supply reference is provided for use in single supply applications. The internal regulator is a current source and must be loaded with a resistor to ensure its sinking capability. If a +6.0 dBmo signal is expected across a 600 Ω input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is possible only if Pin 10 sources 3.66 mA into a resistor normally and will source the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 – $\overline{\text{Coincidence}}$ $\overline{\text{Output}}$

The coincidence output will be low whenever the content of the internal 3–bit shift register is all 1s or all 0s. Pin 11 is an open collector NPN device and requires a pull–up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is R_SC_S while the decay constant is $(R_S + R_P)C_S$. Thus, longer decays are easily achievable. The NPN device should not be required to sink more than 3.0 mA. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4.0 kΩ to 12 V and C_L = 25 pF to ground.

Pin 12 – Digital Threshold

This input sets the switching threshold for Pins 13, 14 and 15. It is intended to aid in interfacing different logic families without external parts. Typically it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 – Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit a signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip–flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit. A 16 k bit rate requires a 16 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum high time for the clock input is 300 ns and minimum low time is 900 ns.

Pin 15 – Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non–voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

Pin 16 – V_{CC}

The power supply range is from 4.75 to 16.5 V between Pin V_{CC} and V_{EE}.

Figure 1. Power Supply Current

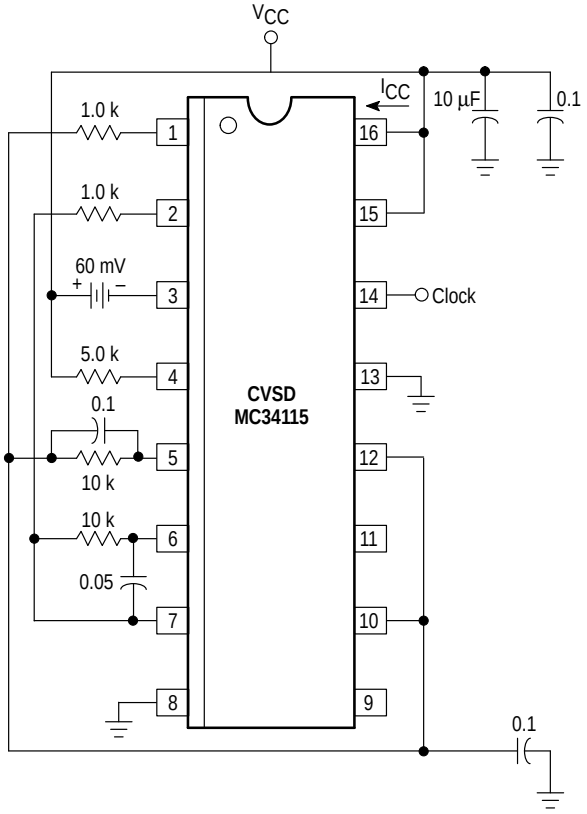
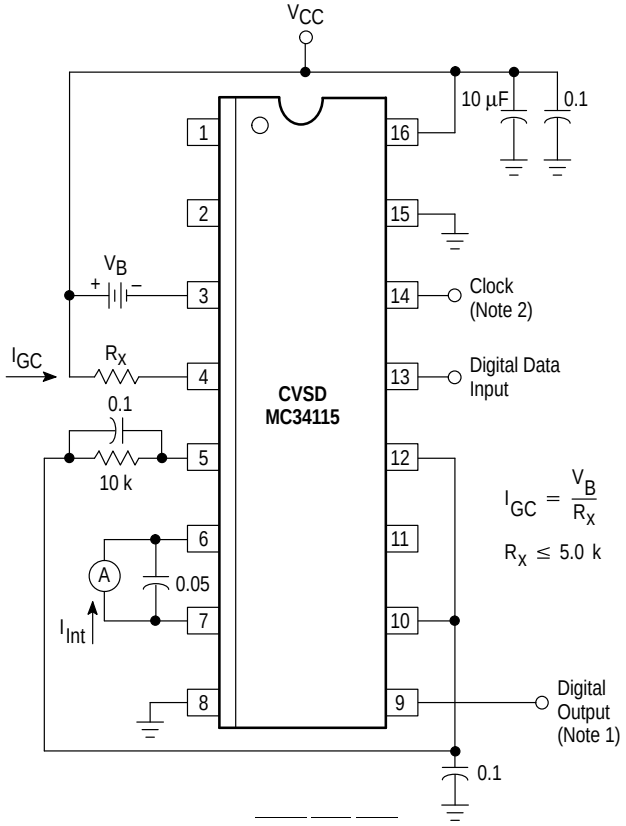
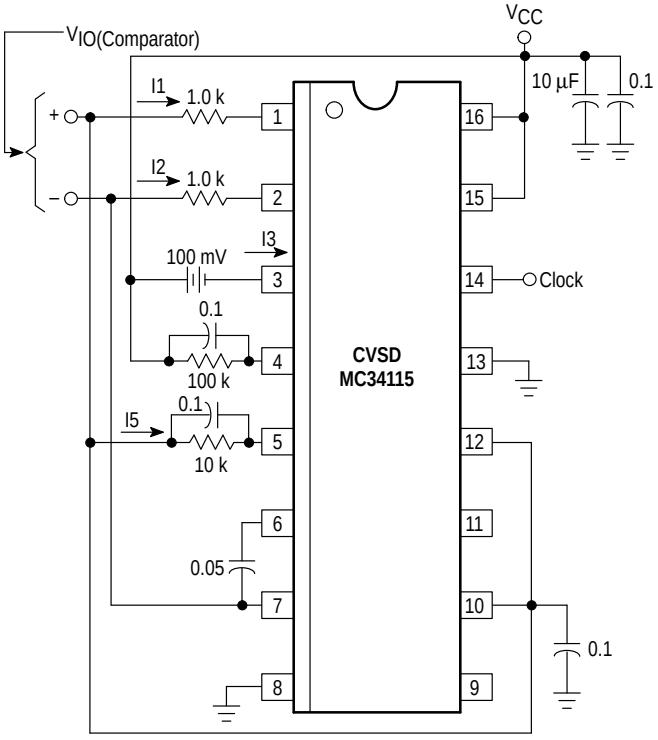


Figure 2. I_{GCR} – Gain Control Range and I_{Int} – Integrating Current



NOTES: 1. Digital Output = Digital Data Input
2. For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

Figure 3. Input Bias Currents, Analog Comparator Offset Voltage and Current



NOTE: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

Figure 4. Integrator Amplifier Offset Voltage and Current

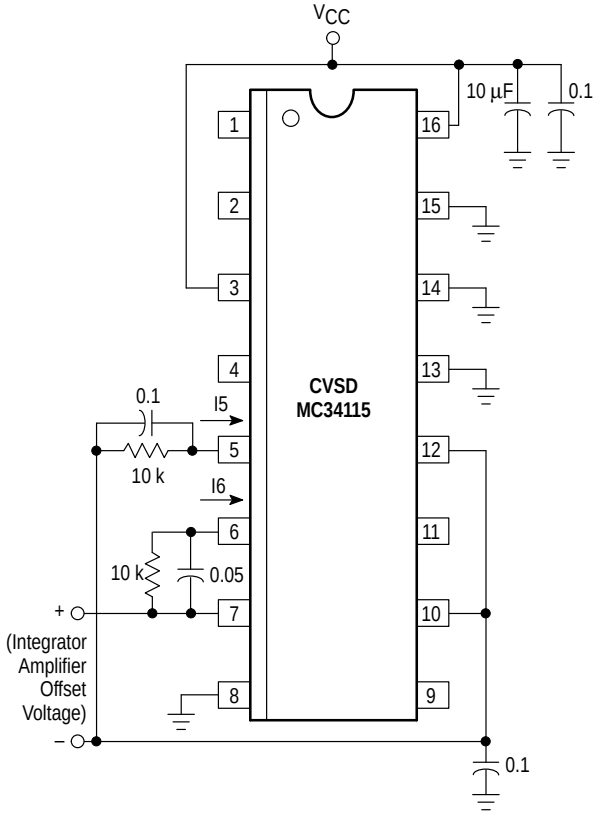
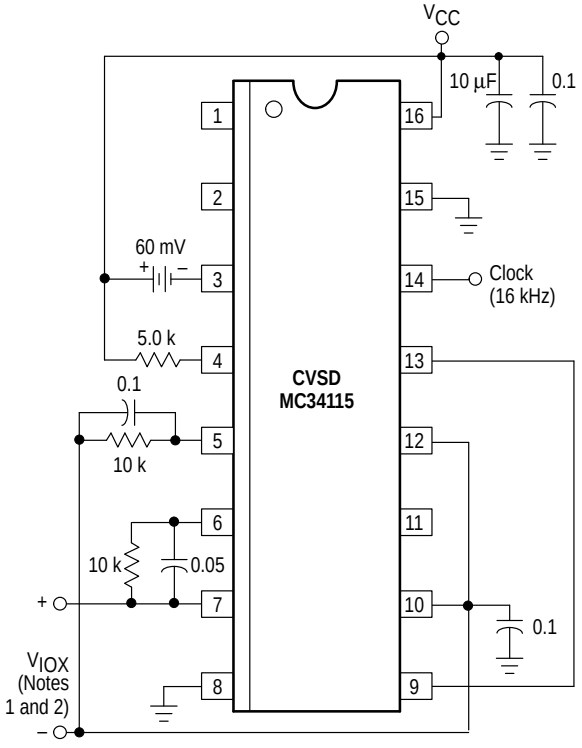
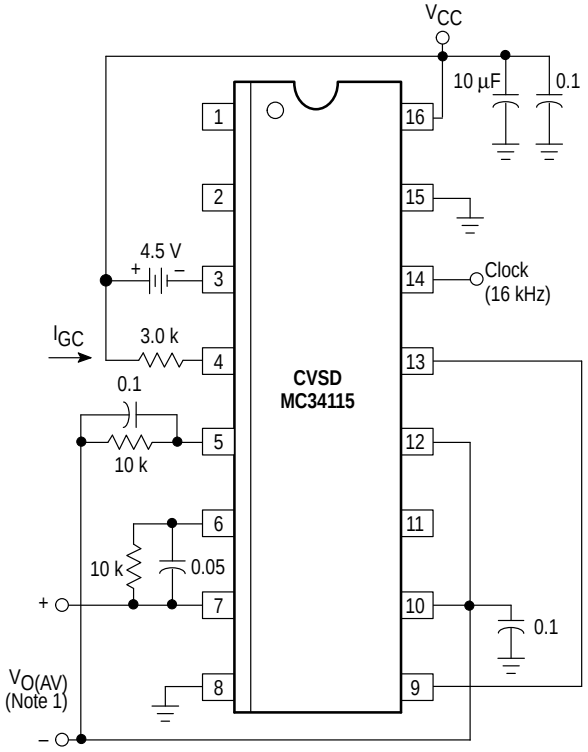


Figure 5. V/I Converter Offset Voltage, V_{IO} and V_{IOX}



NOTES: 1. Integrator amplifier offset voltage plus slope polarity switch mismatch.
2. V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

Figure 6. Dynamic Integrating Current Match



NOTES: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 3 in the Electrical Characteristics table.
3. See Figures 8 and 9.

TYPICAL PERFORMANCE CURVES

Figure 7. Typical I_{Int} versus I_{GC} (Mean ±2 σ)

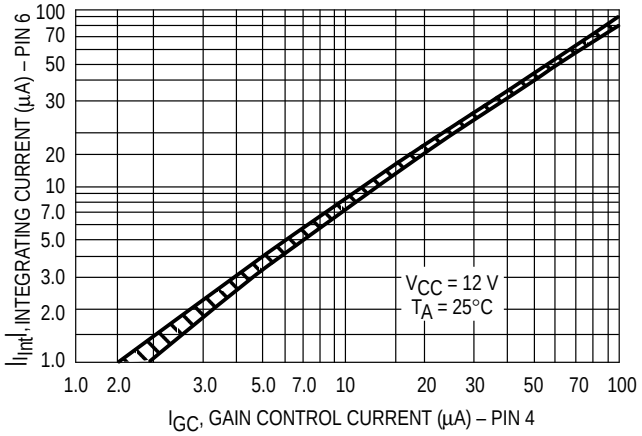


Figure 8. Normalized Dynamic Integrating Current Match versus V_{CC}

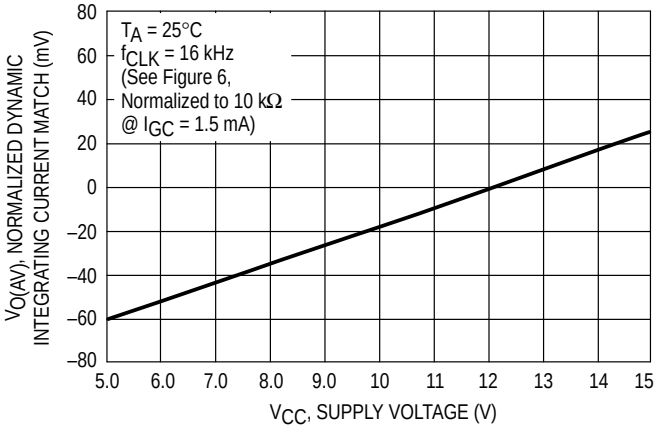


Figure 9. Normalized Dynamic Integrating Current Match versus Clock Frequency

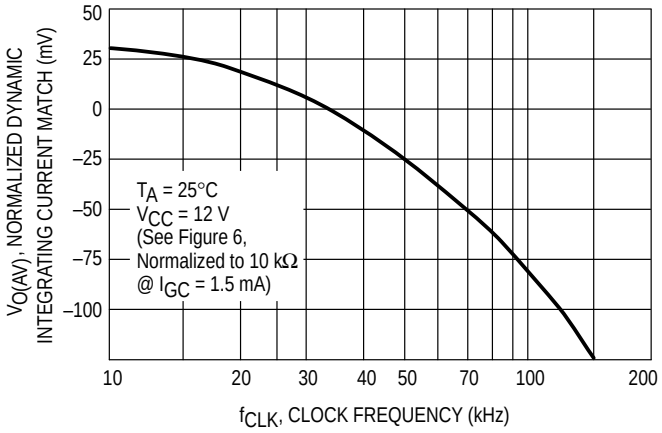


Figure 10. Dynamic Total Loop Offset versus Clock Frequency

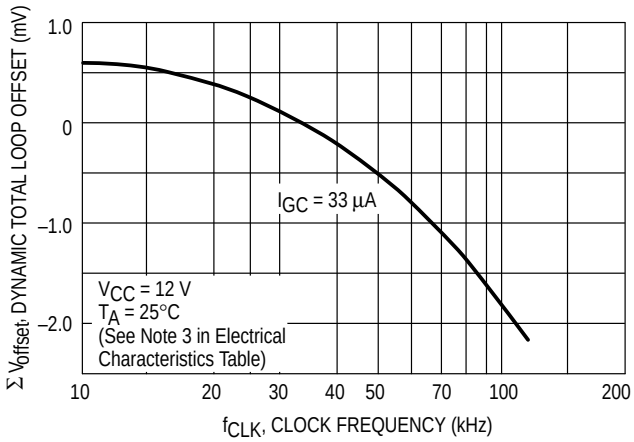


Figure 11. Block Diagram of the CVSD Encoder

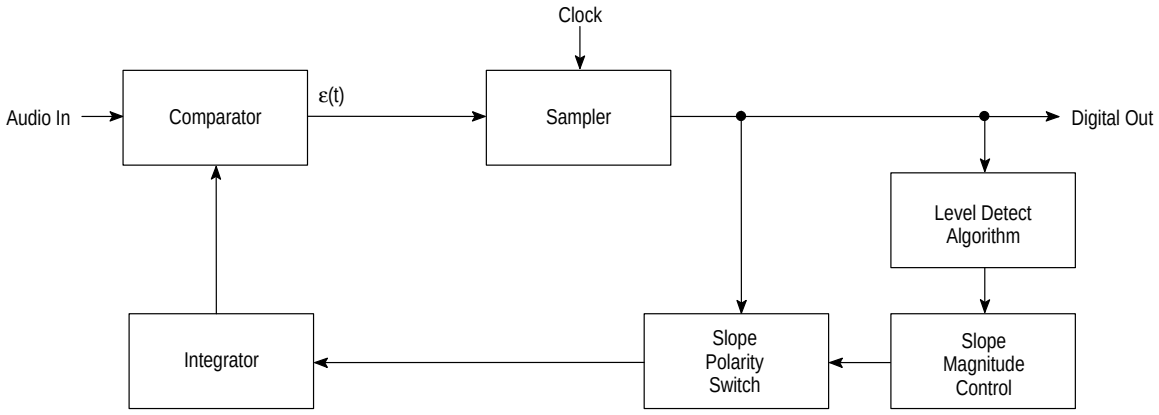


Figure 12. CVSD Waveforms

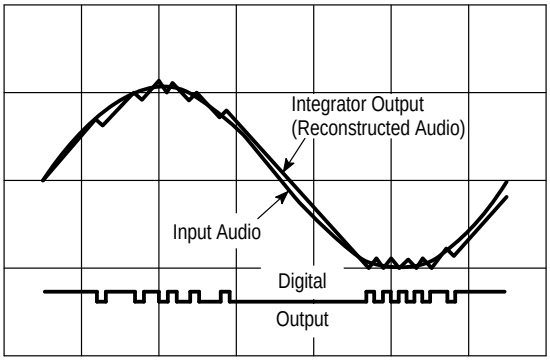
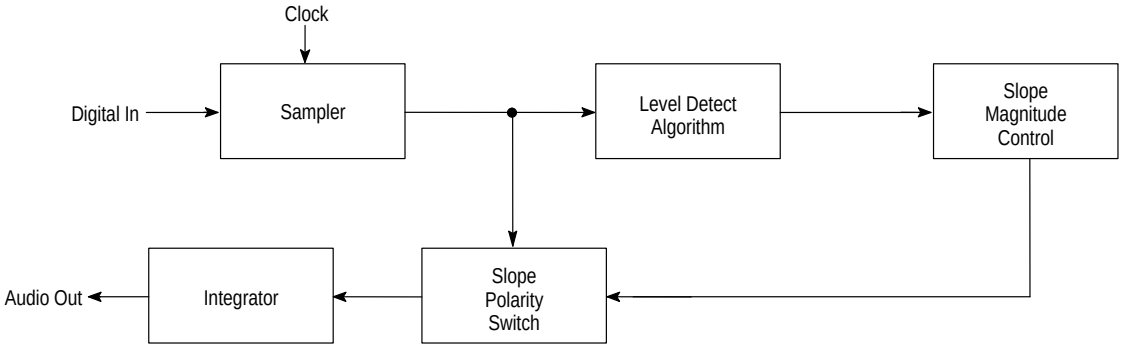


Figure 13. Block Diagram of the CVSD Decoder



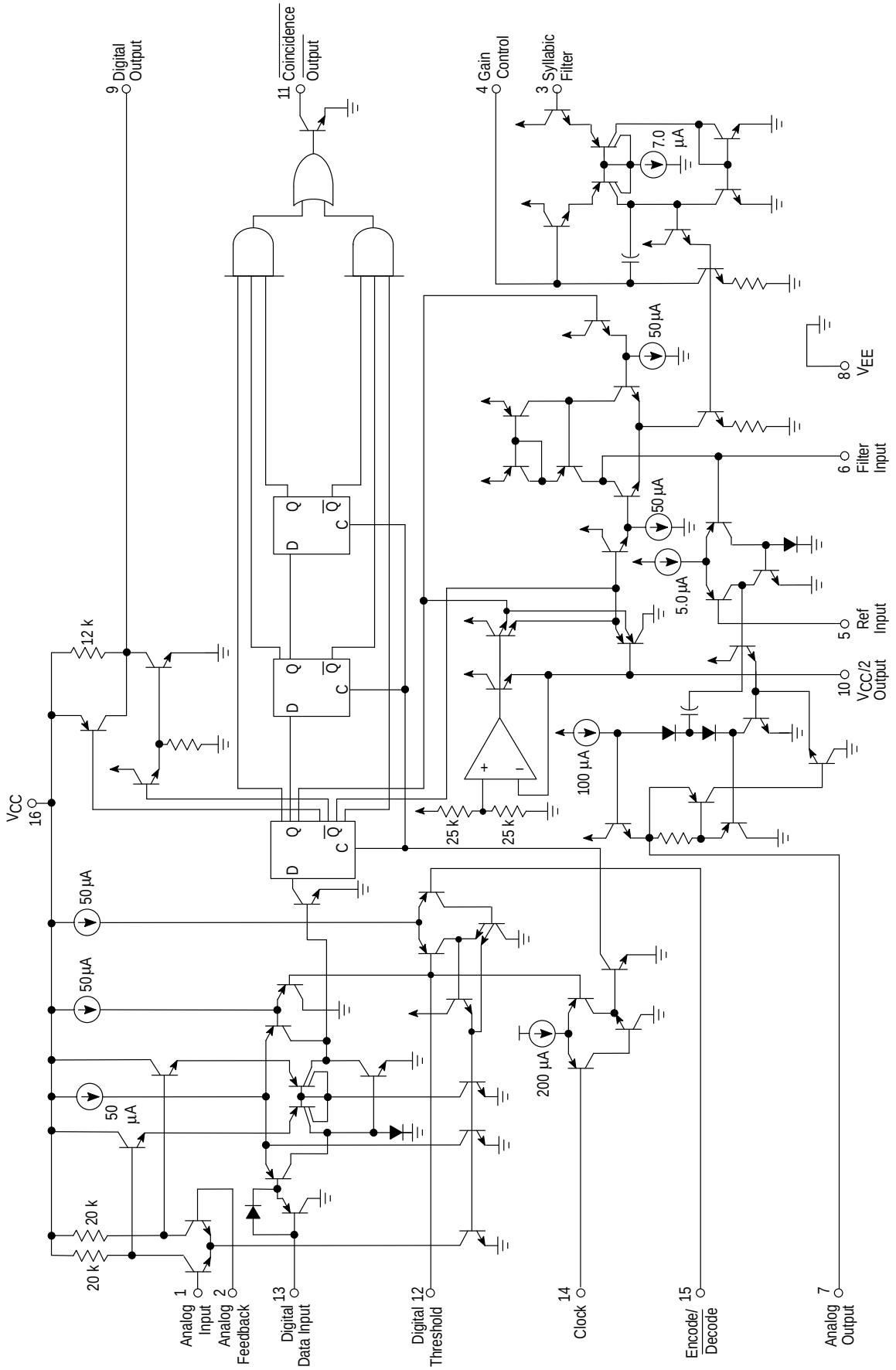


Figure 14. CVSD Circuit Schematic

CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A–D converters do not meet the communications requirements. The CVSD A–D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band–limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4.0 kHz and clock rates from 8.0 k and up are possible. Thus, the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly, a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3–bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single–pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

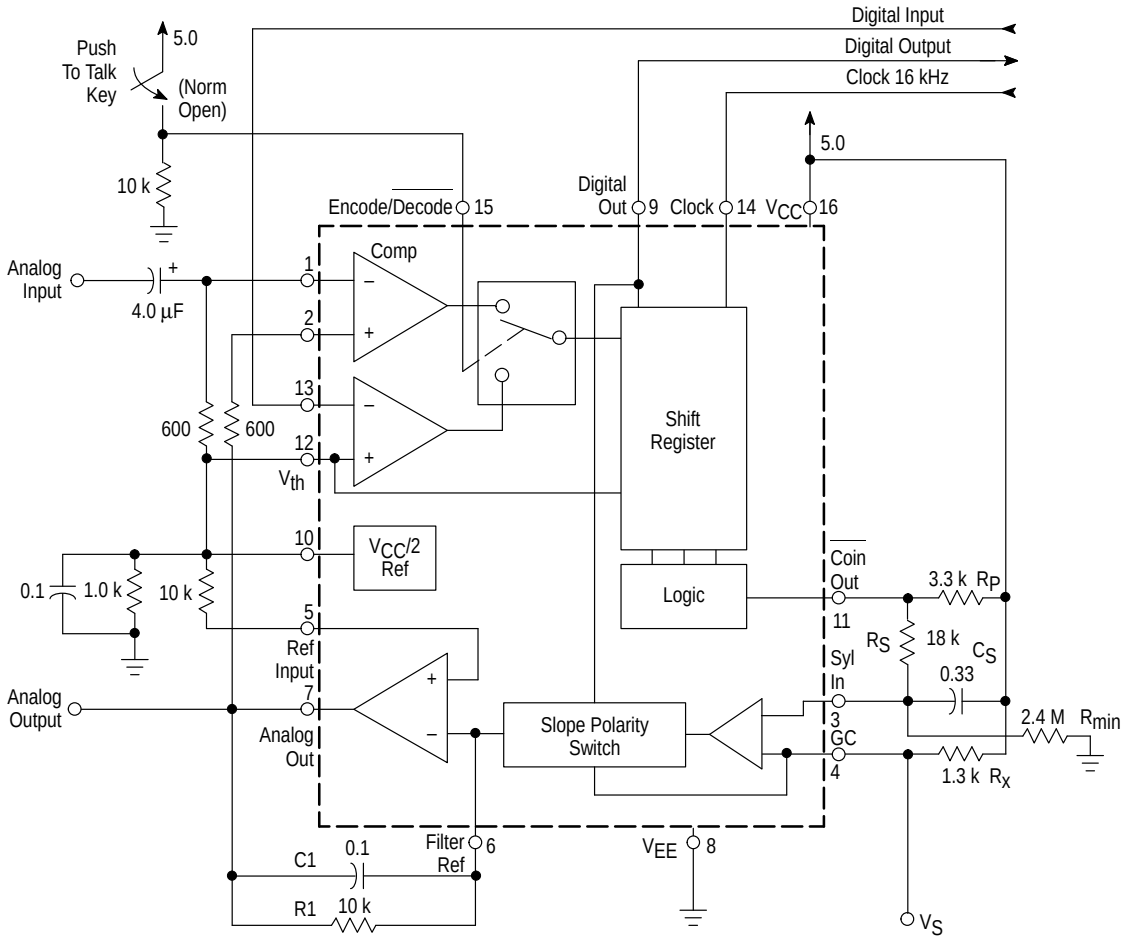
The simplicity of the all 1s, all 0s algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus, a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm operates only on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus, the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

Figure 15. 16 kHz Simplex Voice Codec
(Using MC34115, Single–Pole Companding and Single Integration)



APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC34115 is shown in Figure 15. This IC is a general purpose CVSD building block which allows the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC34115. There are six design considerations involved in designing these basic CVSD building blocks into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Selection of loop gain
3. Selection of minimum step size
4. Design of integration filter transfer function
5. Design of syllabic filter transfer function
6. Design of low pass filter at the receiver

The circuit in Figure 15 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 4 and 5 are reduced to their simplest form. The syllabic and integration filters are both single–pole networks. The selection of items 1 through 3 govern the codec performance.

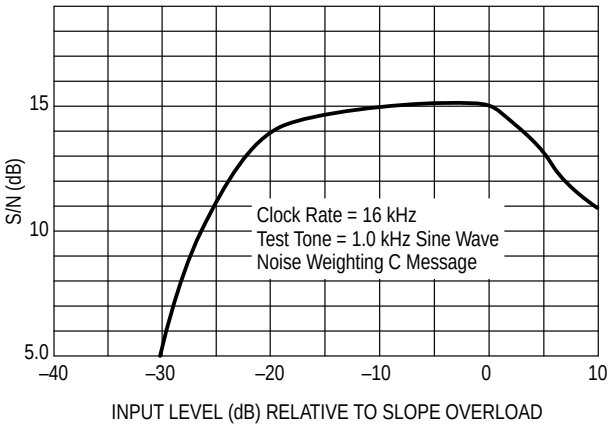
Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13 and 14) from analog signal paths (Pins 1 to 7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications, the circuit in Figure 15 may be operated anywhere from 9.6 to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 15 typically produces the S/N performance shown in Figure 16. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4–wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32 k bits and above.

Figure 16. Signal–to–Noise Performance with Single Integration, Single–Pole and Companding at 16 k Bits (Typical)



Selection of Loop Gain

The gain of the circuit in Figure 15 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus, the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1.0 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6.0 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 15, a single–pole of 160 Hz is used.

$$R1 = 10\ k\Omega,\ C1 = 0.1\ \mu F$$

$$\frac{V_O}{I_i} = \frac{1}{C\left(S + \frac{1}{RC}\right)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\ \pi f$$

$$10^3 = \omega_o = 2\ \pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single–pole response from 300 to 3.0 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_O}{R} + C\frac{dV_O}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 V. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1.0 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2\ (10\ k\Omega)} + \frac{0.1\ \mu F\ (1.1)}{0.125\ ms} = 0.935\ mA$$

* The maximum voltage across R when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25\ (V_{CC})\ \frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 15 is idle channel step size. With no input signal, the digital output becomes a one–zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC34115 is tested to ensure that a 20 mVpp minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one–zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1 – 0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 15) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_O}{R} + C\frac{dV_O}{dt}$$

For values of V_O near $V_{CC}/2$ the V_O/R term is negligible; thus:

$$I_i = C_S\frac{\Delta V_O}{\Delta T}$$

where ΔT is the clock period and ΔV_O is the desired peak–to–peak value of the idle output. For a 16 k bit system using the circuit in Figure 15:

$$I_i = \frac{0.1\ \mu F\ 20\ mV}{62.5\ \mu s} = 32\ \mu A$$

The voltage on C_S which produces a 32 μA current is determined by the value of R_X.

$$I_i R_X = V_S min;\ for\ 32\ \mu A,\ V_S min = 41.6\ mV$$

In Figure 15 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\ \frac{R_S}{R_S + R_{min}} = V_S min \quad R_{min} \simeq 2.4\ M\Omega$$

Having established these three parameters – clock rate, loop gain and minimum step size – the encoder circuit in Figure 15 will function at near optimum performance for input levels around 0 dBm.

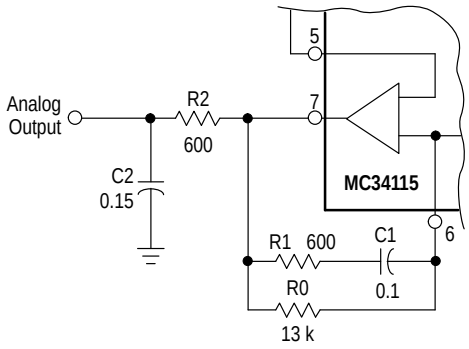
Integration Filter Design

The circuit in Figure 15 uses a single–pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 15 by 1.0 or 2.0 dB by using a two–pole integration network. The improved circuit is shown in Figure 17.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1.0 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1.0 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low–pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2.0 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low–pass filter which breaks at about 2.5 kHz.) The two–pole network in Figure 17 has a transfer function of:

$$\frac{V_O}{I_i} = \frac{R0R1\left(S + \frac{1}{R1C1}\right)}{R2C2(R0 + R1)\left(S + \frac{1}{(R0+R1)C1}\right)S + \left(\frac{1}{R2C2}\right)}$$

Figure 17. Improved Filter Configuration



NOTE: These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Thus, the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 17 represent one implementation of the telephony filter requirement.

The selection of the two–pole filter network affects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_O}{R0} + \left(\frac{R2C2}{R0} + \frac{R1C1}{R0} + C1\right)\frac{\Delta V_O}{\Delta T} + \left(R2C2C1 + \frac{R1C1R2C2}{R0}\right)\frac{\Delta V_O{}^2}{\Delta T^2}$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 15 is a simple single–pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

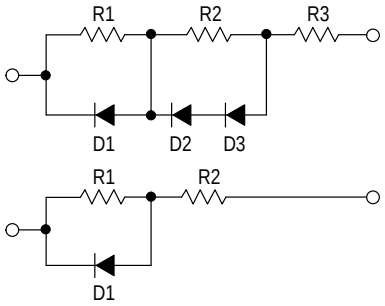
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} – V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor–diode networks are shown in Figure 18.

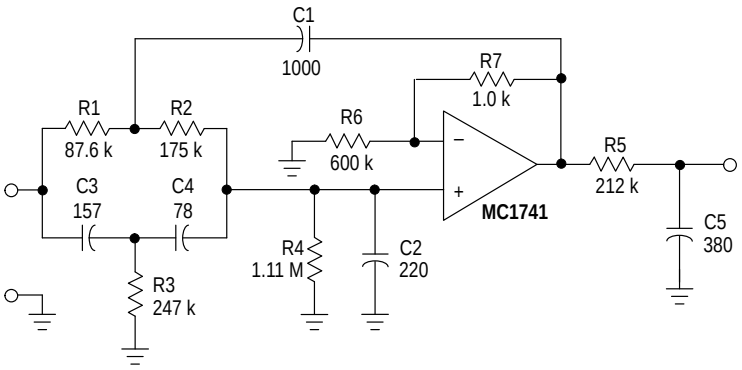
Figure 18. Resistor–Diode Networks



Output Low Pass Filter

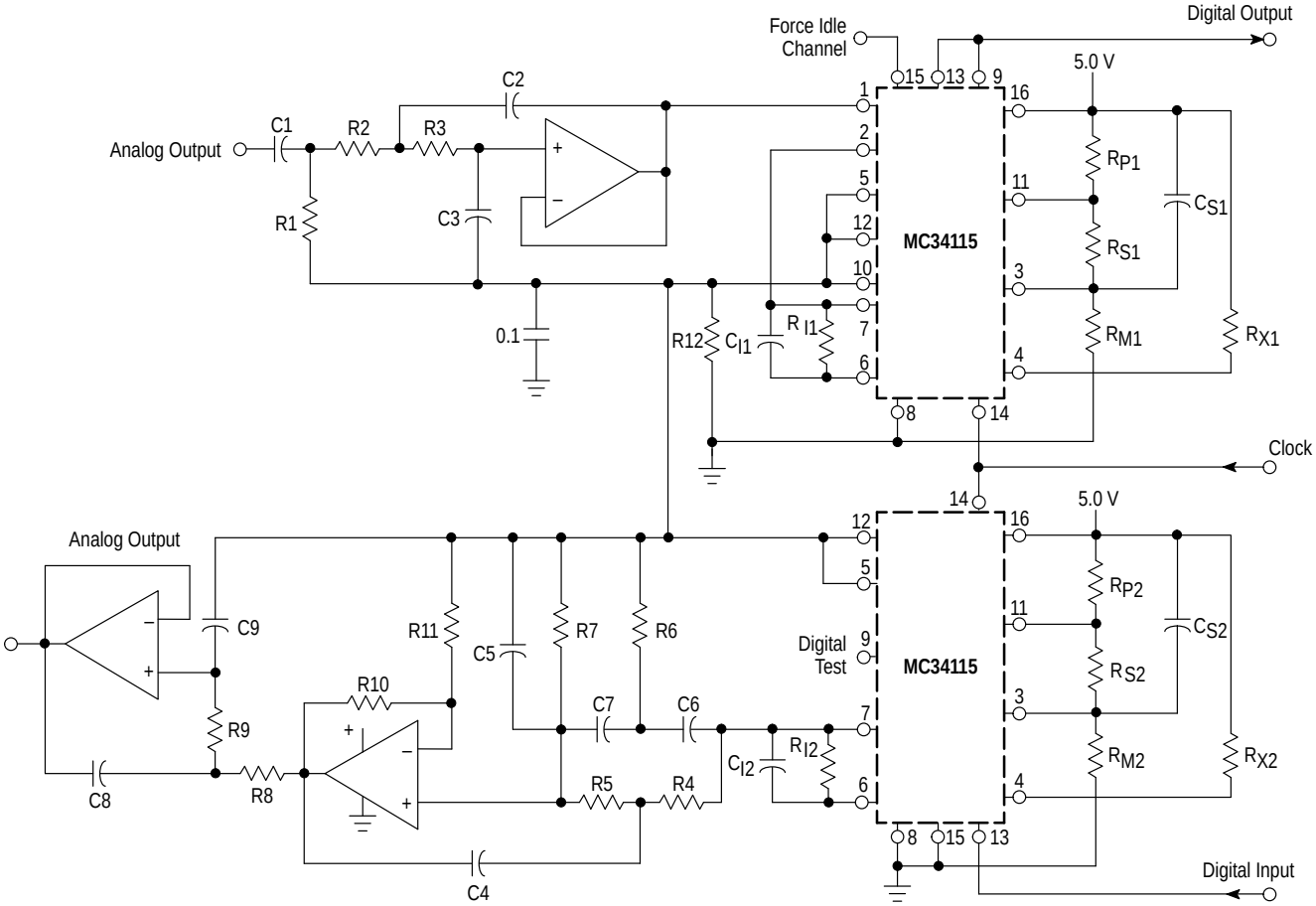
A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 19 provides excellent performance for 12 kHz to 40 kHz systems.

Figure 19. High Performance Elliptic Filter for CVSD Output



Designed for 0.28 dB ripple in the pass band
ω_n = 3.0 kHz
ω_S = ≅ 6.0 kHz
AdB at ω_S and above 29.5 dB

Figure 20. Full Duplex/16 k Bit CVSD Voice Codec



Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1.0 kΩ
R_{M1}, R_{M2} – 10 MΩ
Minimum step size = 20 mV
C_{S1}, C_{S2} – 0.05 μF
C_{I1}, C_{I2} – 0.05 μF
2 MC34115
1 MC3403 (or MC3406)

NOTE: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6.0 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9.0 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

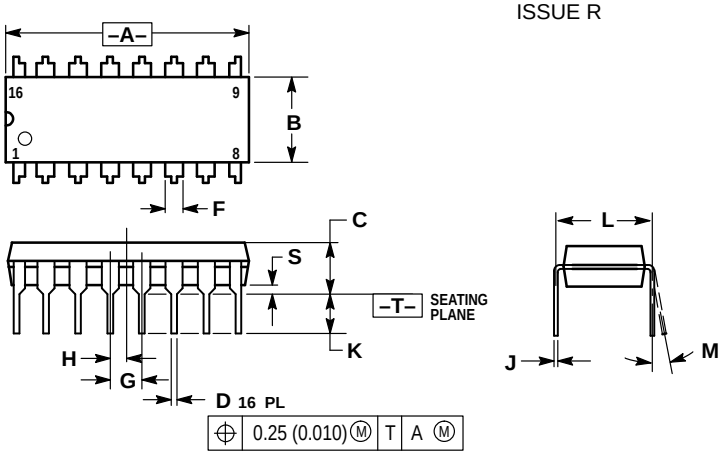
R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 Ω
R11 – 72 kΩ

C1 – 3.3 μF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

NOTE: All Res. 0.1% to 1%
All Cap. 1%

OUTLINE DIMENSIONS

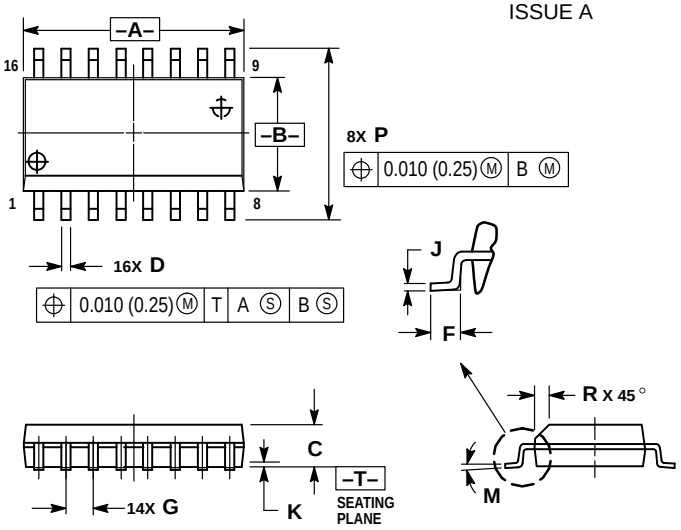
P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02
(SO–16L)
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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