

HM6264A Series

8192-word × 8-bit High Speed CMOS Static RAM

Features

- Low-power standby
 - 0.1 mW (typ)
 - 10 μW (typ) L-/LL-version
- Low power operation
 - 15 mW/MHz (typ)
- Fast access time
 - 100/120/150 ns (max)
- Single +5 V supply
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle time
- Common data input and output, three-state output
- Directly TTL compatible
 - All inputs and outputs
- Battery back up operation capability (L-/LL-version)

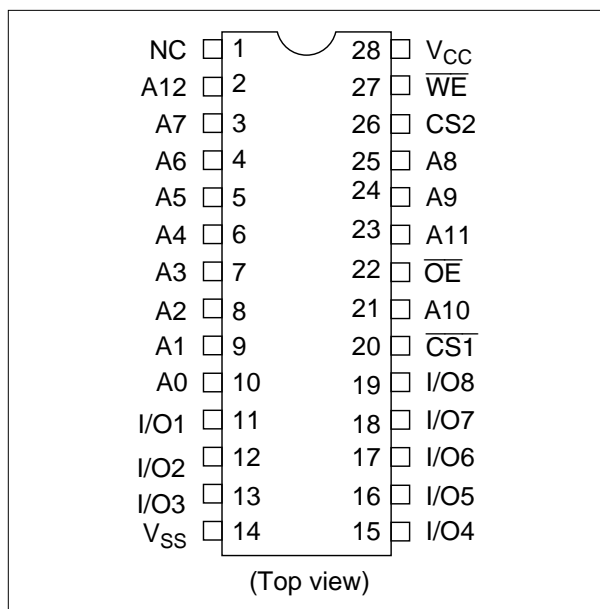
Ordering Information

| Type No. | Access time | Package |
|---------------|-------------|-------------------------------------|
| HM6264AP-10 | 100 ns | 600-mil, 28-pin plastic DIP (DP-28) |
| HM6264AP-12 | 120 ns | |
| HM6264AP-15 | 150 ns | |
| HM6264ALP-10 | 100 ns | |
| HM6264ALP-12 | 120 ns | |
| HM6264ALP-15 | 150 ns | |
| HM6264ALP-10L | 100 ns | |
| HM6264ALP-12L | 120 ns | |
| HM6264ALP-15L | 150 ns | |

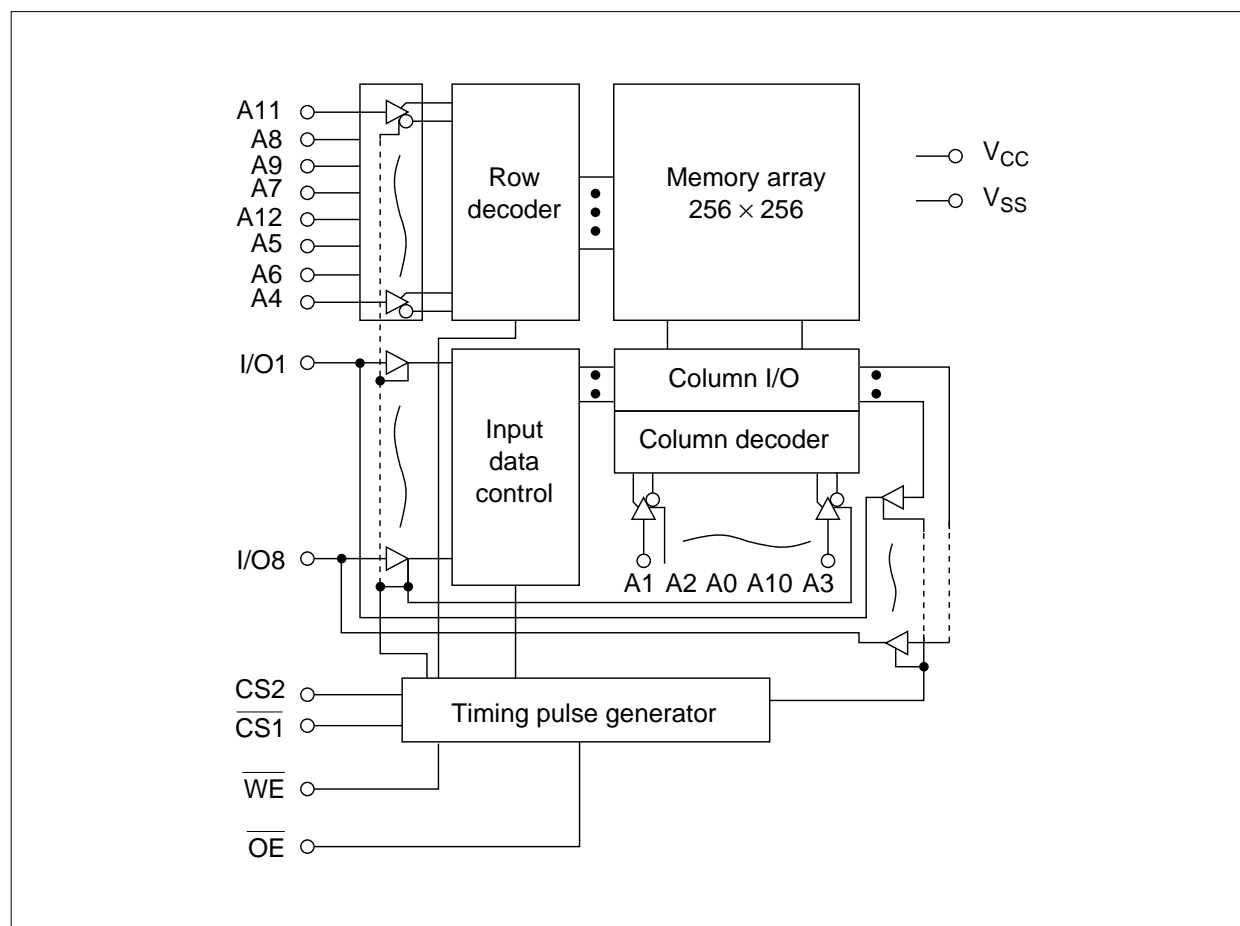
| Type No. | Access time | Package |
|----------------|-------------|--------------------------------------|
| HM6264ASP-10 | 100 ns | 300-mil, 28-pin plastic DIP (DP-28N) |
| HM6264ASP-12 | 120 ns | |
| HM6264ASP-15 | 150 ns | |
| HM6264ALSP-10 | 100 ns | |
| HM6264ALSP-12 | 120 ns | |
| HM6264ALSP-15 | 150 ns | |
| HM6264ALSP-10L | 100 ns | |
| HM6264ALSP-12L | 120 ns | |
| HM6264ALSP-15L | 150 ns | |
| HM6264AFP-10 | 100 ns | 28-pin plastic SOP *1 (FP-28D/DA) |
| HM6264AFP-12 | 120 ns | |
| HM6264AFP-15 | 150 ns | |
| HM6264ALFP-10 | 100 ns | |
| HM6264ALFP-12 | 120 ns | |
| HM6264ALFP-15 | 150 ns | |
| HM6264ALFP-10L | 100 ns | |
| HM6264ALFP-12L | 120 ns | |
| HM6264ALFP-15L | 150 ns | |

Note: 1. T is added to the end of the type number for a SOP of 3.00 mm (max) thickness.

Pin Arrangement



Block Diagram



Truth Table

| \overline{WE} | $\overline{CS1}$ | CS2 | \overline{OE} | Mode | I/O pin | V _{CC} current | Note |
|-----------------|------------------|-----|-----------------|------------------------------|---------|------------------------------------|---------------|
| × | H | × | × | Not selected (power down) | High Z | I _{SB} , I _{SB1} | |
| × | × | L | × | | High Z | I _{SB} , I _{SB1} | |
| H | L | H | H | Output disabled | High Z | I _{CC} | |
| H | L | H | L | Read | Dout | I _{CC} | Read cycle |
| L | L | H | H | Write | Din | I _{CC} | Write cycle 1 |
| L | L | H | L | Write | Din | I _{CC} | Write cycle 2 |

Note: ×: Don't care.

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|----------------------------------|-------------------|-----------------|------|
| Terminal voltage *1 | V _T | -0.5 *2 to +7.0 | V |
| Power dissipation | P _T | 1.0 | W |
| Operating temperature | T _{opr} | 0 to +70 | °C |
| Storage temperature | T _{stg} | -55 to +125 | °C |
| Storage temperature (under bias) | T _{bias} | -10 to +85 | °C |

Notes: 1. With respect to V_{SS}.
2. -3.0 V for pulse width ≤ 50 ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-----------------|---------|-----|-----|------|
| Supply voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| | V _{SS} | 0 | 0 | 0 | V |
| Input voltage | V _{IH} | 2.2 | — | 6.0 | V |
| | V _{IL} | -0.3 *1 | — | 0.8 | V |

Note: 1. -3.0 V for pulse width ≤ 50 ns

DC and Operating Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Test condition |
|--------------------------------|-------------|-----|----------------|------------------|---------------|---|
| Input leakage current | $ I_{LI} $ | — | — | 2 | μA | $V_{in} = V_{SS}\text{ to }V_{CC}$ |
| Output leakage current | $ I_{LO} $ | — | — | 2 | μA | $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}\text{ to }V_{CC}$ |
| Operating power supply current | I_{CCDC} | — | 7 | 15 | mA | $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{ mA}$ |
| Average operating current | I_{CC1} | — | 30 | 45 ⁵ | mA | Min. cycle, duty = 100%, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{ mA}$ |
| | I_{CC2} | — | 3 | 5 | mA | Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0\text{ mA}$, $\overline{CS1} \leq 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$, $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$ |
| Standby power supply current | I_{SB} | — | 1 | 3 | mA | $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ |
| | $ISB1^{*2}$ | — | 0.02 | 2 | mA | $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$ or |
| | | — | 2 ³ | 100 ³ | μA | $0\text{ V} \leq CS2 \leq 0.2\text{ V}$, $0\text{ V} \leq V_{in}$ |
| | | — | 2 ⁴ | 50 ⁴ | | |
| Output voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 2.1\text{ mA}$ |
| | V_{OH} | 2.4 | — | — | V | $I_{OH} = -1.0\text{ mA}$ |

- Notes:
1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = 25^\circ\text{C}$ and not guaranteed.
 2. V_{IL} min = -0.3 V
 3. These characteristics are guaranteed only for the L-version.
 4. These characteristics are guaranteed only for the LL-version.
 5. For 120 ns/150 ns version.
 6. For 100 ns version.

Capacitance ($f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$)*¹

| Parameter | Symbol | Typ | Max | Unit | Test condition |
|--------------------------|-----------|-----|-----|------|------------------------|
| Input capacitance | C_{in} | — | 5 | pF | $V_{in} = 0\text{ V}$ |
| Input/output capacitance | $C_{I/O}$ | — | 7 | pF | $V_{I/O} = 0\text{ V}$ |

- Note:
1. This parameter is sampled and is not 100% tested.

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }+70^\circ\text{C}$)

AC Test Conditions:

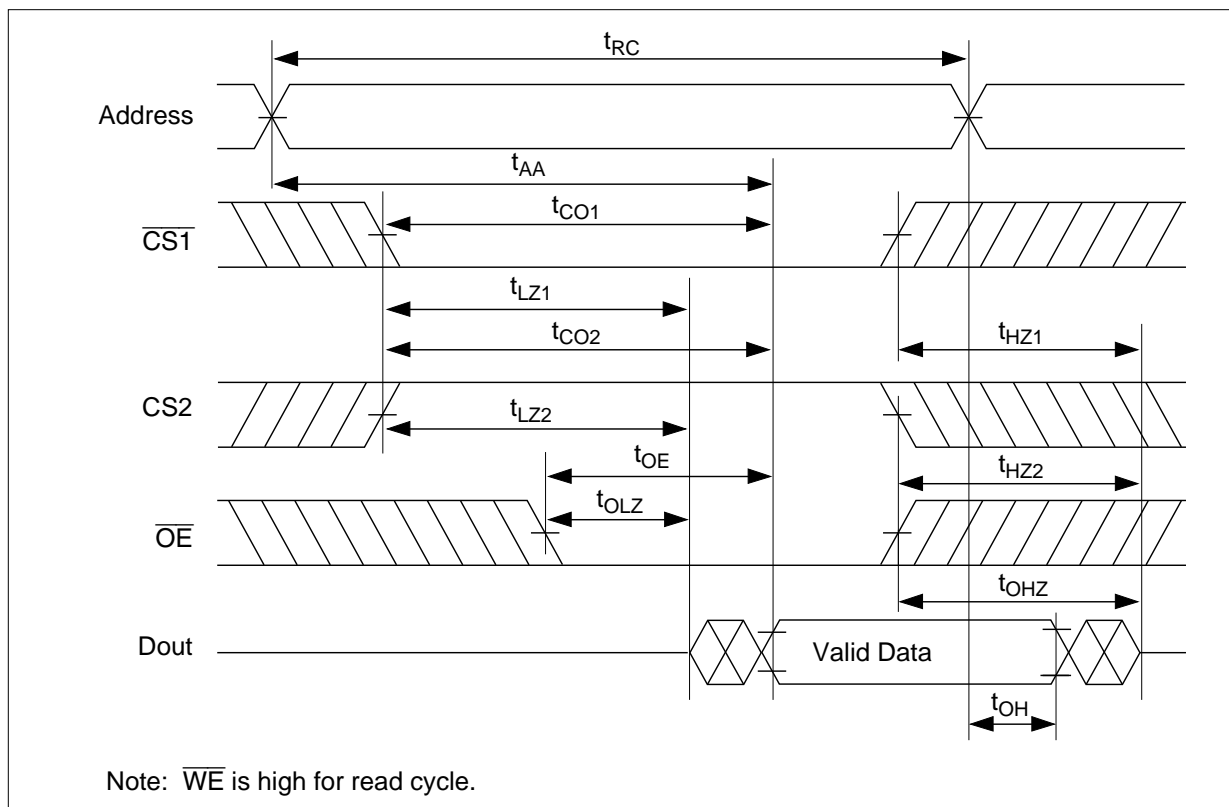
- Input pulse levels: 0.8 V/2.4 V
- Input rise and fall time: 10 ns
- Input timing reference level: 1.5 V
- Output timing reference level
 - HM6264A-10: 1.5 V
 - HM6264A-12/15: 0.8 V/2.0 V
- Output load: 1 TTL gate and C_L (100 pF) (including scope and jig)

Read Cycle

| Parameter | Symbol | HM6264A-10 | | HM6264A-12 | | HM6264A-15 | | Unit |
|--------------------------------------|----------------------------|------------|-----|------------|-----|------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Read cycle time | t_{RC} | 100 | — | 120 | — | 150 | — | ns |
| Address access time | t_{AA} | — | 100 | — | 120 | — | 150 | ns |
| Chip selection to output | $\overline{CS1}$ t_{CO1} | — | 100 | — | 120 | — | 150 | ns |
| | CS2 t_{CO2} | — | 100 | — | 120 | — | 150 | ns |
| Output enable to output valid | t_{OE} | — | 50 | — | 60 | — | 70 | ns |
| Chip selection to output in low Z | $\overline{CS1}$ t_{LZ1} | 10 | — | 10 | — | 15 | — | ns |
| | CS2 t_{LZ2} | 10 | — | 10 | — | 15 | — | ns |
| Output enable to output in low Z | t_{OLZ} | 5 | — | 5 | — | 5 | — | ns |
| Chip deselection to output in high Z | $\overline{CS1}$ t_{HZ1} | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| | CS2 t_{HZ2} | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| Output disable to output in high Z | t_{OHZ} | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| Output hold from address change | t_{OH} | 10 | — | 10 | — | 10 | — | ns |

- Notes
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs to achieve the open circuit condition and are not referred to output voltage levels.
 2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.

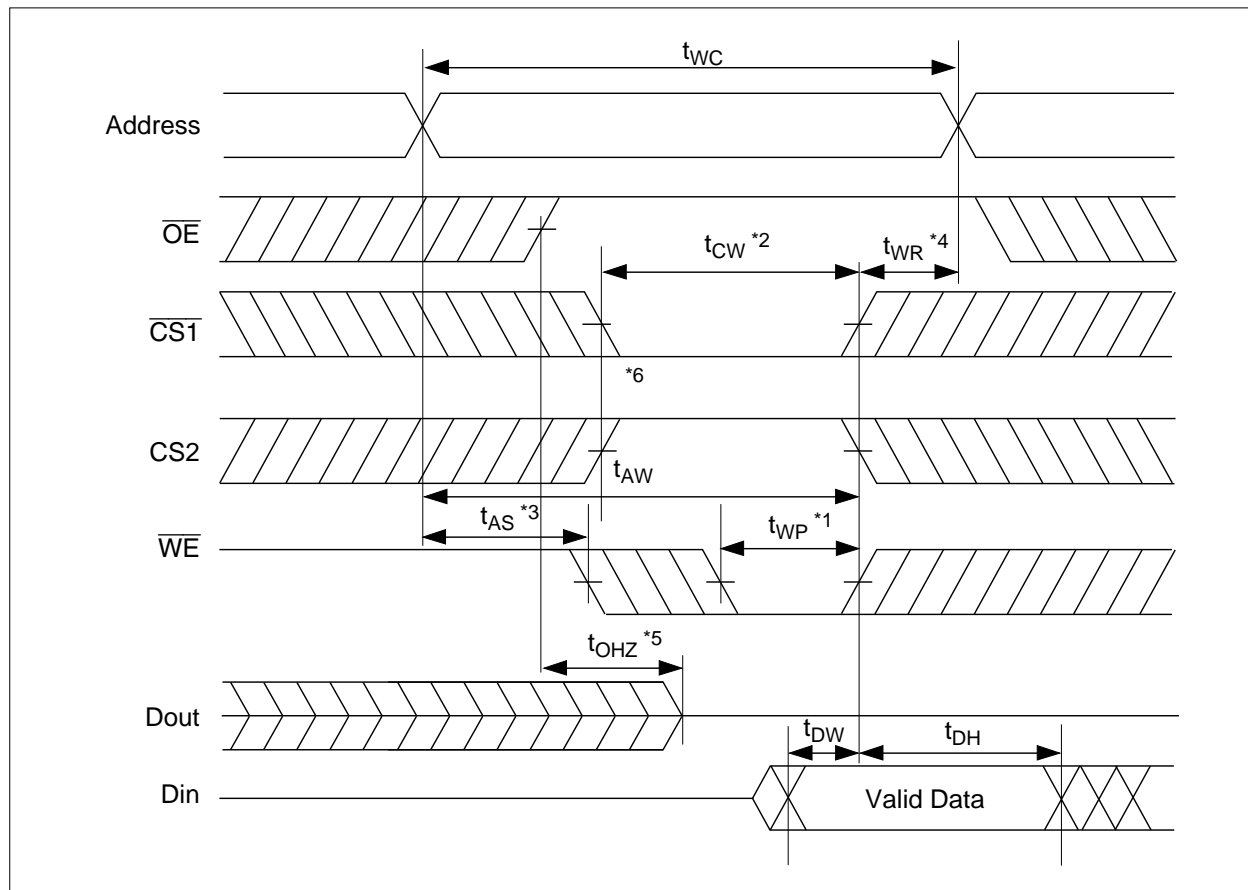
Read Timing Waveform

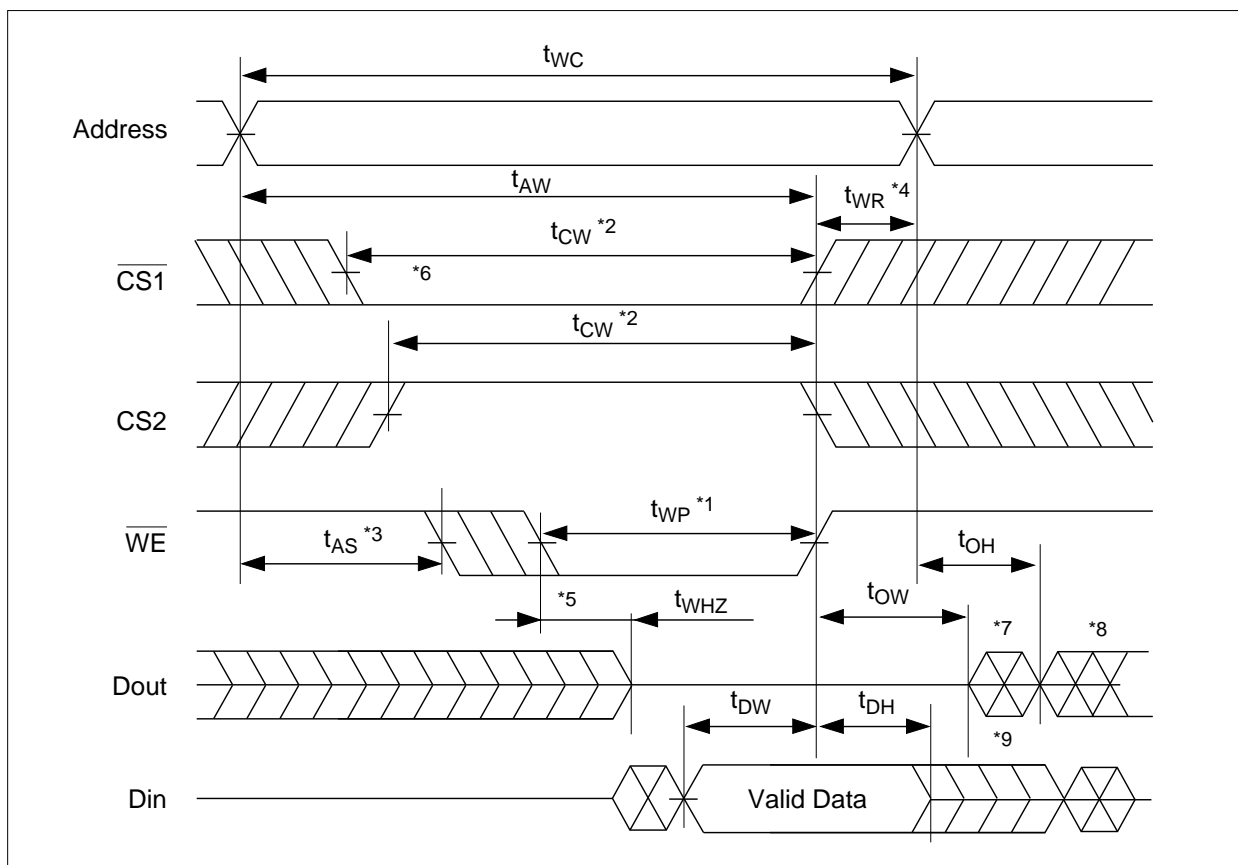


Write Cycle

| Parameter | Symbol | HM6264A-10 | | HM6264A-12 | | HM6264A-15 | | Unit |
|-----------------------------------|-----------|------------|-----|------------|-----|------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Write cycle time | t_{WC} | 100 | — | 120 | — | 150 | — | ns |
| Chip selection to end of write | t_{CW} | 80 | — | 85 | — | 100 | — | ns |
| Address setup time | t_{AS} | 0 | — | 0 | — | 0 | — | ns |
| Address valid to end of write | t_{AW} | 80 | — | 85 | — | 100 | — | ns |
| Write pulse width | t_{WP} | 60 | — | 70 | — | 90 | — | ns |
| Write recovery time | t_{WR} | 0 | — | 0 | — | 0 | — | ns |
| Write to output in high Z | t_{WHZ} | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| Data to write time overlap | t_{DW} | 40 | — | 40 | — | 50 | — | ns |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | 0 | — | ns |
| Output enable to output in high Z | t_{OHZ} | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| Output active from end of write | t_{OW} | 5 | — | 5 | — | 5 | — | ns |

Write Timing Waveform (1) (\overline{OE} Clock)



Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fix)

- Notes:
1. A write occurs during the overlap of a low $\overline{\text{CS1}}$, a high CS2 , and a low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS1}}$ going low, CS2 going high and $\overline{\text{WE}}$ going low. A write ends at the earliest transition among $\overline{\text{CS1}}$ going high, CS2 going low and $\overline{\text{WE}}$ going high. Time t_{WP} is measured from the beginning of write to the end of write.
 2. t_{CW} is measured from the later of $\overline{\text{CS1}}$ going low or CS2 going high to the end of write.
 3. t_{AS} is measured from the address valid to the beginning of write.
 4. t_{WR} is measured from the earliest of $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high or CS2 going low to the end of the write cycle.
 5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
 6. If $\overline{\text{CS1}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ goes low, the outputs remain in high impedance state.
 7. Dout is the same phase of the latest written data in this write cycle.
 8. Dout is the read data of the next address.
 9. If $\overline{\text{CS1}}$ is low and CS2 is high during this period, I/O pins are in the output state. Input signals of opposite phase to the outputs must not be applied to I/O pins

Low V_{CC} Data Retention

In data retention mode, CS2 controls the address, WE, CS1, OE, and the Din buffer. If CS2 controls the data retention mode, V_{in} (for these inputs) can be in the high impedance state. If CS1 controls the data retention mode, CS2 must satisfy either

$CS2 \geq V_{CC} - 0.2 \text{ V}$ or $CS2 \leq 0.2 \text{ V}$. The other input levels (address, WE, OE, I/O) can be in the high impedance state.

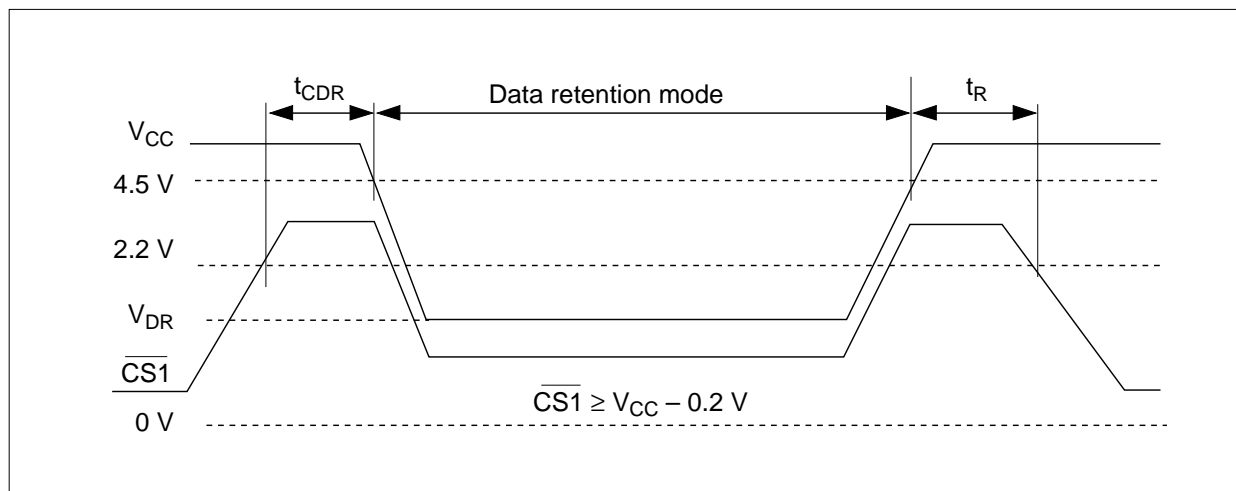
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only L/LL-version.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Condition |
|--------------------------------------|------------|---------------|-----------------|------------------|---------------|---|
| V_{CC} for data retention | V_{DR} | 2.0 | — | — | V | $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$, or $CS2 \leq 0.2 \text{ V}$ |
| Data retention current | I_{CCDR} | — | 1 ^{*1} | 50 ^{*1} | μA | $V_{CC} = 3.0 \text{ V}$, $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$, or $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$, $0 \text{ V} \leq V_{in}$ |
| Chip deselect to data retention time | t_{CDR} | 0 | — | — | ns | See retention waveform |
| Operation recovery time | t_R | t_{RC}^{*3} | — | — | ns | See retention waveform |

- Notes:
- V_{IL} min = -0.3 V , $20 \mu\text{A}$ max at $T_a = 0$ to 40°C . These characteristics are guaranteed only for the L-version.
 - V_{IL} min = -0.3 V , $10 \mu\text{A}$ max at $T_a = 0$ to 40°C . These characteristics are guaranteed only for the LL-version.
 - t_{RC} = Read cycle time.

Low V_{CC} Data Retention Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Waveform (2) ($\overline{CS2}$ Controlled)

