M51366SP

PLL-SPLIT VIF/SIF

DESCRIPTION

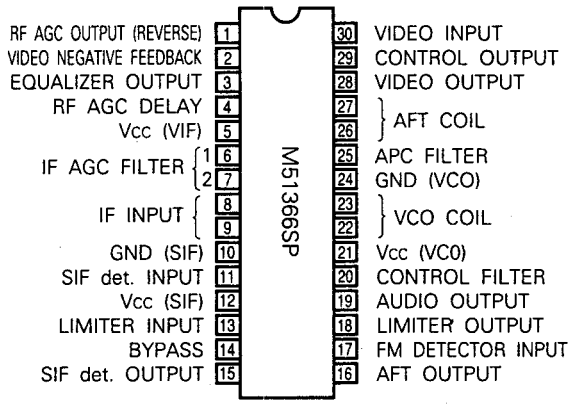
The M51366SP is a semiconductor integrated circuit consisting of IF signal processor suitable for color TV sets and VCRs with AV.

The circuit includes VIF amplifier, Video detector, VCO, APC detector, AFT, video equalizer, IF/RF AGC, SIF detector, SIF limiter and FM detector functions.

FEATURES

- A full synchronous detector circuit using PLL as video detector provides excellent DG, DP, 920 kHz beat and cross color characteristics.
- The PLL-SPLIT method in which video IF and audio IF signal processings are separated and VCO output is used to obtain intercarrier provides good sound sensitivity and reduces buzz. In consumer sets, intercarrier is also available from the video detector output.
- Built-in video equalizer is suitable for VCRs and color TV sets equipped with video output terminals.
- The quadrature detector circuit for FM detector has good linearity, and it is possible to eliminate necessity of adjustment.
- The AGC works fast because of the 2-stage AGC filter.

PIN CONFIGURATION (TOP VIEW)



Outline 30P4B

APPLICATIONS

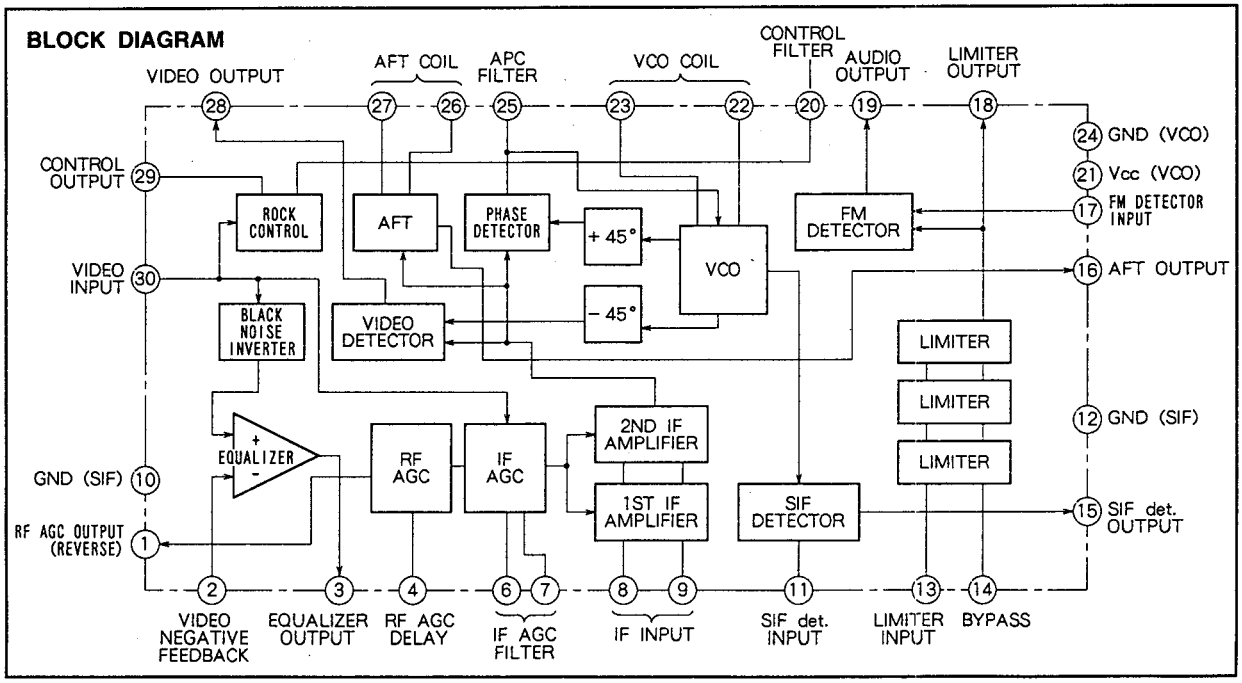
TV sets, VCR tuners

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 8 ~ 10V

Rated supply voltage 9V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
P_d	Power dissipation	1250	mW
T_{opr}	Operating temperature	−20~75	℃
T_{stg}	Storage temperature	−40~125	℃
Surge	Electrostatic discharge	±200	V

ELECTRICAL CHARACTERISTICS (Ta = 25℃, VCC = 9V, unless otherwise noted)

VIF SECTION

Symbol	Parameter	Test circuit	Test point	Test conditions: Input signal VIF	Input signal SIF1	External power supply(V) V_1	V_7	V_{20}	* Switches should usually be set to 1	Limits Min.	Typ.	Max.	Unit
I_{CC} (VIF)	Circuit current (VIF)	1	A1	–	–	3	–	–	SW1 = 2,SW2 = 3	33	45	57	mA
V_{28}	Video detector output DC voltage 1	1	TP9	–	–	3	0	–	SW2 = 3,SW3 = 2	3.4	3.75	4.1	V
V_3	Video detector output DC voltage 2	1	TP2	–	–	3	0	–	SW2 = 3,SW3 = 2	4.3	4.7	5.1	V
$V_{O\ det1}$	Video detector output 1	1	TP9	SG1	–	3	–	–	SW2 = 3	1.15	1.45	1.75	V_{P-P}
$V_{O\ det2}$	Video detector output 2	1	TP2	SG1	–	3	–	–	SW2 = 3	1.75	2.2	2.65	V_{P-P}
P/N	Video S/N	1	TP10	SG2	–	3	–	–	SW2 = 3,SW6 = 2 (Note 1)	50	58		dB
Bw	Video frequency characteristics	1	TP9	SG3	–	3	–	–	SW2 = 3 (Note 2)	5.0	6.5		MHz
$V_{in\ (min)}$	Input sensitivity	1	TP9	SG4	–	3	–	–	SW2 = 3 (Note 3)		46	51	dBμ
$V_{in\ (max)}$	Maximum allowable input	1	TP9	SG5	–	3	–	–	SW2 = 3 (Note 4)	107	110		dBμ
GR	AGC control range	1	–	–	–	–	–	–	(Note 5)	58	64		dB
V_{IH}	IF AGC maximum voltage	1	TP3	–	–	3	–	–	SW2 = 3	6.5	8.6		V
$V_{I\ (80dB\mu)}$	IF AGC voltage(80dBμ)	1	TP3	SG6	–	3	–	–	SW2 = 3	4.1	4.7	5.3	V
V_{IL}	IF AGC minimum voltage		TP3	SG7	–	3	–	–	SW2 = 3	3.4	3.9	4.4	V
$V_{O\ SIF-1}$	SIF det, 4.5MHz output (100dBμ)	1	TP4	SG2	SG8	3	–	–	SW2 = 3	104	109	114	dBμ
$V_{O\ SIF-2}$	SIF det, 4.5MHz output (80dBμ)	1	TP4	SG2	SG9	3	–	–	SW2 = 3	90	96	101	dBμ
V_{16}	AFT output voltage	1	TP5	–	–	3	0	–	SW2 = 3	3.2	4.3	5.4	V
μ	AFT detector sensitivity	1	TP5	SG10	–	3	–	–	SW2 = 3 (Note 6)	48	70	92	mV/kHz
V_{16H}	AFT maximum voltage	1	TP5	SG10	–	3	–	–	SW2 = 3 (Note 7)	8	8.7		V
V_{16L}	AFT minimum voltage	1	TP5	SG10	–	3	–	–	SW2 = 3 (Note 8)		0.38	1.0	V
V_{1H}	RF AGC maximum voltage	1	TP1	SG2	–	2	–	–	SW2 = 3	6.9	7.8		V
V_{1L}	RF AGC minimum voltage	1	TP1	SG2	–	4	–	–	SW2 = 3		0	1.0	V
CL-U1	Capture range (U)	1	TP9	SG11	–	3	–	–	SW2 = 3 (Note 9)	0.5	1.0		MHz
CL-L1	Capture range (L)	1	TP9	SG11	–	3	–	–	SW2 = 3 (Note 10)	1.2	1.7		MHz
CL-T	Capture range (T)	1	–	–	–	–	–	–	(Note 11)	2.0	2.7		MHz
CL-U2	Capture range (U)	1	TP9	SG11	–	3	–	–	SW2 = 3,SW5 = 2 (Note 9)	0.45	1.0	1.60	MHz
CL-L2	Capture range (L)	1	TP9	SG11	–	3	–	–	SW2 = 3,SW5 = 2 (Note 10)	0.95	1.5	2.05	MHz
V_{20TH}	Lock detector threshold voltage	1	TP8	–	–	3	5	Variable	SW2 = 3,SW3,4,5 = 2 (Note 12)	3.6	4.0	4.4	V
V_{29L}	Minimum voltage at pin㉙	1	TP8	–	–	3	5	Variable	SW2 = 3,SW3,4,5 = 2 (Note 13)		0.15	0.5	V

VIF SECTION (cont.)

Symbol	Parameter	Test circuit	Test point	Test conditions: Input signal VIF	Input signal SIF1	External power supply(V) V_1	V_7	V_{20}	* Switches should usually be set to 1	Limits Min.	Typ.	Max.	Unit
FC1	EQ frequency characteristics 1	1	TP9 TP2	SG12	–	3	–	–	SW2 = 3 (Note 14)	2.0	3.5	5.0	dB
FC2	EQ frequency characteristics 2	1	TP9 TP2	SG13	–	3	–	–	SW2 = 3 (Note 14)	4.2	5.7	7.2	dB
FC3	EQ frequency characteristics 3	1	TP9 TP2	SG14	–	3	–	–	SW2 = 3 (Note 14)	9.5	12.0	14.5	dB
IM	Intermodulation	1	TP9	SG15	–	3	Variable	–	SW2 = 3,SW3 = 2 (Note 15)	30	35		dB
DG	DG	1	TP9	SG16	–	3	–	–	SW2 = 3 (Note 16)		2	5	%
DP	DP	1	TP9	SG16	–	3	–	–	SW2 = 3 (Note 16)		2	5	deg.
V_{BTH}	Black spot inverter threshold level	1	TP2	SG1	–	3	Variable	–	SW2 = 3,SW3 = 2 (Note 17)	1.0	1.4	1.8	V
V_{BCL}	Black spot inverter clamp level	1	TP2	SG1	–	3	Variable	–	SW2 = 3,SW3 = 2 (Note 17)	3.7	4.2	4.7	V
V_{SYNC}	Sync tip level at pin ③	1	TP2	SG2	–	3	–	–	SW2 = 3	1.8	2.2	2.6	V
Rin (V)	VIF input resistance	2		90dBμ	–	3	–	–			0.95		kΩ
Cin (V)	VIF input capacitance	2		90dBμ	–	3	–	–			5		pF
Rin (S1)	SIF1 input resistance	2		–	90dBμ	3	–	–			2.1		kΩ
Cin (S1)	SIF1 intput capacitance	2		–	90dBμ	3	–	–			2.5		pF

SIF SECTION

Symbol	Parameter	Test circuit	Test point	Test conditions: Input signal SIF2	External power supply(V) V_1	V_7	V_{20}	* Switches should usually be set to 1	Limits Min.	Typ.	Max.	Unit
Icc (SIF)	Circuit current (SIF)	1	A2	–	0	–	–	SW1 = 3,SW2 = 2	5.0	7.2	9.4	mA
V_{19}	AF output DC voltage	1	TP6	–	0	–	–	SW1 = 3	4.1	4.7	5.3	V
V_{OAFMAX}	Maximum AF output	1	TP6	SG17	0	–	–	SW1 = 3	530	680	830	mVrms
THD_{AF}	AF output distortion	1	TP6	SG21	0	–	–	SW1 = 3		0.4	1.2	%
Vin (lim)	Input limiting sensitivity	1	TP6	SG18	0	–	–	SW1 = 3 (Note 18)		38	46	dBμ
AMR	AMR	1	TP6	SG19	0	–	–	SW1 = 3 (Note 19)	50	60		dB
S/N	AF S/N	1	TP6	SG20	0	–	–	SW1 = 3 (Note 20)	60	75		dB

ELECTRICAL CHARACTERISTICS TEST METHOD

Note1. Video S/N "P/N"

a. Input SG6 in VIF IN.

b. The noise appearing at pin ㉘ is determined by measuring the r.m.s. voltage at TP10 through low pass filter (–3dB at 5MHz).

c. $P/N = 20 \log \left\{ \frac{\text{Vodet 1 } (V_{P\text{-}P}) \times 0.7}{\text{noise (Vrms)}} \right\}$

where Vodet 1 denotes video detection output 1.

Note2. Video frequency characteristics "Bw"

a. Set SG3 as follows:

f_1 = 45.75MHz V_i = 90dBμ
f_2 = 45.75MHz V_i = 70dBμ
} mixed signal

b. Measure element of 1MHz at TP9 at this time and it is defined as V_1.

c. Decrease the frequency until element (f_1–f_2) becomes 3dB smaller than V_1 and then, read the frequency.

d. Bw = 45.75 – f_2 (MHz)

Note3. Input sensitivity "Vin (min)"

a. Input SG4 in VIF IN.

b. Decrease the SG4 level and the level at which detector output at pin ㉘ reaches 3dB smaller than Vodet 1 is defined as input sensitivity.

Note4. Maximum allowable input "$V_{in\ (max)}$"

a. Set SG5 to 90dBμ and input it in VIF IN.

b. Detector output at pin ㉘ at this time is defined as V_2.

c. Increase the SG5 and the voltage at which detector output reaches 3dB smaller than V_2 is defined as maximum allowable input.

Note5. AGC control range "GR"

a. AGC control range is defined as follows:

GR = Maximum allowable input – Input sensitivity

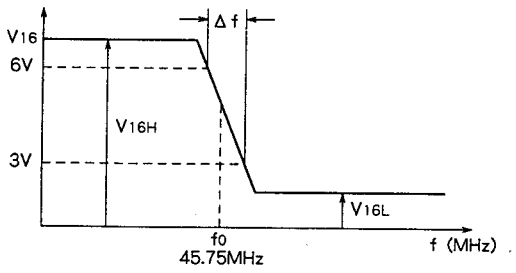
Note6. AFT detector sensitivity "μ"

a. Input SG10 in VIF IN.

b. Measure difference of frequency between 3.0V and 6.0V of DC voltage at TP5 and it is defined as Δf.

c. AFT detector sensitivity μ is defined as follows:

$$\mu = \frac{3000mV}{\Delta f\ (kHz)}\ (mV/kHz)$$



Note7. AFT maximum voltage "V_{16H}"

a. Maximum DC voltage in the above figure is defined as V_{16H}.

Note8. AFT minimum voltage "V_{16L}"

a. Minimum DC voltage in the above figure is defined as V_{16L}.

Note9. Capture range (U) "CL–U–1," "CL–U–2"

a. Input SG11 in VIF IN and increase the frequency till VCO lock is released.

b. Decrease the frequency of SG11 and the frequency at which VCO locks again is defined as fv (MHz).

c. Capture range (U) is defined as fv – 45.75 (MHz).

Note10. Capture range (L) "CL–L–1," "CL–L–2"

a. Input SG11 in VIF IN and decrease the frequency until VCO lock is released.

b. Increase the frequency of SG11 and the frequency at which VCO locks again is defined as f_L (MHz).

c. Capture range (L) is defined as 45.75 – f_L (MHz).

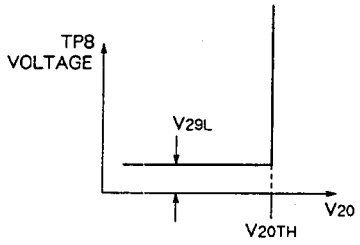
Note11. Capture range (T) "CT–T"

a. "CL–T" is defined as "CL–U–1" + "CL–L–1" (MHz).

Note12. Lock detector threshold voltage "V_{20TH}"

a. Set the voltage at V_{20} to 3V and observe TP8.

b. Increase the voltage at V_{20} and the point at which TP8 voltage changes drastically is defined as V_{20TH} (threshold 1V).



Note13. Minimum voltage at pin ㉙ "V_{29L}"

a. Minimum voltage in Note12 is defined as V_{29L}.

Note14. EQ frequency characteristics "FC1", "FC2", "FC3"

a. Input SG12, SG13 or SG14 in VIF IN.

b. Measure the level of element (f_1–f_2) at TP9 and it is defined as $V_{EQ\ IN}$ (dBμ).

c. Measure the level of element (f_1–f_2) at TP2 and it is defined as $V_{EQ\ OUT}$ (dBμ).

d. EQ frequency characteristics is defined as follows:

FC1~3 = $V_{EQ\ OUT}$ – $V_{EQ\ IN}$ (dB)

Note15. Intermodulation "IM"

a. Input SG15 in VIF IN.

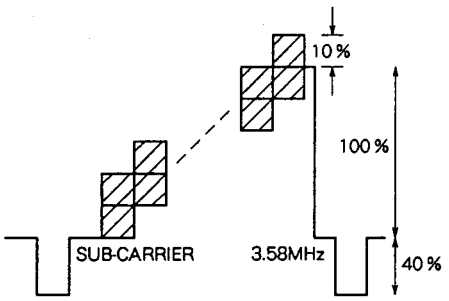
b. Observe TP9 with oscilloscope, and adjust the voltage of V_6 so that the minimum level of detector output waveform will come to 2V.

c. Observe TP9 with spectrum analyzer, and the ratio of the 920kHz level to the 3.58MHz level is defined as intermodulation.

Note16. DG, DP "DG, DP"

a. Modulated waves of SG16 is generated by 87.5% video modulation of the 10-step waves as shown in the figure below.

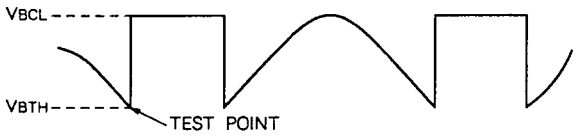
b. Measure DG and DP at TP9 with vectorscope.



Note17. Black spot inverter threshold level and clamp level "$V_{B\ TH}$, $V_{B\ CL}$"

a. Input SG1 in VIF IN.

b. By varying V_6, output the waveform as shown in the figure below to TP2 and measure each DC voltage.



Note18. Input limiting sensitivity "$V_{in\ (lim)}$"

a. Set SG18 to 80dBμ and input it in SIF2 IN.

b. Decrease the output level of SG18 until detector output at TP6 becomes 3dB smaller than $V_{O\ AF\ MAX}$. The level of SG18 at this time is defined as input limiting sensitivity.

Note19. AMR "AMR"

a. Input SG19 in SIF2 IN.

b. Measure the output voltage at TP6 and it is defined as V_{AM}.

c. AMR is defined as follows:

$$AMR = 20 \log \left\{ \frac{V_{O\ AF\ MAX}\ (mVrms)}{V_{AM}\ (mVrms)} \right\} (dB)$$

Note20. AF S/N "S/N"

a. Input SG20 in SIF2 IN.

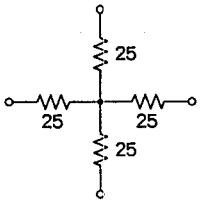
b. Measure the output voltage at TP6 and it is defined as V_N.

c. AF S/N is defined as follows:

$$S/N = 20 \log \left\{ \frac{V_{O\ AF\ MAX}\ (mVrms)}{V_N\ (mVrms)} \right\} (dB)$$

✻• Amplitude level of all AM modulated waves is the peak level of modulated waves.

• The following is used for the mixer:

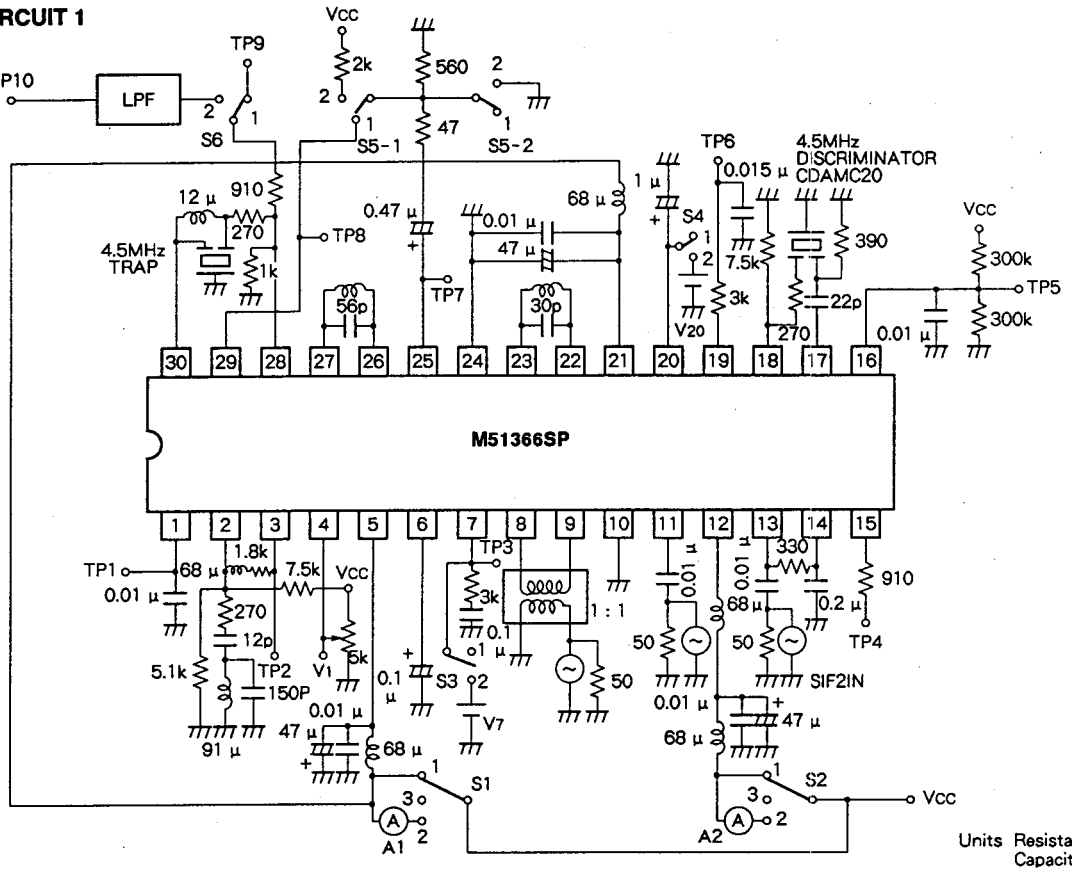


• With V_{CO} coil, IF AGC 0V and non-input condition, adjust free run frequency to 45.75MHz.

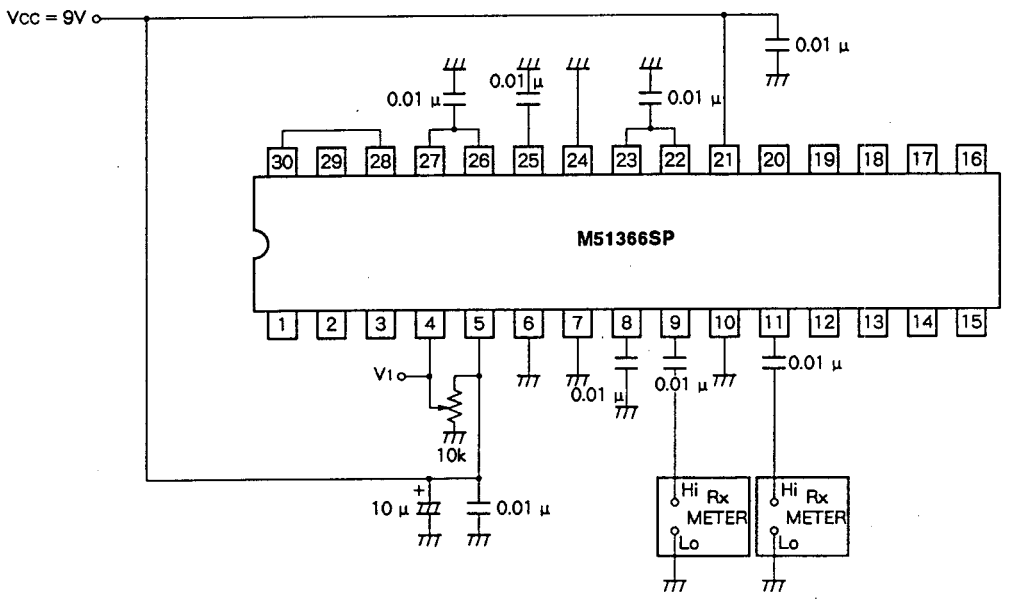
INPUT SIGNAL

SG No.	Input Signal (with 50 Ω Termination)
SG1	f_0=45.75MHz V_i=90dBμ 77.78%AM (87.5% Video modulation equivalent fm=20kHz)
SG2	f_0 = 45.75MHz V_i = 90dBμ
SG3	f_1 = 45.75MHz V_i = 90dBμ f_2 = 40 ± 5MHz V_i = 70dBμ } mixed signal
SG4	f_0 = 45.75MHz V_i = Vaviable f_m = 20kHz 77.78% AM
SG5	f_0 = 45.75MHz V_i = Vaviable f_m = 20kHz 16% AM
SG6	f_0 = 45.75MHz V_i = 80dBμ
SG7	f_0 = 45.75MHz V_i = 110dBμ
SG8	f_0 = 41.25MHz V_i = 100dBμ
SG9	f_0 = 41.25MHz V_i = 80dBμ
SG10	f_0 = 45.75MHz ± 5MHz V_i = 90dBμ
SG11	f_0=45.75MHz ± 5MHz V_i=90dBμ f_m=20kHz 77.78%AM
SG12	f_1 = 45.75MHz V_i = 90dBμ f_2 = 45.25MHz V_i = 60dBμ } mixed signal
SG13	f_1 = 45.75MHz V_i = 90dBμ f_2 = 42.75MHz V_i = 60dBμ } mixed signal
SG14	f_1 = 45.75MHz V_i = 90dBμ f_2 = 41.25MHz V_i = 60dBμ } mixed signal
SG15	f_1 = 45.75MHz V_i = 90dBμ f_2 = 42.17MHz V_i = 80dBμ f_3 = 41.25MHz V_i = 80dBμ } mixed signal
SG16	f_0 = 45.75MHz Standard 10-step wave modulation m = 87.5% Video modulation Sync chip level 90dBμ
SG17	f_0 = 4.5MHz ±25kHz dev V_i = 100dBμ f_m = 400Hz
SG18	f_0 = 4.5MHz ±25kHZ dev V_i = Vaviable f_m = 400Hz
SG19	f_0 = 4.5MHz V_i = 100dBμ 30% AM f_m = 400Hz
SG20	f_0 = 4.5MHz V_i = 100dBμ

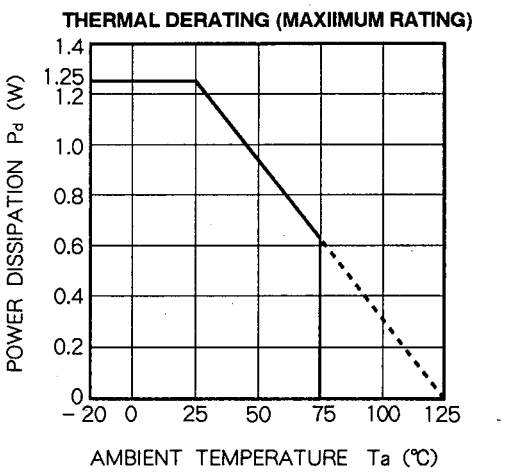
TEST CIRCUIT 1



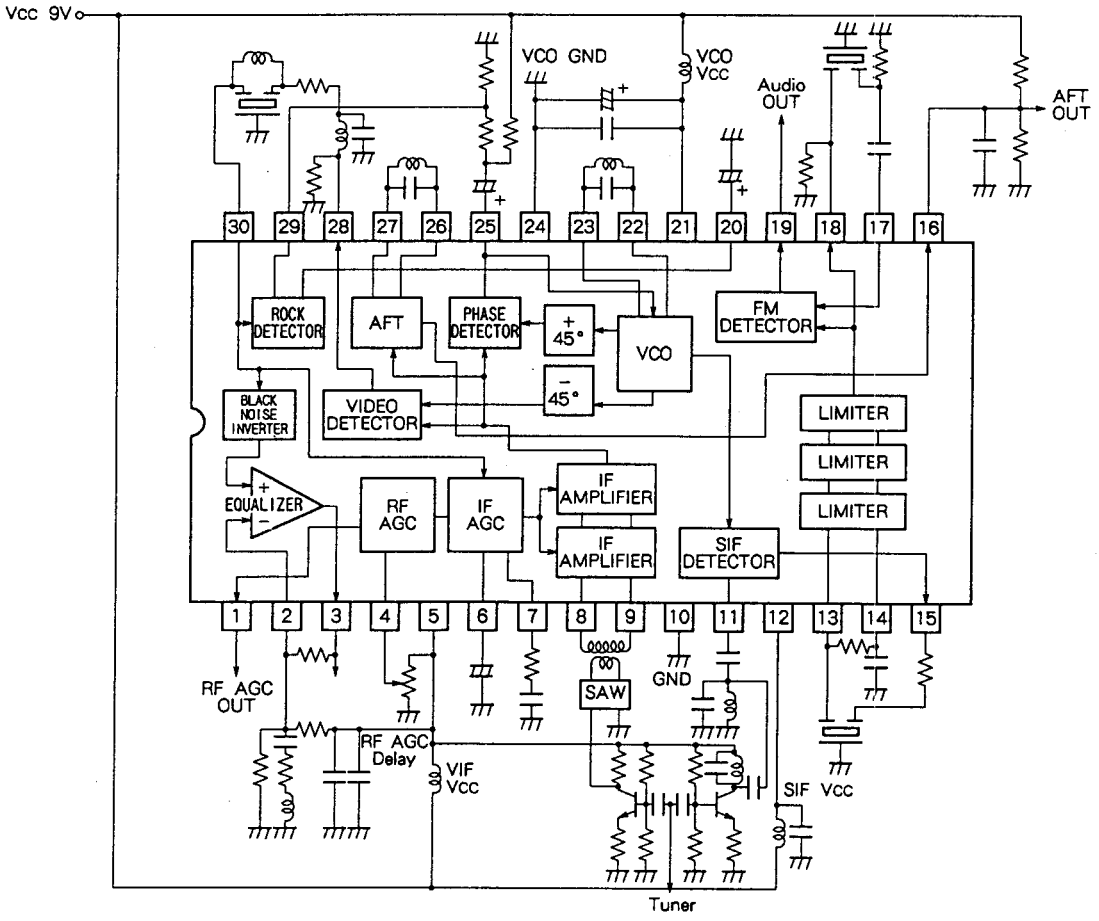
TEST CIRCUIT 2



TYPICAL CHARACTERISTICS

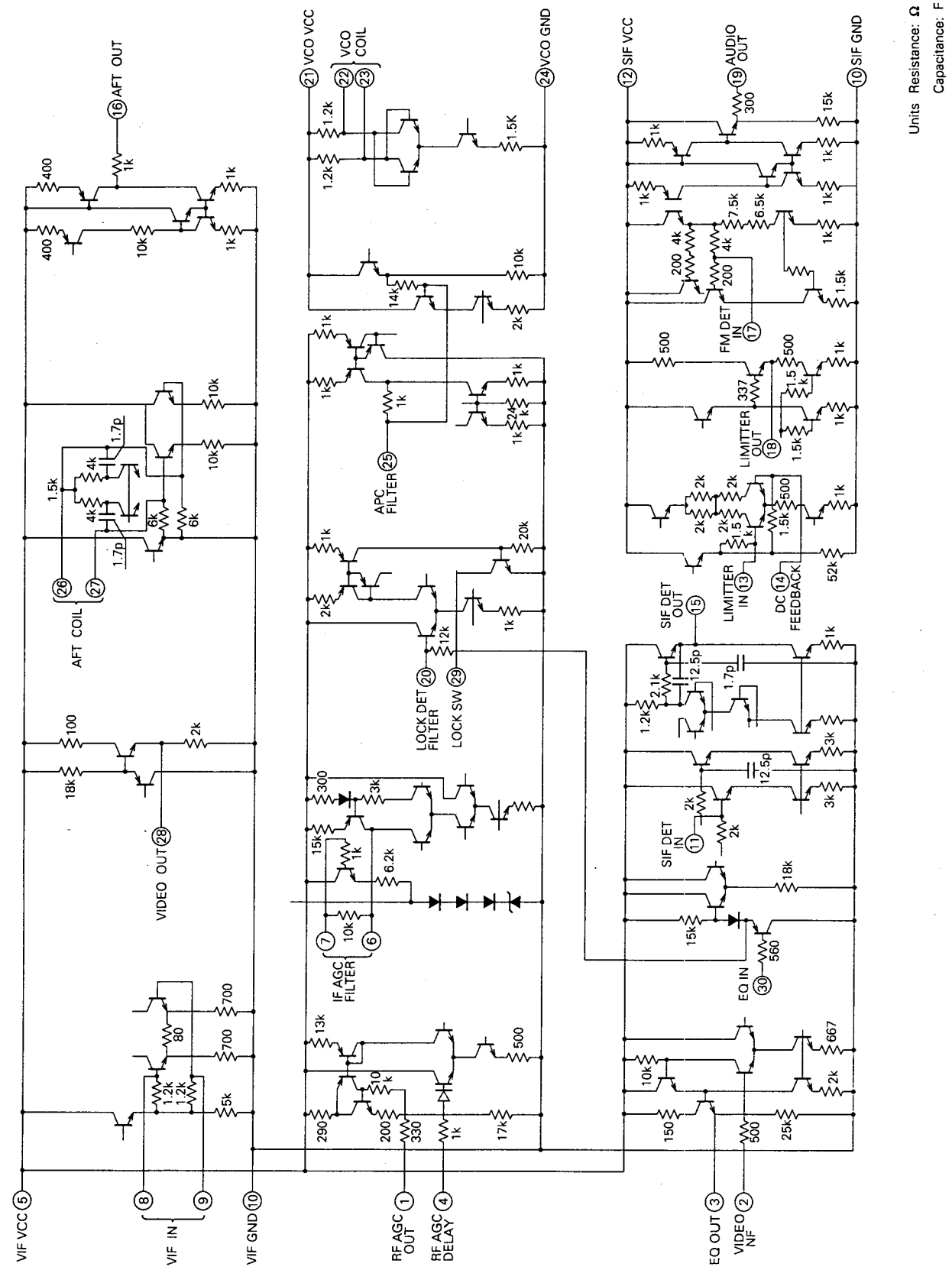


APPLICATION EXAMPLE



M51366SP

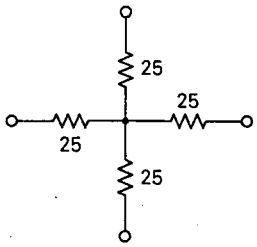
DESCRIPTION OF PIN



PRECAUTIONS FOR APPLICATION

Note:

- Amplitude level of all AM modulated waves shall be the peak level of modulated waves.
- The following is used for the mixer:



- With Vco coil, IF AGC 0V and non-input condition, adjust free run frequency to 45.75MHz.