National Semiconductor

LM124AQML
LM124QML

October 12, 2010

Low Power Quad Operational Amplifiers

General Description

The LM124/124A consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124/124A can be directly operated off of the standard +5Vdc power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional +15Vdc power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Available with Radiation Guarantee
  - — High Dose Rate 100 krad(Si)
  - — ELDRS Free 100 krad(Si)
- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  Single supply 3V to 32V
  or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 µA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^+ – 1.5V

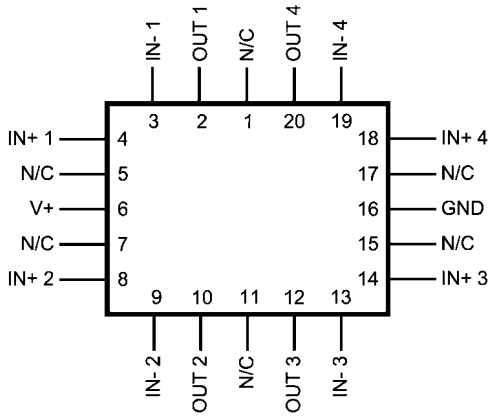
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM124J/883	7704301CA	J14A	14LD CERDIP
LM124AE/883	77043022A	E20A	20LD LEADLESS CHIP CARRIER
LM124AJ/883	7704302CA	J14A	14LD CERDIP
LM124AW/883		W14B	14LD CERPACK
LM124AWG/883	7704302XA	WG14A	14LD CERAMIC SOIC
LM124AJRQMLV (*Note 11*)	5962R9950401VCA, 100 krad(Si)	J14A	14LD CERDIP
LM124AJRLQMLV (*Note 12*)	5962R9950402VCA, 100 krad(Si)	J14A	14LD CERDIP
LM124AWGRQMLV (*Note 11*)	5962R9950401VZA, 100 krad(Si)	WG14A	14LD CERAMIC SOIC
LM124AWGRLQMLV (*Note 12*)	5962R9950402VZA, 100 krad(Si)	WG14A	14LD CERAMIC SOIC
LM124AWRQMLV (*Note 11*)	5962R9950401VDA, 100 krad(Si)	W14B	14LD CERPACK
LM124AWRLQMLV (*Note 12*)	5962R9950402VDA, 100 krad(Si)	W14B	14LD CERPACK
LM124 MDE (*Note 12*)	5962R9950402V9A, 100 krad(Si)	(*Note 1*)	Bare Die
LM124 MDR (*Note 11*)	5962R9950401V9A, 100 krad(Si)	(*Note 1*)	Bare Die

Note 1: FOR ADDITIONAL DIE INFORMATION, PLEASE VISIT THE HI REL WEB SITE AT: www.national.com/analog/space/level_die

Connection Diagrams

Leadless Chip Carrier



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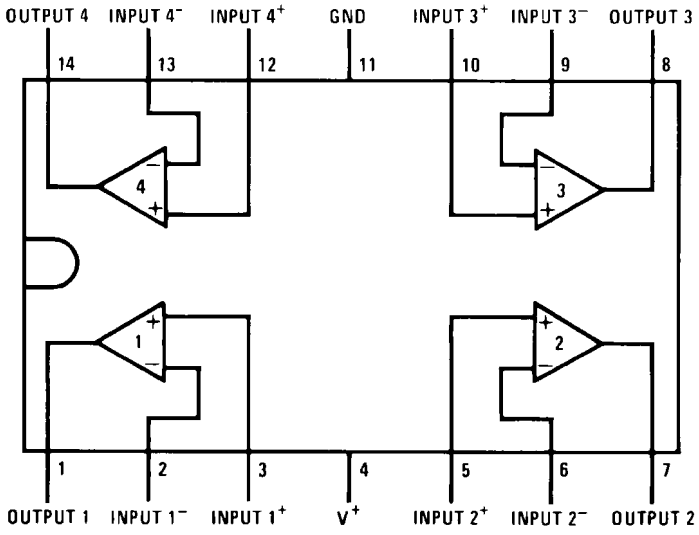
See NS Package Number E20A

Dual-In-Line Package



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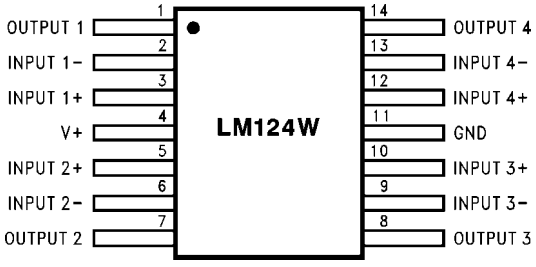
Top View
See NS Package Number J14A



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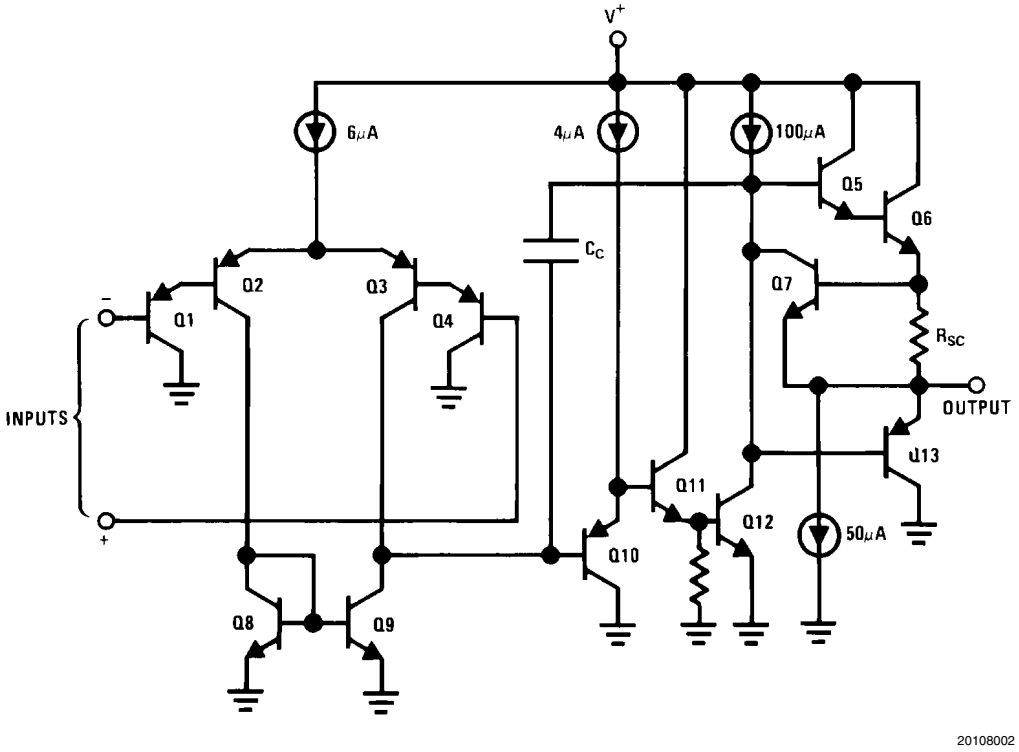
See NS Package Number W14B or WG14A

Schematic Diagram

(Each Amplifier)



Absolute Maximum Ratings (*Note 2*)

Supply Voltage, V^+	32Vdc or ±16Vdc
Differential Input Voltage	32Vdc
Input Voltage	−0.3Vdc to +32Vdc
Input Current	
(V_{IN} < −0.3Vdc) (*Note 5*)	50 mA
Power Dissipation (*Note 3*)	
CERDIP	1260mW
CERPACK	700mW
LCC	1350mW
CERAMIC SOIC	700mW
Output Short-Circuit to GND	
(One Amplifier) (*Note 4*)	
$V^+ \leq$ 15Vdc and T_A = 25°C	Continuous
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$
Maximum Junction Temperature	150°C
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$
Lead Temperature (Soldering, 10 seconds)	260°C
Thermal Resistance ThetaJA	
CERDIP (Still Air)	103°C/W
(500LF/Min Air flow)	51°C/W
CERPACK (Still Air)	176°C/W
(500LF/Min Air flow)	116°C/W
LCC (Still Air)	91°C/W
(500LF/Min Air flow)	66°C/W
CERAMIC SOIC (Still Air)	176°C/W
(500LF/Min Air flow)	116°C/W
ThetaJC	
CERDIP	19°C/W
CERPACK	18°C/W
LCC	24°C/W
CERAMIC SOIC	18°C/W
Package Weight (Typical)	
CERDIP	2200mg
CERPACK	460mg
LCC	470mg
CERAMIC SOIC	410mg
ESD Tolerance (*Note 6*)	250V

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LM124/883 Electrical Characteristics SMD: 77043

DC Parameters

(The following conditions apply to all the following parameters, unless otherwise specified.)

All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
I_{CC}	Power Supply Current	V+ = 5V			1.2	mA	1, 2, 3
		V+ = 30V			3.0	mA	1
					4.0	mA	2, 3
I_{SINK}	Output Sink Current	V+ = 15V, V_{OUT} = 200mV, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		12		uA	1
		V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		10		mA	1
				5		mA	2, 3
I_{SOURCE}	Output Source Current	V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = -65mV			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	V+ = 5V, V_{OUT} = 0V		-60		mA	1
V_{IO}	Input Offset Voltage	V+ = 30V, V_{CM} = 0V		-5	5	mV	1
				-7	7	mV	2, 3
		V+ = 30V, V_{CM} = 28V		-5	5	mV	1
				-7	7	mV	2, 3
		V+ = 5V, V_{CM} = 0V		-5	5	mV	1
				-7	7	mV	2, 3
		V+ = 30V, V_{CM} = 28.5V		-5	5	mV	1
CMRR	Common Mode Rejection Ratio	V+ = 30V, V_{IN} = 0V to 28.5V	(*Note 14*)	70		dB	1
$+I_{IB}$	Input Bias Current	V+ = 5V, V_{CM} = 0V	(*Note 13*)	-150	10	nA	1
				-300	10	nA	2, 3
I_{IO}	Input Offset Current	V+ = 5V, V_{CM} = 0V		-30	30	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V, V_{CM} = 0V		65		dB	1
V_{CM}	Common Mode Voltage Range	V+ = 30V	(*Note 7*)		28.5	V	1
			(*Note 14*)		28	V	2, 3
A_{VS}	Large Signal Gain	V+ = 15V, R_L = 2K Ω, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6
V_{OH}	Output Voltage High	V+ = 30V, R_L = 2K Ω		26		V	4, 5, 6
		V+ = 30V, R_L = 10K Ω		27		V	4, 5, 6
V_{OL}	Output Voltage Low	V+ = 30V, R_L = 10K Ω			40	mV	4, 5, 6
		V+ = 30V, I_{SINK} = 1uA			40	mV	4
					100	mV	5, 6
		V+ = 5V, R_L= 10K Ω			20	mV	4, 5, 6
	Channel Separation (Amp to Amp Coupling)	1KHz, 20KHz	(*Note 9*) (*Note 15*)	80		dB	4

LM124A/883 Electrical Characteristics SMD: 77043

DC Parameters

(The following conditions apply to all the following parameters, unless otherwise specified.)

All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
I_{CC}	Power Supply Current	V+ = 5V			1.2	mA	1, 2, 3
		V+ = 30V			3.0	mA	1
					4.0	mA	2, 3
I_{SINK}	Output Sink Current	V+ = 15V, V_{OUT} = 200mV, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		12		uA	1
		V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		10		mA	1
				5		mA	2, 3
I_{SOURCE}	Output Source Current	V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = -65mV			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	V+ = 5V, V_{OUT} = 0V		-60		mA	1
V_{IO}	Input Offset Voltage	V+ = 30V, V_{CM} = 0V		-2	2	mV	1
				-4	4	mV	2, 3
		V+ = 30V, V_{CM} = 28.5V		-2	2	mV	1
		V+ = 30V, V_{CM} = 28V		-4	4	mV	2, 3
		V+ = 5V, V_{CM} = 0V		-2	2	mV	1
				-4	4	mV	2, 3
CMRR	Common Mode Rejection Ratio	V+ = 30V, V_{IN} = 0V to 28.5V	(*Note 14*)	70		dB	1
$\pm I_{IB}$	Input Bias Current	V+ = 5V, V_{CM} = 0V	(*Note 13*)	-50	10	nA	1
				-100	10	nA	2, 3
I_{IO}	Input Offset Current	V+ = 5V, V_{CM} = 0V		-10	10	nA	1
				-30	30	nA	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V, V_{CM} = 0V		65		dB	1
V_{CM}	Common Mode Voltage Range	V+ = 30V	(*Note 7*) (*Note 14*)		28.5	V	1
					28	V	2, 3
A_{VS}	Large Signal Gain	V+ = 15V, R_L = 2K Ω, V_O = 1V to 11V	(*Note 8*)	50		V/mV	4
				25		V/mV	5, 6
V_{OH}	Output Voltage High	V+ = 30V, R_L = 2K Ω		26		V	4, 5, 6
		V+ = 30V, R_L = 10K Ω		27		V	4, 5, 6
V_{OL}	Output Voltage Low	V+ = 30V, R_L = 10K Ω			40	mV	4, 5, 6
		V+ = 30V, I_{SINK} = 1uA			40	mV	4
					100	mV	5, 6
		V+ = 5V, R_L = 10K Ω			20	mV	4, 5, 6
	Channel Separation Amp to Amp Coupling	1KHz, 20KHz	(*Note 9*) (*Note 15*)	80		dB	4

LM124A RAD HARD Electrical Characteristics

SMD: 5962R99504 (*Note 11*, *Note 12*)

DC Parameters

(The following conditions apply to all the following parameters, unless otherwise specified.)

All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	UniT	Sub-Groups
V_{IO}	Input Offset Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-2	2	mV	1
				-4	4	mV	2, 3
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-2	2	mV	1
				-4	4	mV	2, 3
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-2	2	mV	1
				-4	4	mV	2, 3
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-2	2	mV	1
				-4	4	mV	2, 3
I_{IO}	Input Offset Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-10	10	nA	1, 2
				-30	30	nA	3
$\pm I_{IB}$	Input Bias Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(*Note 13*)	-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
+PSRR	Power Supply Rejection Ratio	V_{CC}- = Gnd, V_{CM} = +1.4V, 5V ≤ V_{CC} ≤ 30V		-100	100	uV/V	1, 2, 3
CMRR	Common Mode Rejection Ratio		(*Note 14*)	76		dB	1, 2, 3
I_{OS}+	Output Short Circiut Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_O = 25V		-70		mA	1, 2,3
I_{CC}	Power Supply Current	V_{CC}+ = 30V, V_{CC}- = Gnd			3	mA	1, 2
					4	mA	3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V	(*Note 10*)	-30	30	uV/ °C	2
		-55°C ≤ T_A ≤ +25°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V		-30	30	uV/ °C	3
$\Delta_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V	(*Note 10*)	-400	400	pA/° C	2
		-55°C ≤ T_A ≤ +25°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V		-700	700	pA/ °C	3

LM124A RAD HARD SMD: 5962R99504 (*Note 11*, *Note 12*)

AC/DC Parameters

(The following conditions apply to all the following parameters, unless otherwise specified.)

All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	UniT	Sub-Groups
V_{OL}	Logical "0" Output Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, R_L = 10K Ω			35	mV	4, 5, 6
		V_{CC}+ = 30V, V_{CC}- = Gnd, I_{OI} = 5mA			1.5	V	4, 5, 6
		V_{CC}+ = 4.5V, V_{CC}- = Gnd, I_{OI} = 2uA			0.4	V	4, 5, 6
V_{OH}	Logical "1" Output Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, I_{OH} = -10mA		27		V	4, 5, 6
		V_{CC}+ = 4.5V, V_{CC}- = Gnd, I_{OH} = -10mA		2.4		V	4, 5, 6
A_{VS}+	Voltage Gain	V_{CC}+ = 30V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 26V, R_L = 10K Ω		50		V/mV	4
				25		V/mV	5, 6
		V_{CC}+ = 30V, V_{CC}- = Gnd, 5V ≤ V_O ≤ 20V, R_L = 2K Ω		50		V/mV	4
				25		V/mV	5, 6
A_{VS}	Voltage Gain	V_{CC}+ = 5V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 10K Ω		10		V/mV	4, 5, 6
		V_{CC}+ = 5V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 2K Ω		10		V/mV	4, 5, 6
$+V_{OP}$	Maximum Output Voltage Swing	V_{CC}+ = 30V, V_{CC}- = Gnd, V_O = +30V, R_L = 10K Ω		27		V	4, 5, 6
		V_{CC}+ = 30V, V_{CC}- = Gnd, V_O = +30V, R_L = 2K Ω		26		V	4, 5, 6
$TR_{(TR)}$	Transient Response: Rise Time	V_{CC}+ = 30V, V_{CC}- = Gnd			1	uS	7, 8A, 8B
$TR_{(OS)}$	Transient Response: Overshoot	V_{CC}+ = 30V, V_{CC}- = Gnd			50	%	7, 8A, 8B
$\pm S_R$	Slew Rate: Rise	V_{CC}+ = 30V, V_{CC}- = Gnd		0.1		V/uS	7, 8A, 8B
	Slew Rate: Fall	V_{CC}+ = 30V, V_{CC}- = Gnd		0.1		V/uS	7, 8A, 8B

LM124A RAD HARD SMD: 5962R99504 (*Note 11*, *Note 12*)

AC Parameters

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $+V_{CC}$ = 30V, $-V_{CC}$ = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
NI_{BB}	Noise Broadband	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, BW = 10Hz to 5KHz			15	uVrm s	7
NI_{PC}	Noise Popcorn	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, R_S = 20K Ω, BW = 10Hz to 5KHz			50	uVpK	7
C_S	Channel Separation	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, R_L = 2K Ω	(*Note 15*)	80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, A to B		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, A to C		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, A to D		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, B to A		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, B to C		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, B to D		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, C to A		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, C to B		80		dB	7
		R_L = 2K Ω, Vin = 1V and 16V, C to D		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, D to A		80		dB	7
		R_L = 2K Ohms, V_{IN} = 1V and 16V, D to B		80		dB	7
		R_L = 2K Ω, Vin = 1V and 16V, D to C		80		dB	7

LM124A RAD HARD - DC Drift Values SMD: 5962R99504 (*Note 11*, *Note 12*)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: "Delta calculations performed on QMLV devices at group B, subgroup 5 only"

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
V_{IO}	Input Offset Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-10	10	nA	1

LM124A - POST RADIATION LIMITS +25°C SMD: 5962R99504 (*Note 11*, *Note 12*)

(The following conditions apply to all the following parameters, unless otherwise specified.)

All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
V_{IO}	Input Offset Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(*Note 11*)	-2.5	2.5	mV	1
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-2.5	2.5	mV	1
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-2.5	2.5	mV	1
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-2.5	2.5	mV	1
I_{IO}	Input Offset Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(*Note 11*)	-15	15	nA	1
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-15	15	nA	1
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-15	15	nA	1
		V_{CC}+ = 2.5V, V_{CC}- = -2.5V, V_{CM} = -1.1V		-15	15	nA	1
$\pm I_{IB}$	Input Bias Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(*Note 11*)	-75	+0.1	nA	1
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-75	+0.1	nA	1
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-75	+0.1	nA	1
		V_{CC}+ = 2.5V, V_{CC}- = -2.5V, V_{CM} = -1.1V		-75	+0.1	nA	1
A_{VS}+	Voltage Gain	V_{CC}+ = 30V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 26V, R_L = 10K Ω	(*Note 11*)	40		V/mV	4
		V_{CC}+ = 30V, V_{CC}- = Gnd, 5V ≤ V_O ≤ 20V, R_L = 2K Ω		40		V/mV	4

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), $ThetaJ_A$ (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/ThetaJ_A$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 4: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 5: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$ (at 25°C).

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

Note 7: Guaranteed by V_{IO} tests.

Note 8: Datalog reading in K=V/mV

Note 9: Guaranteed, not tested

Note 10: Calculated parameters

Note 11: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019

Note 12: Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

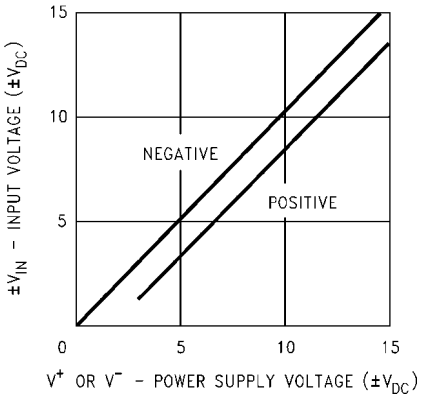
Note 13: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 14: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage independent of the magnitude of V+.

Note 15: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

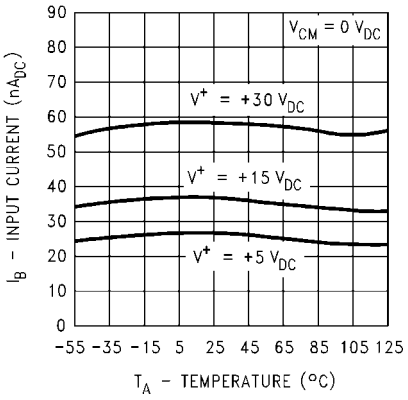
Typical Performance Characteristics

Input Voltage Range



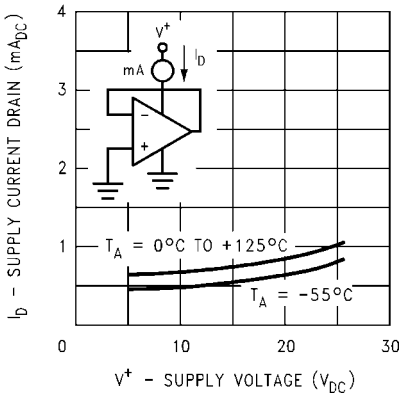
20108034

Input Current



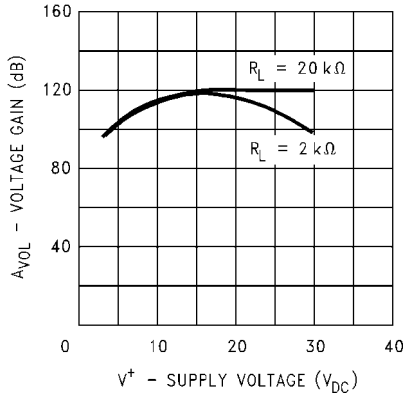
20108035

Supply Current



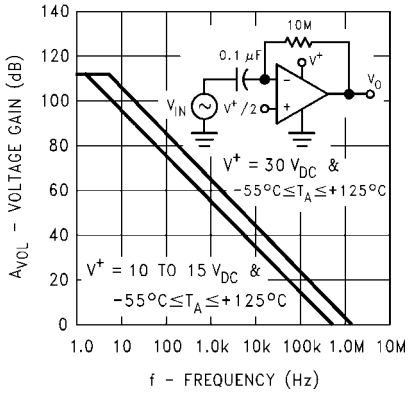
20108036

Voltage Gain



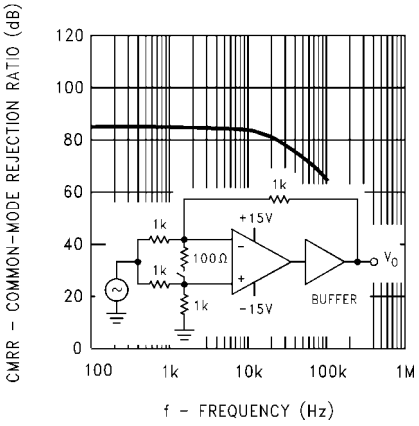
20108037

Open Loop Frequency Response



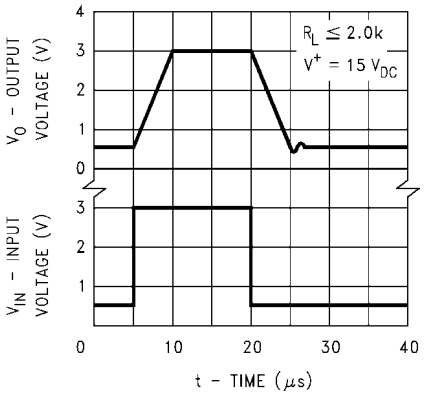
20108038

Common Mode Rejection Ratio



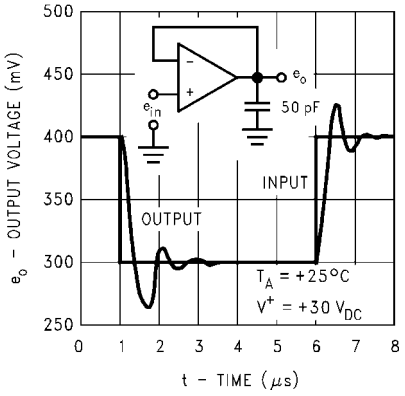
20108039

Voltage Follower Pulse Response



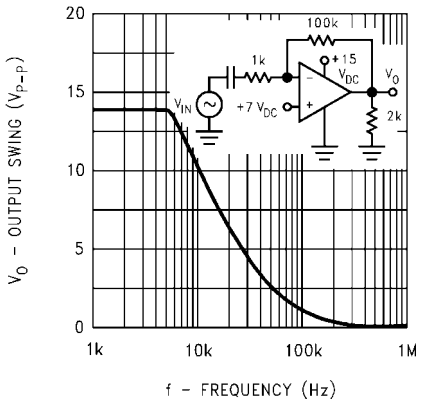
20108040

Voltage Follower Pulse Response (Small Signal)



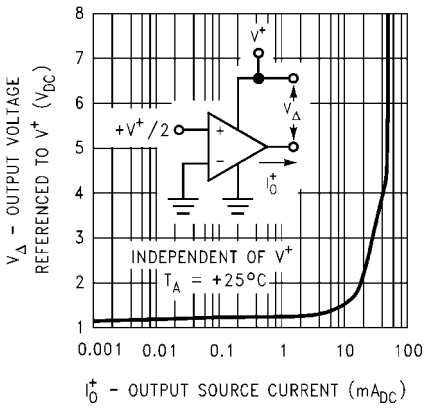
20108041

Large Signal Frequency Response



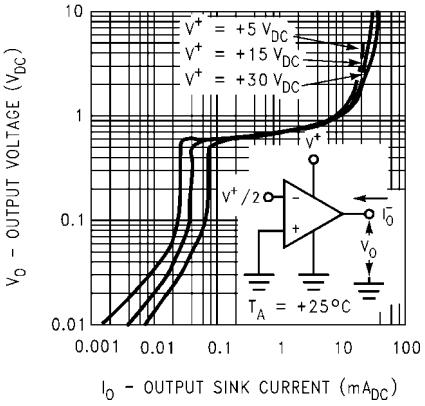
20108042

Output Characteristics Current Sourcing



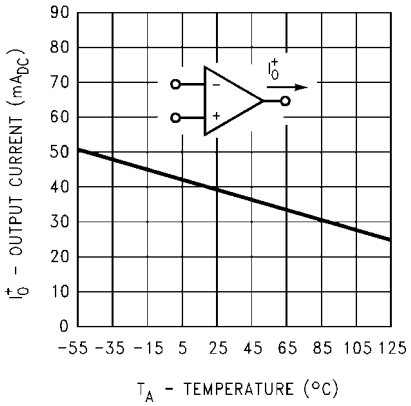
20108043

Output Characteristics Current Sinking



20108044

Current Limiting



20108045

Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

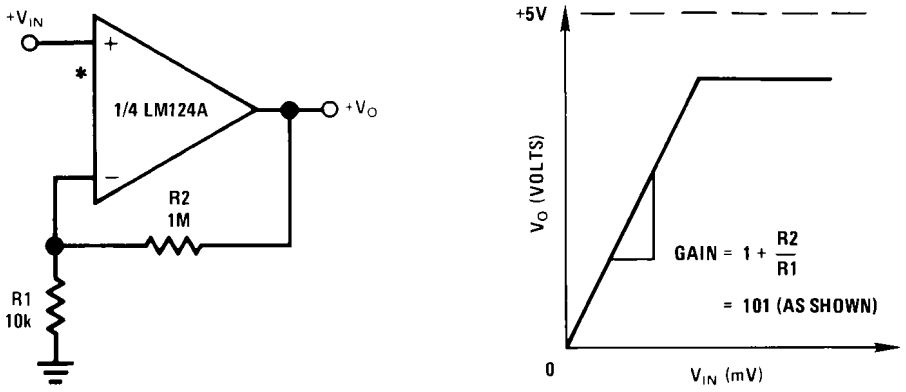
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})

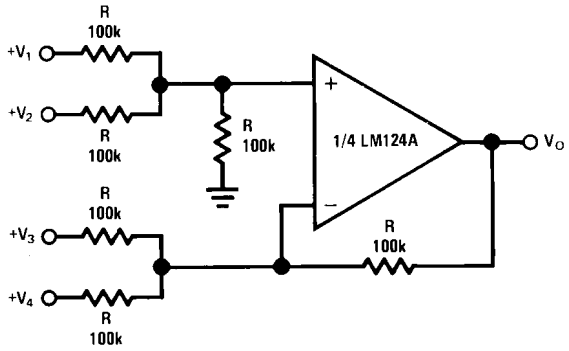
Non-Inverting DC Gain (0V Input = 0V Output)



20108005

*R not needed due to temperature independent I_{IN}

DC Summing Amplifier
($V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)

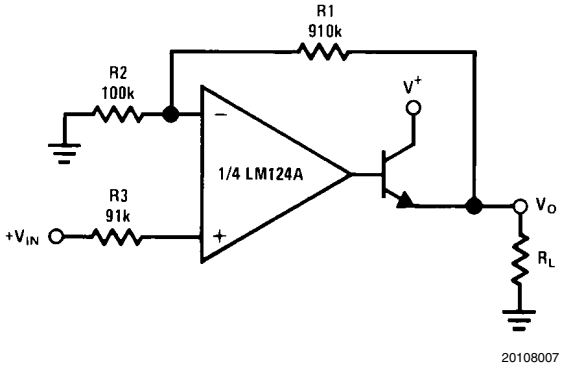


20108006

Where: $V_0 = V_1 + V_2 - V_3 - V_4$

$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier

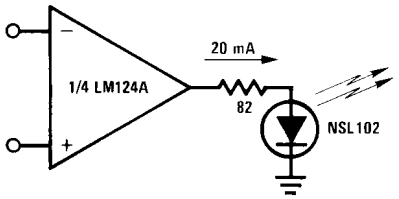


20108007

$V_0 = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$

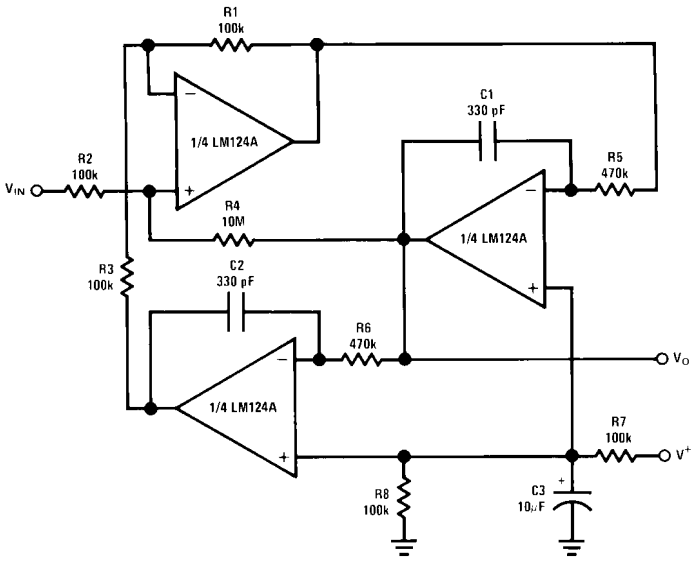
$A_V = 10$

LED Driver



20108008

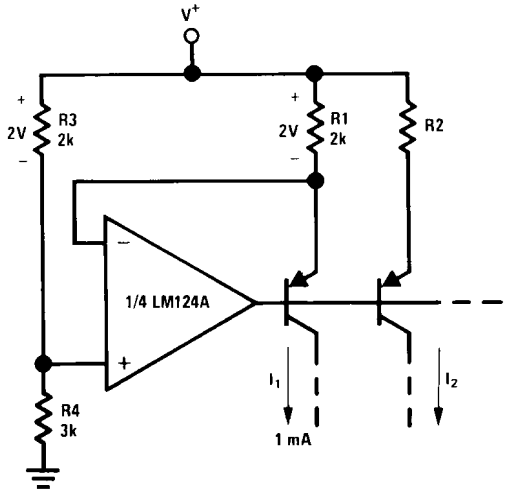
"BI-QUAD" RC Active Bandpass Filter



20108009

f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

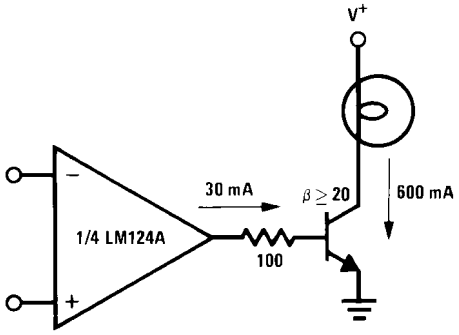
Fixed Current Sources



20108010

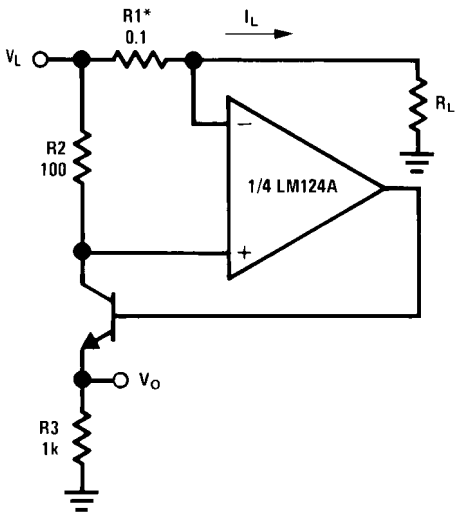
$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Lamp Driver



20108011

Current Monitor



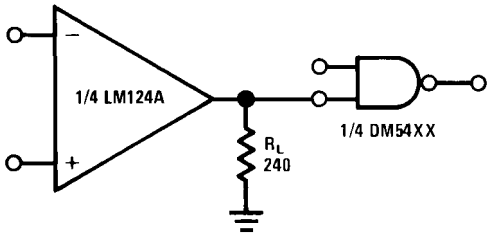
20108012

$$V_O = \frac{1V(I_L)}{1A}$$

$$V_L \leq V^+ - 2V$$

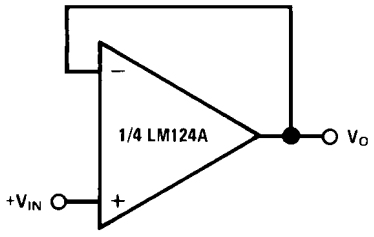
*(Increase R1 for I_L small)

Driving TTL



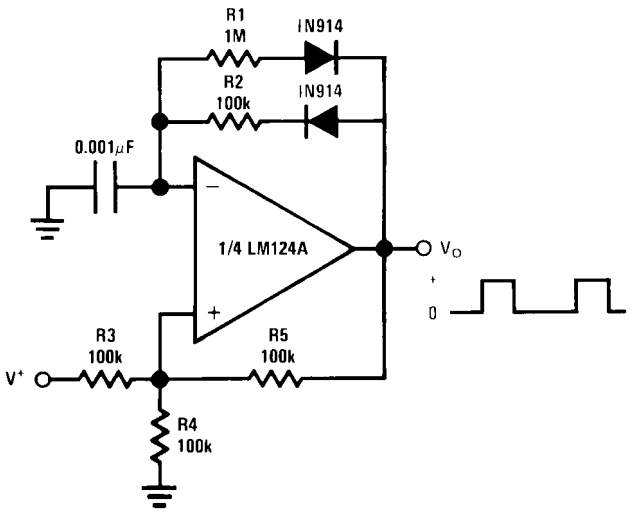
20108013

Voltage Follower



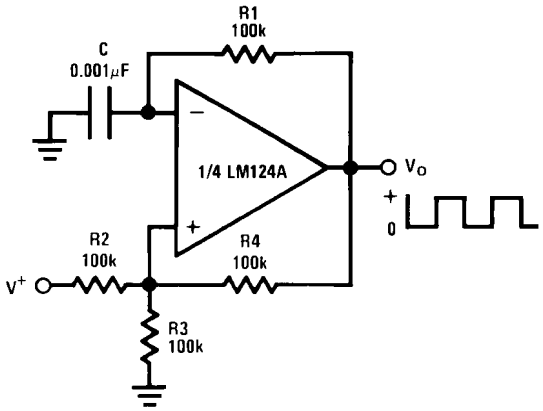
20108014

Pulse Generator



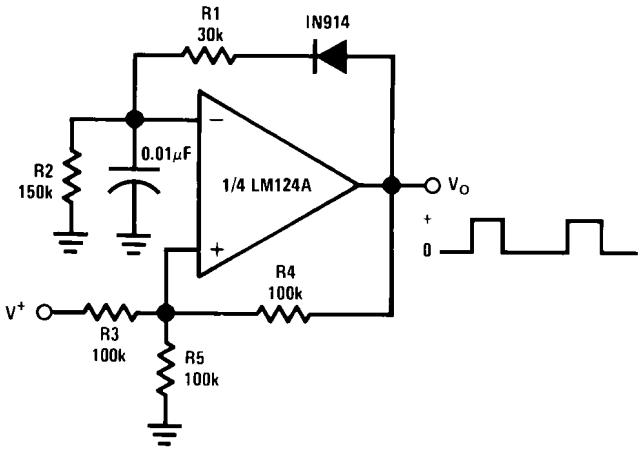
20108015

Squarewave Oscillator



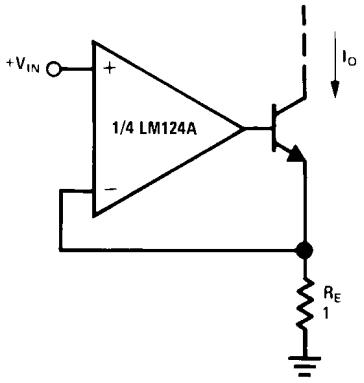
20108016

Pulse Generator



20108017

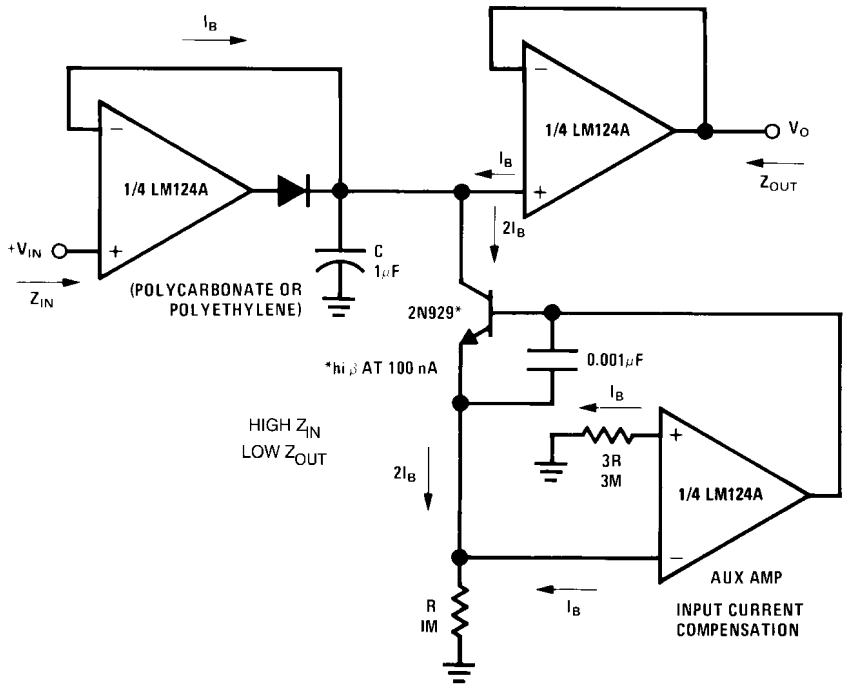
High Compliance Current Sink



20108018

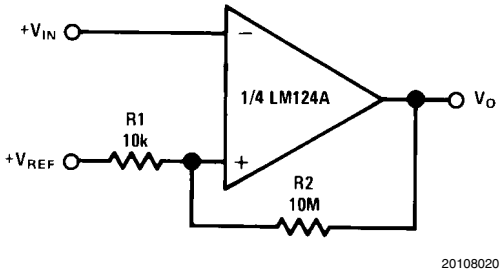
I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

Low Drift Peak Detector

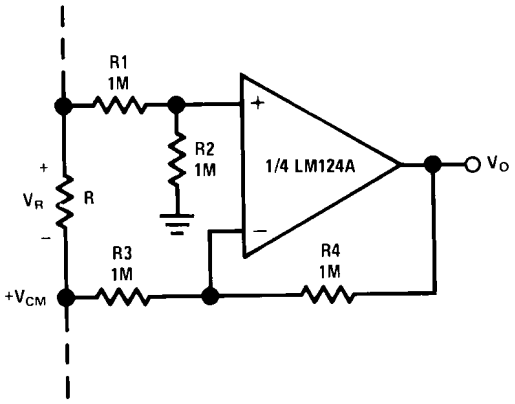


20108019

Comparator with Hysteresis

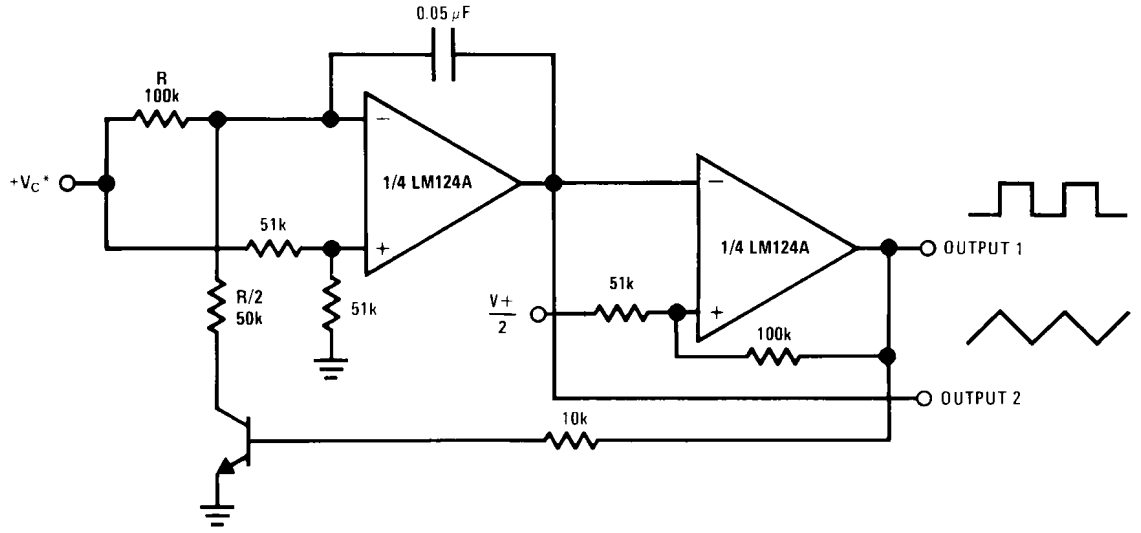


Ground Referencing a Differential Input Signal



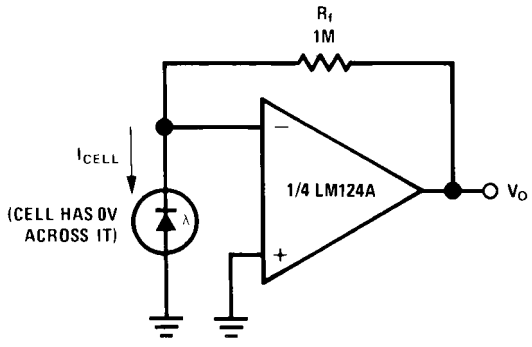
$V_O = V_R$

Voltage Controlled Oscillator Circuit

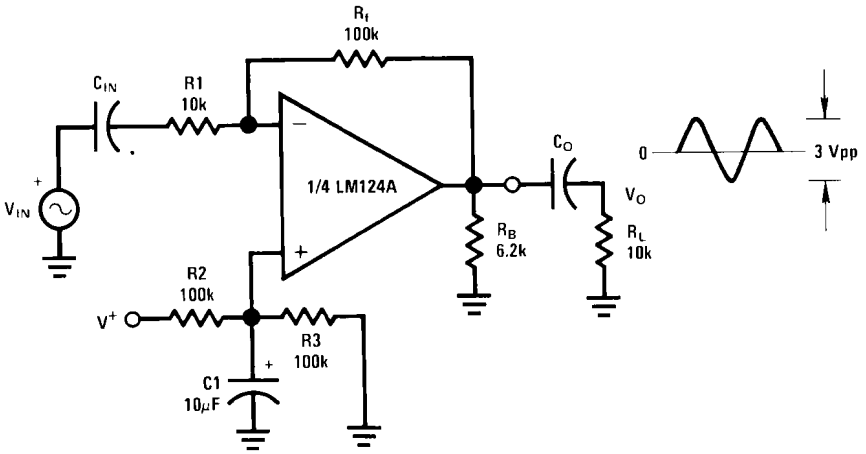


*Wide control voltage range: 0 $V_{DC} \leq V_C \leq 2\ (V^+ - 1.5\ V_{DC})$

Photo Voltaic-Cell Amplifier



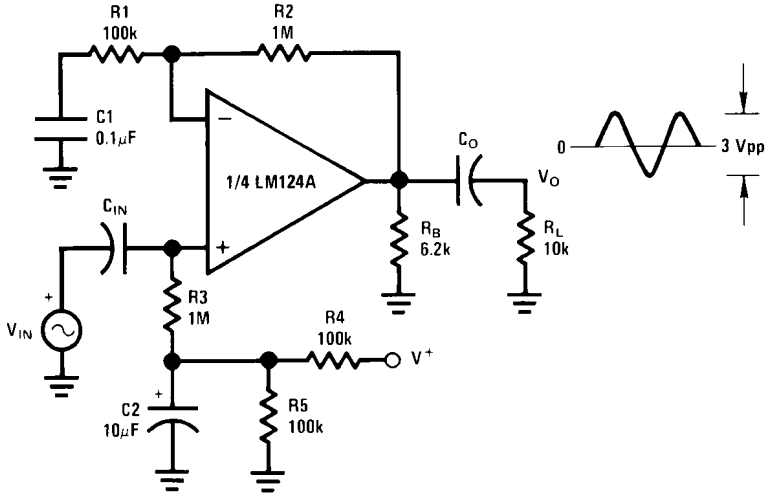
AC Coupled Inverting Amplifier



20108024

$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10)$$

AC Coupled Non-Inverting Amplifier

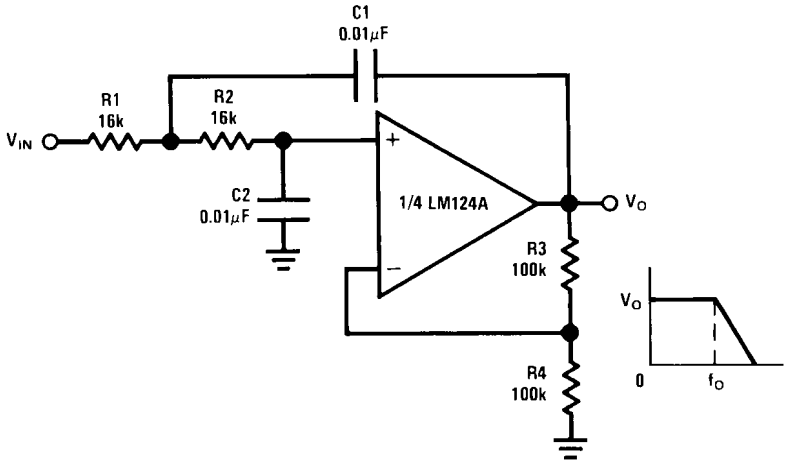


20108025

$$A_V = 1 + \frac{R2}{R1}$$

$$A_V = 11 \text{ (As shown)}$$

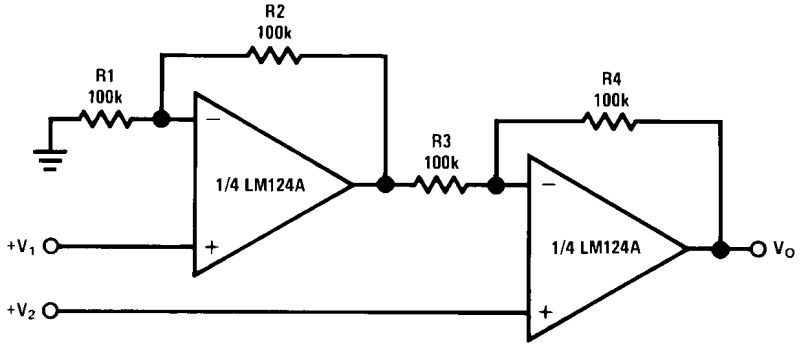
DC Coupled Low-Pass RC Active Filter



20108026

f_O = 1 kHz
Q = 1
A_V = 2

High Input Z, DC Differential Amplifier



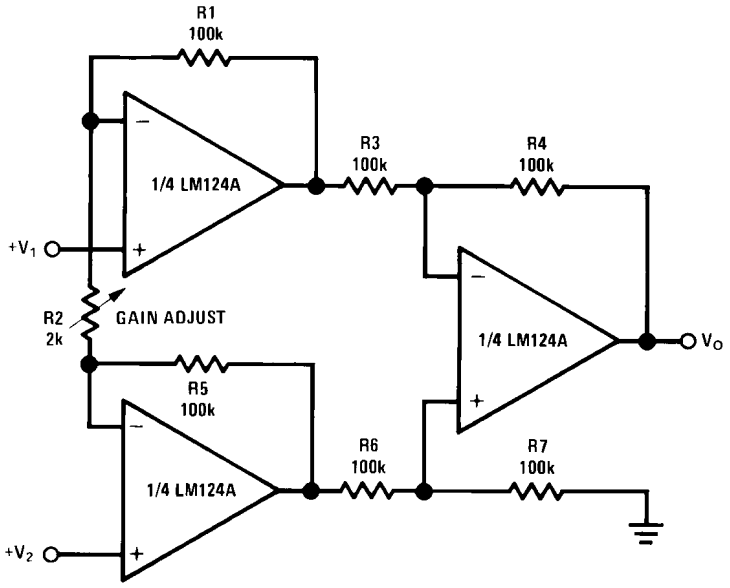
20108027

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



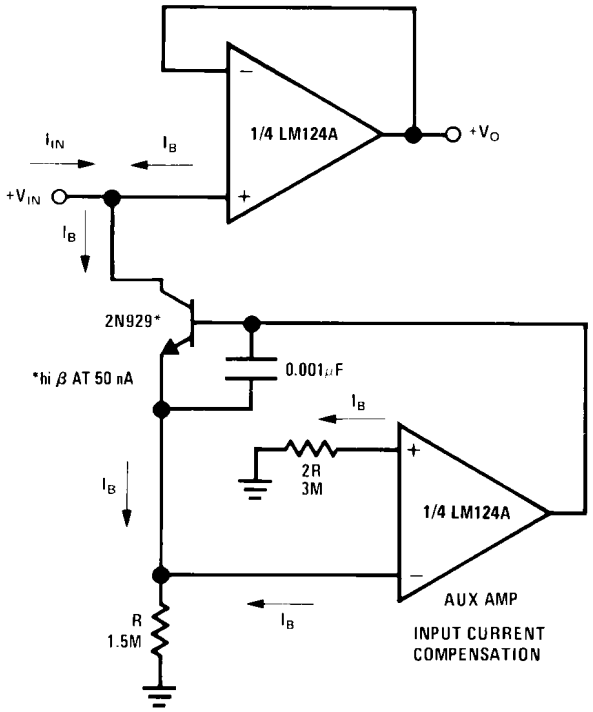
20108028

If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

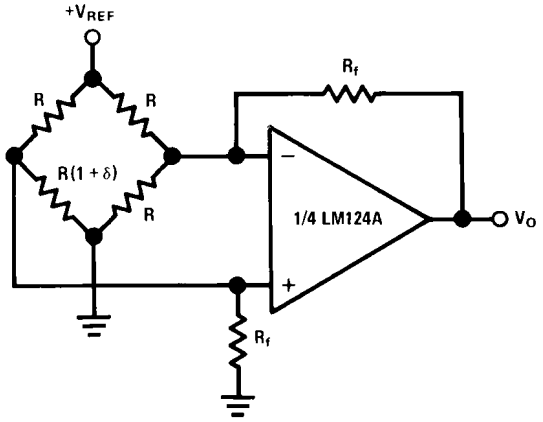
As shown $V_O = 101\,(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



20108029

Bridge Current Amplifier

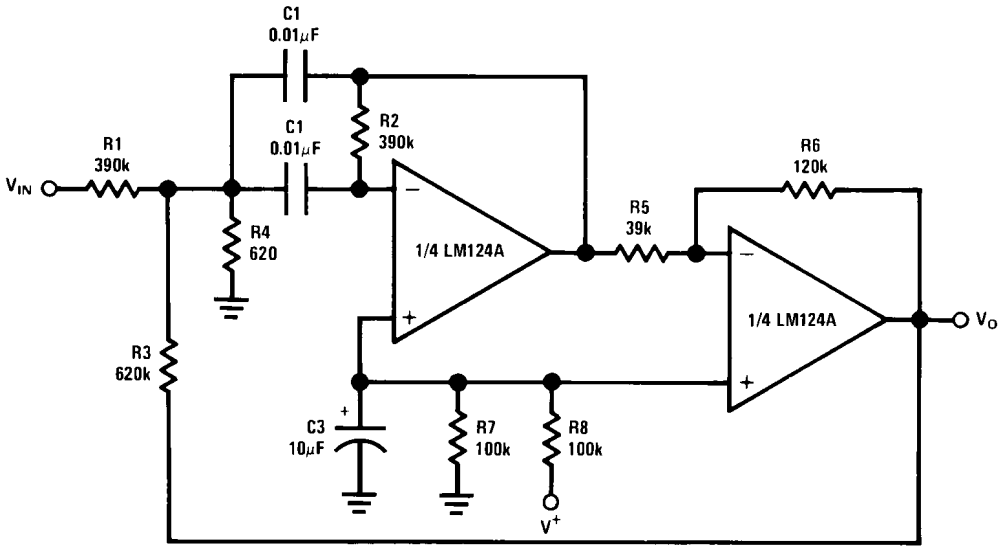


20108030

For $\delta << 1$ and $R_f >> R$

$$V_O \simeq V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Bandpass Active Filter



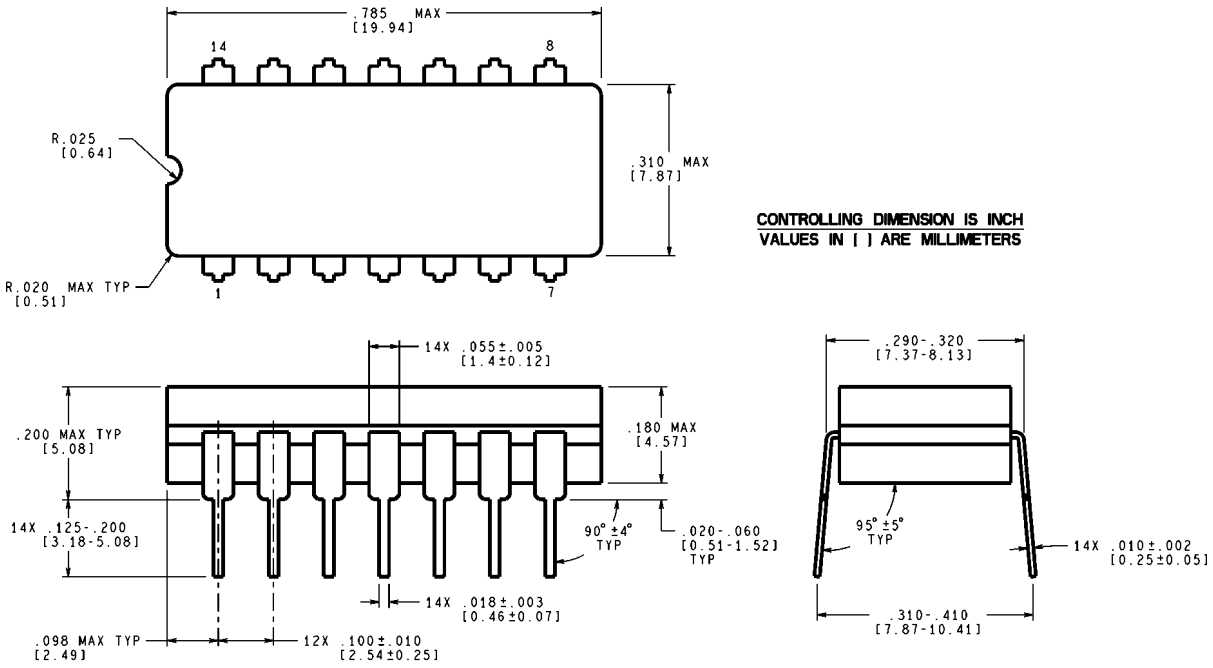
20108031

f_O = 1 kHz
Q = 25

Revision History

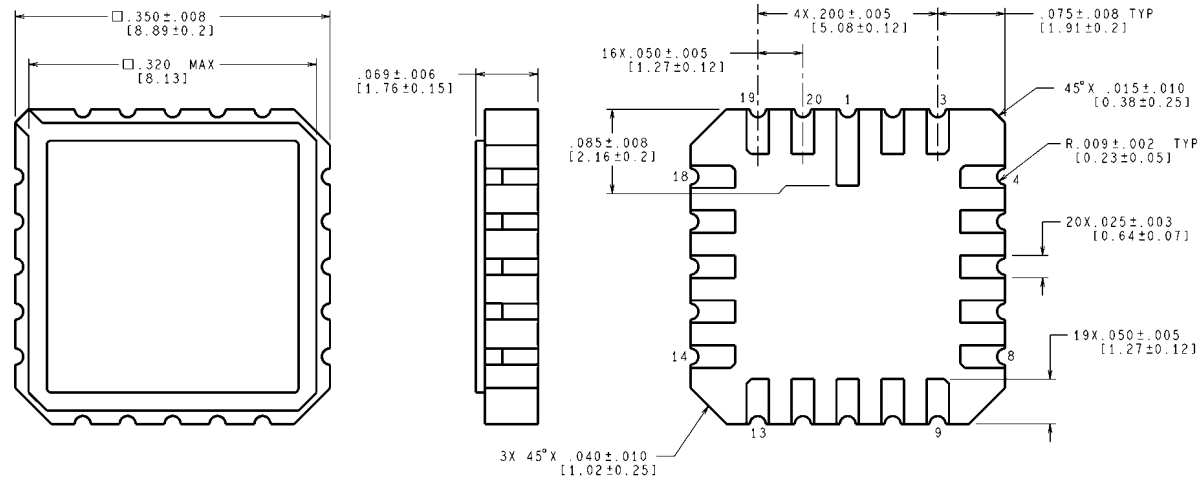
Date Released	Revision	Section	Changes
9/2/04	A	New Release, Corporate format	3 MDS data sheets converted into one Corp. data sheet format. MNLM124-X, Rev. 1A2, MNLM124A-X, Rev. 1A3 and MRLM124A-X-RH, Rev. 5A0. MDS data sheets will be archived.
01/27/05	B	Connection Diagrams, Quality Conformance Inspection Section, and Physical Dimensions drawings	Added E package Connection Diagram. Changed verbiage under Quality Conformance Title, and Updated Revisions for the Marketing Drawings.
04/18/05	C	Update Absolute Maximum Ratings Section	Corrected typo for Supply Voltage limit From: 32Vdc or +16Vdc TO: 32Vdc or ±16Vdc. Added cerpack, cerdip, LCC package weight.
06/16/06	D	Features, Ordering Information Table, Rad Hard Electrical Section and Notes	Added Available with Radiation Guarantee, Low Dose NSID's to table 5962R9950402VCA LM124AJRLQMLV, 5962R9950402VDA LM124AWRLQMLV, 5962R9950402VZA LM124AWGRLQMLV, and reference to Note 10 and 11. Deleted code K NSID's LM124AJLQMLV 5962L9950401VCA, LM124AWGLQMLV 5962L9950401VZA, LM124AWLQMLV 5962L9950401VDA, Note 11 to Rad Hard Electrical Heading. Note 11 to Notes.
10/07/2010	E	Data sheet title, Features, Ordering table, Electrical characteristic headings, Rad Hard conditions	Update with current device information and format. Revision D will be Archived

Physical Dimensions inches (millimeters) unless otherwise noted



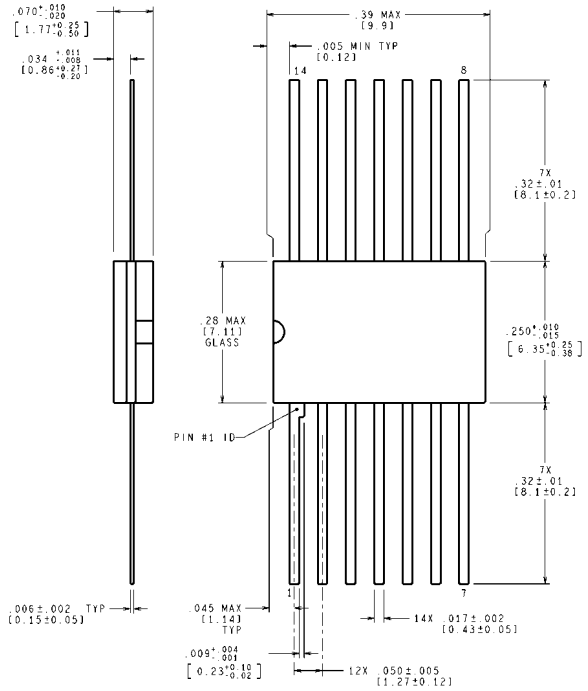
J14A (Rev J)

SAMPLE TEXT Ceramic Dual-In-Line Package (J)
NS Package Number J14A



E20A (Rev F)

SAMPLE TEXT 20 Pin Leadless Chip Carrier, Type C (E)
NS Package Number E20A



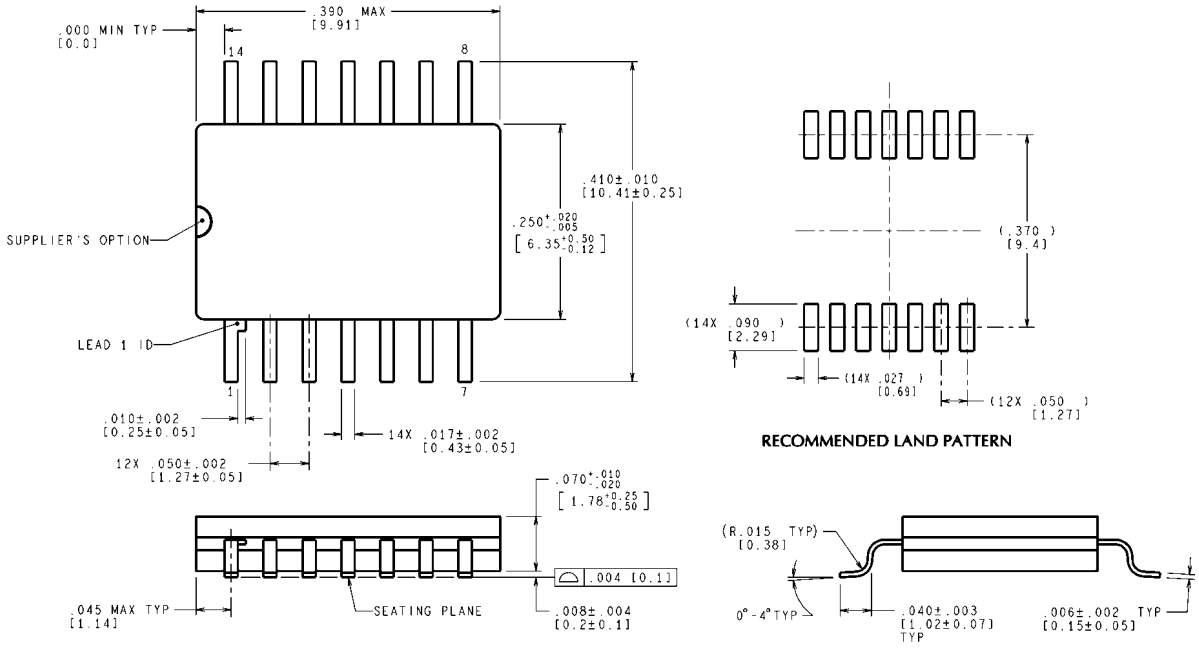
MIL-PRF-38535 CONFIGURATION CONTROL

MIL-STD-1835B CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

W14B (Rev P)

SAMPLE TEXT Ceramic Flatpak Package
NS Package Number W14B



MIL-PRF-38535 CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

WG14A (Rev D)

SAMPLE TEXT 14-Pin Ceramic Package (WG)
NS Package Number WG14A

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
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