HARRIS Semiconductor

IH6208

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
DG409, DG509A, HI-0509(A)

April 1999

8-Channel CMOS Analog Multiplexer

Features

- **Ultra Low Leakage - $I_{D(OFF)} \leq$ 100pA (Typ)**
- **$r_{DS(ON)}$ < 400Ω Over Full Signal and Temperature Range**
- **Power Supply Quiescent Current Less Than 100μA**
- **±14V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Binary Address Control (2 Address Inputs Control 2 Out of 8 Channels)**
- **TTL and CMOS Compatible Address Control**
- **Pin Compatible with DG509A, HI-509 and ADG509A**
- **Internal Diode in Series with V+ for Fault Protection**

Description

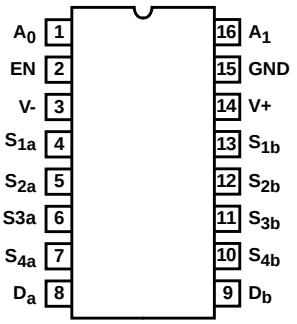
The IH6208 is a CMOS 2 of 8 multiplexer. The part is a plug-in replacement for the DG509A. Two-line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided for use as a system enable. When the ENABLE input is high (5V), the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs arecontrolled by TTL logic or CMOS logic elements with a “0” corresponding to any voltage less than 0.8V and a “1” corresponding to any voltage greater than 2.4V. Note that the ENABLE input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

Part Number Information

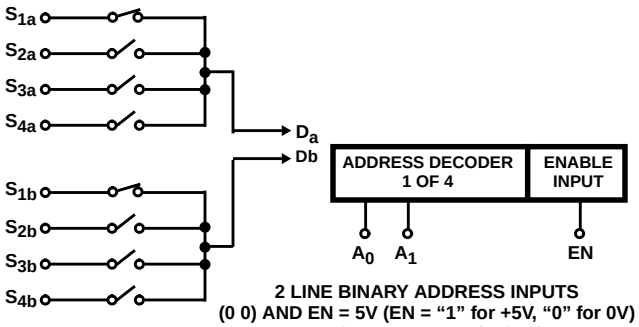
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
IH6208MJE	-55 to 125	16 Ld CERDIP	F16.3
IH6208MJE/883B	-55 to 125	16 Ld CERDIP	F16.3
IH6208MFE/883B	-55 to 125	16 Ld Flat Pack	K16.A
IH6208CJE	0 to 70	16 Ld CERDIP	F16.3
IH6208CPE	0 to 70	16 Ld PDIP	E16.3

Pinout

IH6208
(CERDIP, PDIP)
TOP VIEW



Functional Diagram



2 LINE BINARY ADDRESS INPUTS (0 0) AND EN = 5V (EN = “1” for +5V, “0” for 0V) ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON.

TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
x	x	0	None
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

NOTE: A_0, A_1
Logic “1” = $V_{AH} \geq 2.4V$, $V_{ENH} \geq 4.5V$
Logic “0” = $V_{AL} \leq 0.8V$.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3157.2**

Absolute Maximum Ratings

V_{IN} (A, EN) to Ground . . . . . -15V to 15V
V_S or V_D to V+ . . . . . 0V, -36V
V_S to V_D to V- 0V, 36V
V+ to Ground 18V
V- to Ground . . . . . -18V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA

Operating Conditions

Temperature Range
C Suffix . . . . . 0^oC to 70^oC
M Suffix . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	80	22
Ceramic Flatpack Package	85	25
PDIP Package	100	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V+ = 15V, V- = -15V, V_{EN} = +5V, Ground = 0V, Unless Otherwise Specified, (Note 4)

PARAMETER	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	TEST CONDITIONS	M SUFFIX (°C)			C SUFFIX (°C)			UNITS
					-55	25	125	0	25	70	
SWITCH											
$r_{DS(ON)}$	S to D	8	180	V_D = +10V, I_S = -1.0mA Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V	300	300	400	350	350	450	Ω
		8	150	V_D = -10V, I_S = -1.0mA Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V	300	300	400	350	350	450	Ω
$\Delta r_{DS(ON)}$			20	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG}}$, V_S = ±10V	-	-	-	-	-	-	%
$I_{S(OFF)}$	S	8	0.002	V_S = 10V, V_D = -10V	-	±0.5	±50	-	±1	±50	nA
		8	0.002	V_S = -10V, V_D = 10V, V_{EN} = 0.8V	-	±0.5	±50	-	±1	±50	nA
$I_{D(OFF)}$	D	2	0.03	V_D = 10V, V_S = -10V, V_{EN} = 0.8V	-	±2	±50	-	±5	±100	nA
		2	0.03	V_D = -10V, V_S = 10V, V_{EN} = 0.8V	-	±2	±50	-	±5	±100	nA
$I_{D(ON)}$	D	8	0.1	$V_{S(ALL)}$ = V_D = 10V, Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V	-	±2	±50	-	±5	±100	nA
		8	0.1	$V_{S(ALL)}$ = -10V, Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V	-	±2	±50	-	±5	±100	nA
INPUT											
$I_{AN(ON)}$	A_0, A_1	2	0.01	V_A = 0V	-	-10	-30	-	-10	-30	µA
$I_{AN(OFF)}$		2	0.01	V_A = 14V	-	10	30	-	10	30	µA
I_A	A_0, A_1	2	0.01	V_{EN} = 5V, All V_A = 0V (Address Pins)	-	-10	-30	-	-10	-30	µA
	EN	1	0.01	V_{EN} = 0V, All V_A = 0V (Address Pins)	-	-10	-30	-	-10	-30	µA

Electrical Specifications V+ = 15V, V- = -15V, V_{EN} = +5V, Ground = 0V, Unless Otherwise Specified, (Note 4) **(Continued)**

PARAMETER	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	TEST CONDITIONS	M SUFFIX (°C)			C SUFFIX (°C)			UNITS
					-55	25	125	0	25	70	
DYNAMIC											
$t_{TRANSITION}$	D		0.3	See Figure 1	-	1	-	-	-	-	µs
t_{OPEN}	D		0.2	See Figure 2	-	-	-	-	-	-	µs
$t_{EN(ON)}$	D		0.6	See Figure 3	-	1.5	-	-	-	-	µs
$t_{EN(OFF)}$	D		0.4	See Figure 3	-	1	-	-	-	-	µs
"OFF" Isolation	D		60	V_{EN} = 0V, R_L = 200Ω, C_L = 3pF, V_S = $3V_{RMS}$, f = 500kHz	-	-	-	-	-	-	dB
$C_{S(OFF)}$	S		5	V_S = 0V, V_{EN} = 0V, f = 140kHz to 1MHz	-	-	-	-	-	-	pF
$C_{D(OFF)}$	D		12	V_D = 0V, V_{EN} = 0V, f = 140kHz to 1MHz	-	-	-	-	-	-	pF
$C_{DS(OFF)}$	D to S		1	V_S = 0V, V_D = 0V, V_{EN} = 0V, f = 140kHz to 1MHz	-	-	-	-	-	-	pF
SUPPLY											
Positive Supply Current	V+	1	40	V_{EN} = 5V, All V_A = 0V or 5V	-	-	200	-	-	1000	µA
Negative Supply Current	V-	1	2	V_{EN} = 5V, All V_A = 0V or 5V	-	-	100	-	-	1000	µA
Positive Standby Current	V+	1	1	V_{EN} = 0V, All V_A = 0V or 5V	-	-	100	-	-	1000	µA
Negative Standby Current	V-	1	1	V_{EN} = 0V, All V_A = 0V or 5V	-	-	100	-	-	1000	µA

NOTE:

2. See "Enable Input Strobing Levels" in Application Section.

Switching Information

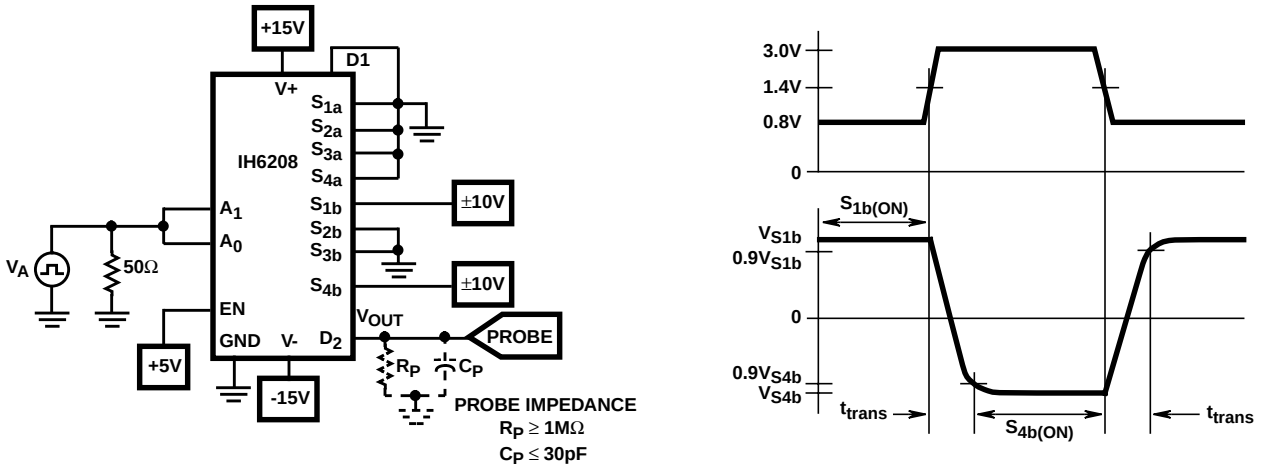


FIGURE 1. $t_{TRANSITION}$ SWITCHING TEST CIRCUIT AND WAVEFORMS

Switching Information (Continued)

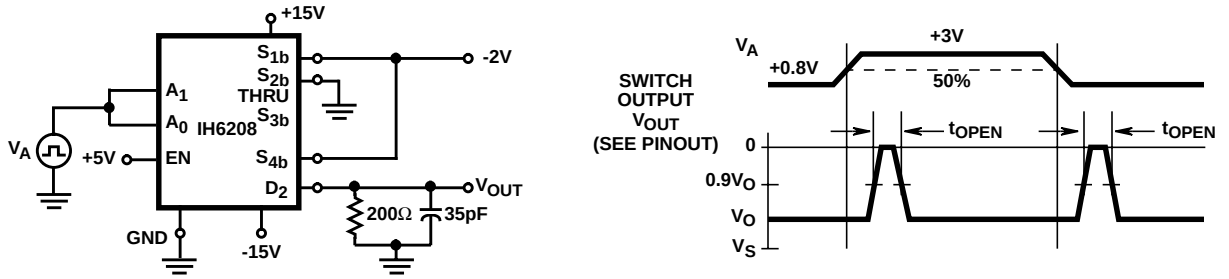


FIGURE 2. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TEST CIRCUIT AND WAVEFORMS

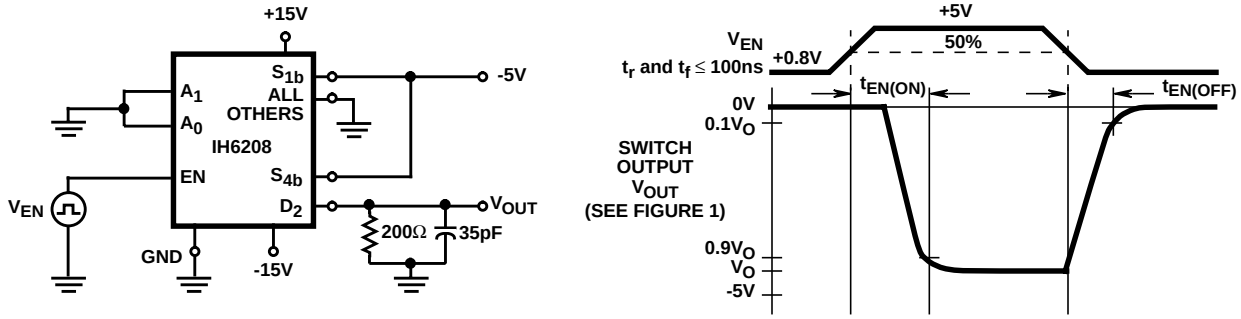


FIGURE 3. t_{ON} AND t_{OFF} SWITCHING TEST CIRCUIT AND WAVEFORMS

IH6208 Application Information

ENABLE Input Strobing Levels

The ENABLE input on the IH6208 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the ENABLE input is being driven from TTL logic, a pull-up resistor of 1kΩ to 3kΩ is required from the gate output to +5V supply. (See Figure 4)

When the EN in put is driven from CMOS logic, no pullup is necessary, see Figure 5.

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The following chart shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL T_{TRANS} AT 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENABLE Strobe Logic.

The examples shown in Figure 4 and 5 deal with ENABLE strobing when expansion to more than eight channels is required. In these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6208 at all times.

Using the IH6208 with Supplies Other Than ±15V

The IH6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(ON)}$ will increase as the supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(ON)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V+ at all times. If this is not done, the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V+ (pin 14) via a silicon diode as shown in Figure 6. When using this type of configuration, a further requirement must be met: the strobe levels of A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 6 the EN voltage is 11.3V which means that logic high at A0 and A1 is +8.8V (logic low continues to be 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V+ and EN, (See Figure 7). A 1µF capacitor can be placed across the diode to minimize switching glitches.

Switching Information

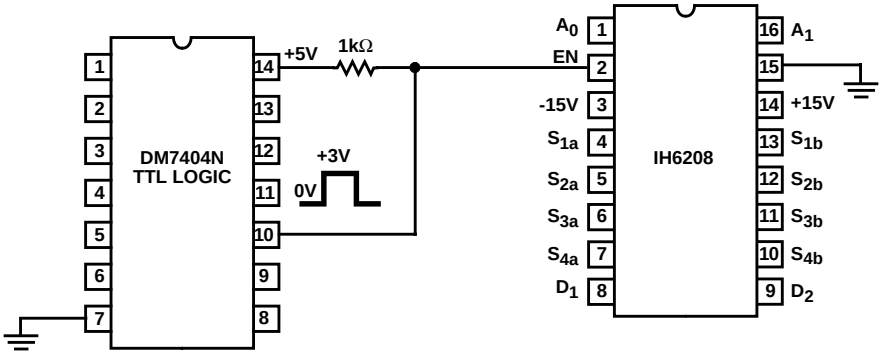


FIGURE 4. ENABLE INPUT STROBING FROM TTL LOGIC

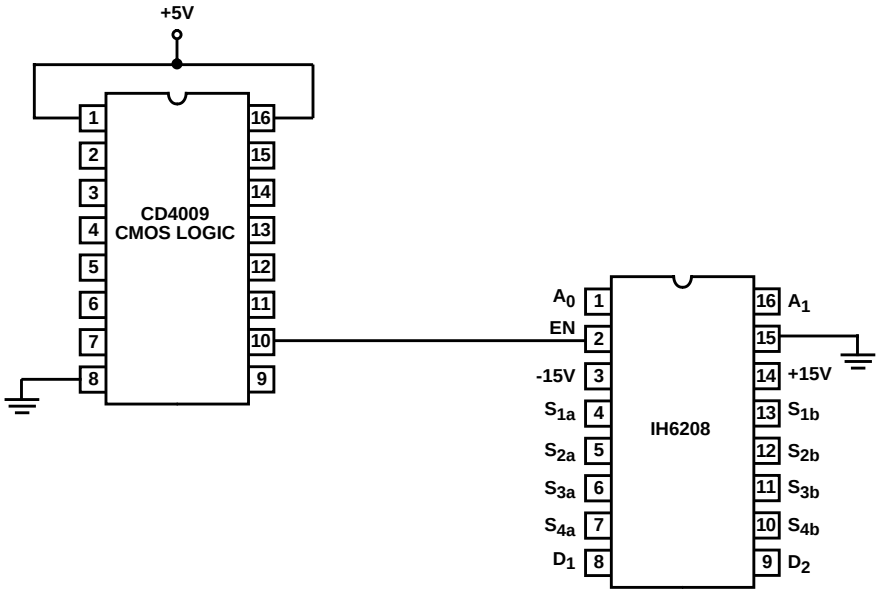


FIGURE 5. CMOS LOGIC DRIVING ENABLE PIN

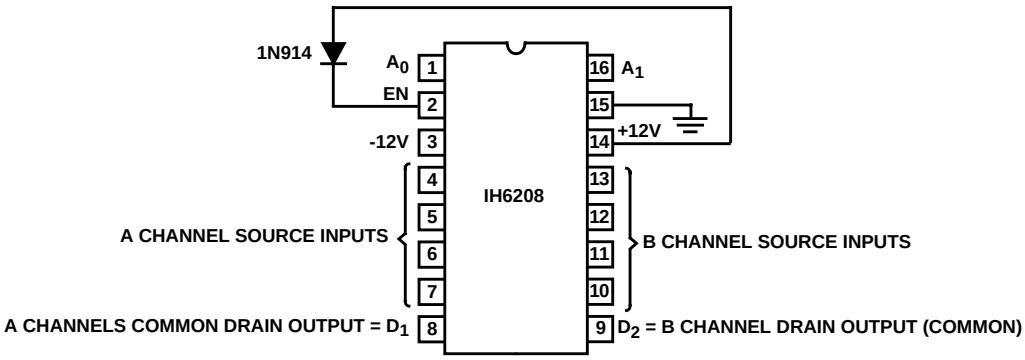


FIGURE 6. IH6208 CONNECTION DIAGRAM FOR LESS THAN ±15V SUPPLY OPERATION

Switching Information (Continued)

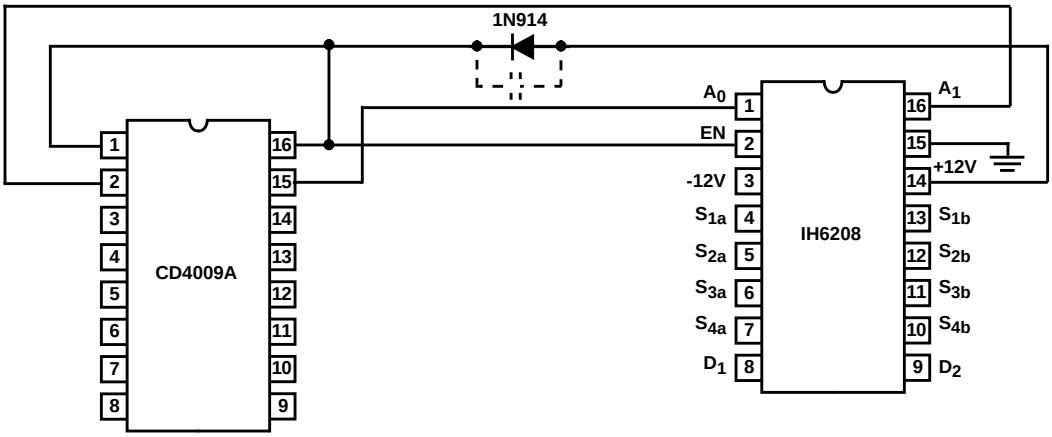


FIGURE 7. IH6208 CONNECTION DIAGRAM WITH ENABLE INPUT STROBING FOR LESS THAN ±15V SUPPLY OPERATION

Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually -15V to +14.3V because of the input protection diode) when using the ±15V supplies.

The electrical specifications of the IH6208 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(ON)}$ and slightly higher leakages.

Schematic Diagram

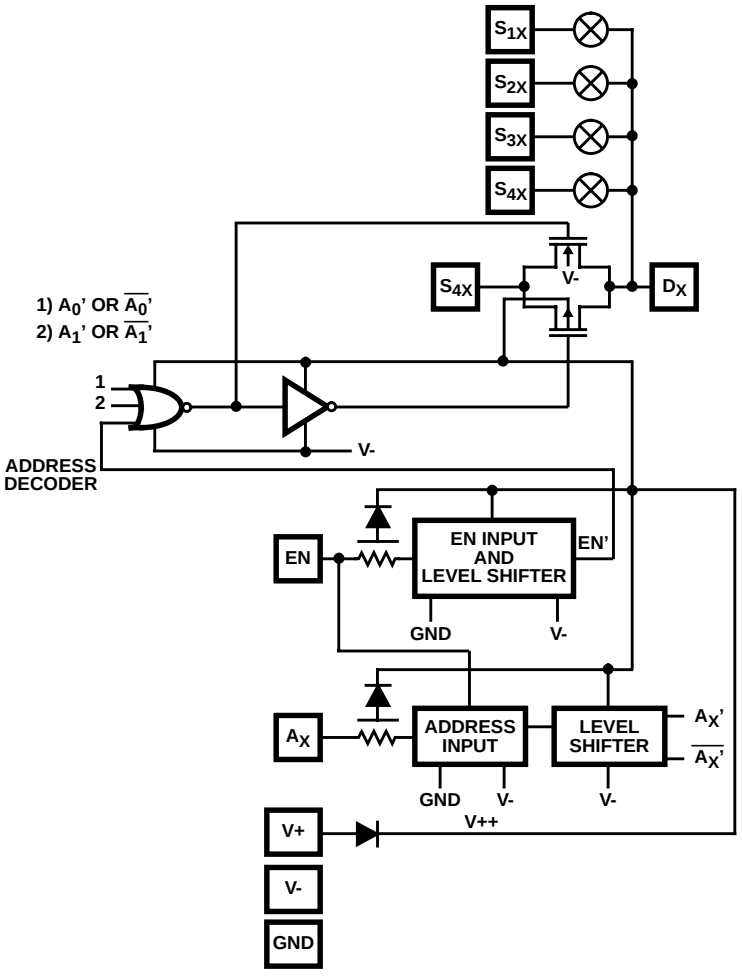


FIGURE 8. 1/2 IH6208 SCHEMATIC DIAGRAM

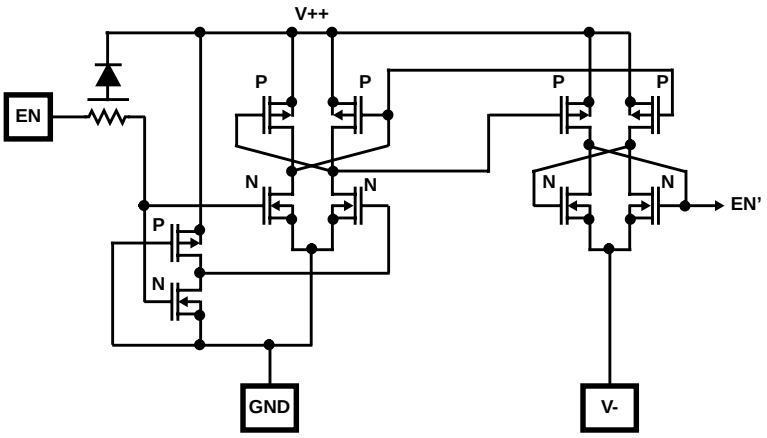


FIGURE 9. ENABLE INPUT AND LEVEL SHIFTER

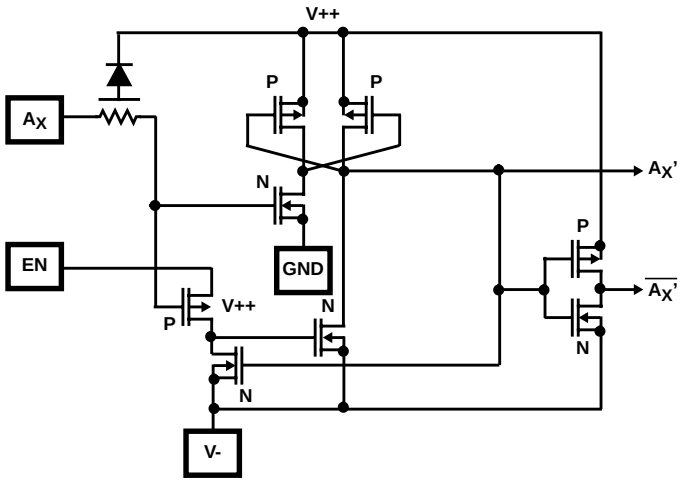


FIGURE 10. ADDRESS INPUT AND LEVEL SHIFTER