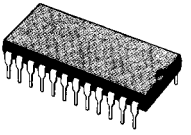
ETC9410/ETC9411 ETC9310/ETC9311

CMOS MICROCONTROLLERS

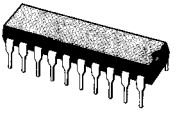
- LOWEST POWER DISSIPATION (40µW typical)
- LOW COST
- POWER SAVING HALT MODE WITH CONTINUE FUNCTION
- POWERFUL INSTRUCTION SET
- 512 x 8 ROM, 32 x 4 RAM
- 20 I/O LINES (ETC9410)
- TWO-LEVEL SUBROUTINE STACK
- DC TO 4µs INSTRUCTION TIME
- SINGLE SUPPLY OPERATION (2.4V to 5.5V)
- GENERAL PURPOSE AND TRI-STATE® OUTPUTS
- INTERNAL BINARY/COUNTER REGISTER WITH MICROWIRE® COMPATIBLE SERIAL I/O
- LSTTL/CMOS COMPATIBLE IN AND OUT
- SOFTWARE/HARDWARE COMPATIBLE WITH OTHER MEMBERS OF THE ET9400 FAMILY
- EXTENDED TEMPERATURE (- 40°C to + 85°C)
- S.O.I.C. 20/24 PACKAGE AVAILABLE

ETC9410/ETC9310



N
(Plastic Package)

ETC9411/ETC9311



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(Plastic Package)

DESCRIPTION

The ETC9410, C9411,C9310, and C9311, fully Static, Single-Chip CMOS Microcontrollers are fully compatible with the COPS® family, fabricated using double-poly, silicon gate CMOS technology. These Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETC9411 is identical to the ETC9410 but with 16 I/O lines instead of 20. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

The ETC9310/C9311 is the extended temperature range version of the ETC9410/C9411.

PIN CONNECTIONS

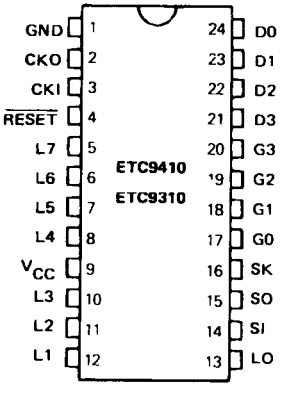
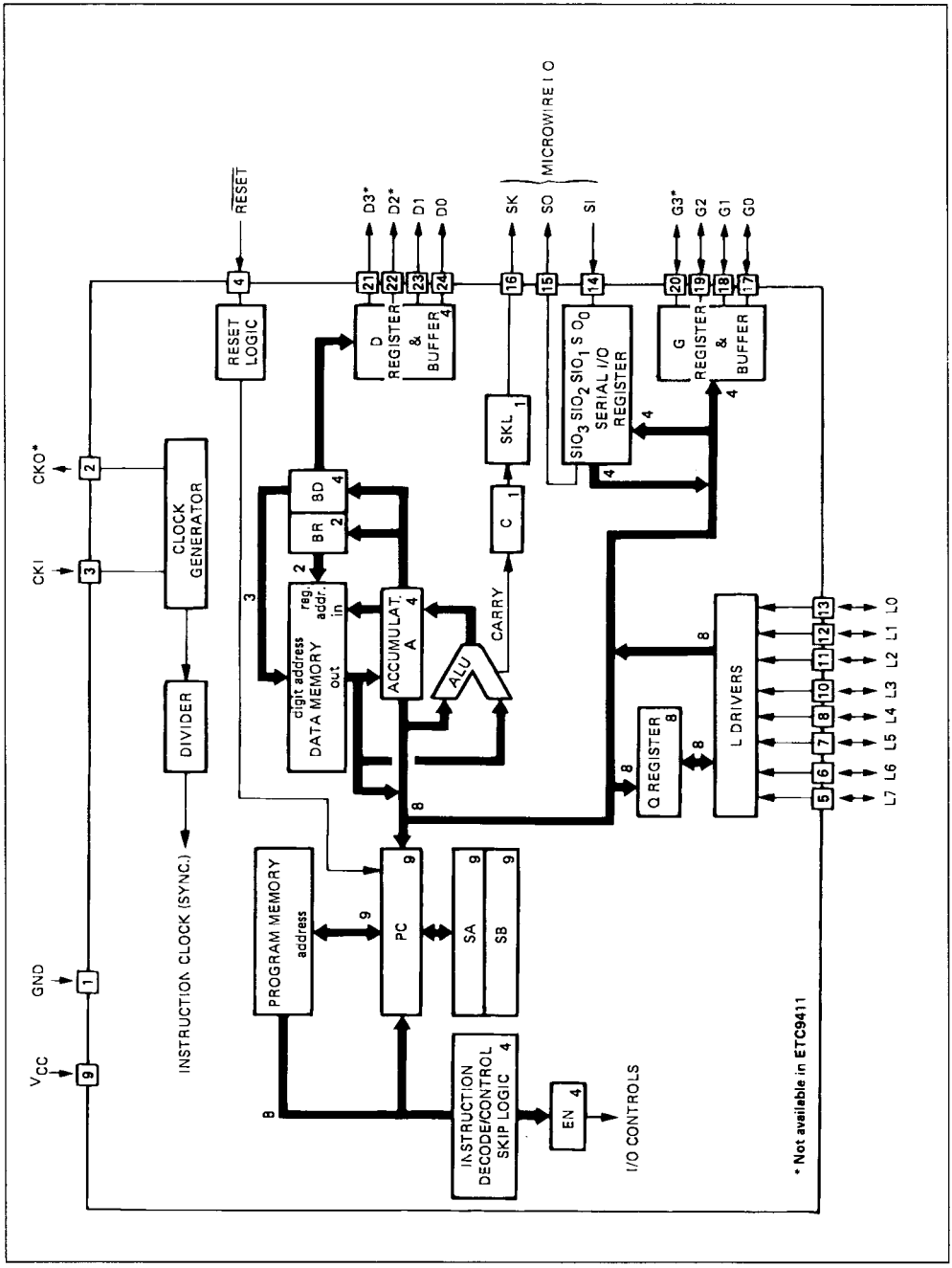


Figure 1 : Block Diagram (24-pin version).



ETC9410/ETC9411

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (V_{CC})	6	V
V_i	Voltage at any Pin Relative to GND	– 0.3 to V_{CC} + 0.3	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{stg}	Ambient Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (soldering, 10 seconds)	300	°C
	Total Source Current	25	mA
	Total Sink Current	25	mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C < T_A < +70°C$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (note 5)	Peak to Peak		$0.1V_{CC}$	
Supply Current (note 1)	V_{CC} = 2.4V, tc = 125µs		40	µA
	V_{CC} = 5.0V, tc = 16µs		500	µA
	V_{CC} = 5.0V, tc = 4µs		2000	µA
	(tc is the instruction cycle time)			
HALT Mode Current (note 2)	V_{CC} = 5.0V, Fin = 0kHz		15	µA
	V_{CC} = 2.4V, Fin = 0kHZ		6	µA
Input Voltage Levels				
RESET, CKI				
Logic High		$0.9V_{CC}$		V
Logic Low			$0.1V_{CC}$	V
All Other Inputs				
Logic High		$0.7V_{CC}$		V
Logic Low			$0.2V_{CC}$	V
Hi-Z Input Leakage		− 1	+ 1	µA
Input Capacitance			+ 7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ± 5%			
Logic High	IOH = − 25µA	2.7		V
Logic Low	IOL = 400µA		0.4	V
CMOS Operation				
Logic High	I_{OH} = − 10µA	V_{CC}–0.2		V
Logic Low	I_{OL} = 10µA		0.2	V
Output Current Levels	(except CKO)			
Sink (note 6)	V_{CC} = 4.5V, V_{out} = V_{CC}	1.2		mA
	V_{CC} = 2.4V, V_{out} = V_{CC}	0.2		mA
Source (standard option)	V_{CC} = 4.5V, V_{out} = 0V	0.5		mA
	V_{CC} = 2.4V, V_{out} = 0V	0.1		mA
Source (low current option)	V_{CC} = 4.5V, V_{out} = 0V	30	330	µA
	V_{CC} = 2.4V, V_{out} = 0V	6	80	µA
CKO (as clock out) Current Levels				
Sink	V_{CC} = 4.5V, CKI = V_{CC}, V_{out} = V_{CC}	0.3		mA
divide by 4		0.6		mA
divide by 8		1.2		mA
divide by 16				
Source	V_{CC} = 4.5V, CKI = V_{CC}, V_{out} = 0	0.3		mA
divide by 4		0.6		mA
divide by 8		1.2		mA
divide by 16				
Allowable Loading on CKO (as HALT)				
Current needed to over-ride HALT	(note 3)		100	pF
To continue	V_{CC} = 4.5V, ViN = $2V_{CC}$		.6	mA
To halt	V_{CC} = 4.5V, ViN = $7V_{CC}$		1.6	mA
TRI-STATE® or open drain leakage current.		− 2	+ 2	µA

ETC9410/ETC9411

AC ELECTRICAL CHARACTERISTICS $0°C < T_A < +70°C$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Units
Instruction Cycle Time = tc	$V_{CC} \geq 4.5V$	4	DC	µs
	$4.5V > V_{CC} \geq 2.4V$	16	DC	µs
Operating CKI Frequency	÷ 4 Mode, $V_{CC} \geq 4.5V$	DC	1.0	MHz
	÷ 8 Mode, $V_{CC} \geq 4.5V$	DC	2.0	MHz
	÷ 16 Mode, $V_{CC} \geq 4.5V$	DC	4.0	MHz
	÷ 4 Mode, $V_{CC} \geq 2.4V$	DC	250	kHz
	÷ 8 Mode, $V_{CC} \geq 2.4V$	DC	500	kHz
	÷ 16 Mode, $V_{CC} \geq 2.4V$	DC	1.0	MHz
Instruction Cycle Time - CKI (RC) (note 4)	R = 30k ± 5%, V_{CC} = 5V, C = 82pF ± 5% (÷ 4 mode)	8	16	µs
INPUTS : (see fig. 3)				
t_{SETUP}	G Inputs, $V_{CC} \geq 4.5V$	tc/4 = + 0.7		µs
	SI Input, $V_{CC} \geq 4.5V$	0.3		µs
	All Others, $V_{CC} \geq 4.5V$	1.7		µs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25		µs
	$V_{CC} \geq 2.4V$	1.0		µs
OUTPUT Propagation Delay (see fig. 3)	V_{out} = 1.5V, C_L = 100pF, R_L = 5K			
t_{PD1}, t_{PD0}	$V_{CC} \geq 4.5V$		1.0	µs
t_{PD1}, t_{PD0}	$V_{CC} \geq 2.4V$		4.0	µs

Note :
1. Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors.
2. The HALT mode will stop CKI from oscillating in the RC and crystal configurations.
3. When forcing HALT, current is only needed for a short time (approx. 200ns) to flip the HALT flip-flop.
4. This parameter is only sampled and not 100% tested.
5. Voltage change must be less than 0.5 volt in a 1ms period.
6. SO output sink current must be limited to keep V_{OL} below 0.2 V_{CC} when port is running in order to prevent entering test mode.

ETC9310/ETC9311

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (V_{CC})	6	V
V_i	Voltage at any Pin	− 0.3 to V_{CC} + 0.3	V
	Total Allowable Source Current	25	mA
	Total Allowable Sink Current	25	mA
T_{op}	Operating Temperature Range	− 40 to + 85	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C
T_L	Lead Temperature (soldering, 10 sec.)	300	°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS – 40°C ≤ T_A ≤ + 85°C (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Units
Operating Voltage		3.0	5.3	V
Power Supply Ripple (note 5)	Peak to Peak		$0.1V_{CC}$	V
Supply Current (note 1)	V_{CC} = 3.0V, t_c = 125µs V_{CC} = 5.0V, t_c = 16µs V_{CC} = 5.0V, t_c = 4µs (tc is the instruction cycle time)		60 600 2500	µA µA µA
HALT Mode Current (note 2)	V_{CC} = 5.0V, F_{IN} = 0kHz V_{CC} = 3.0V, F_{IN} = 0kHz		25 13	µA µA
Input Voltage Levels RESET, CKI Logic High Input Logic Low All Other Inputs Logic High Logic Low		 $0.9V_{CC}$ $0.7V_{CC}$	 $0.1V_{CC}$ $0.2V_{CC}$	 V V V V
Hi-Z Input Leakage		– 2	+ 2	µA
Input Capacitance			7	pF
Output Voltage Levels LSTTL Operation Logic High Logic Low CMOS Operation Logic High Logic Low	Standard Outputs V_{CC} = 5.0V ± 5% I_{OH} = 25µA I_{OL} = 400µA I_{OH} = – 10µA I_{OL} = 10µA	 2.7 V_{CC}–0.2 	 0.4 0.2	 V V V V
Output Current Levels Sink (note 6) Source (standard option) Source (low current option)	 V_{CC} = 4.5V, V_{out} = V_{CC} V_{CC} = 3.0V, V_{out} = V_{CC} V_{CC} = 4.5V, V_{out} = 0V V_{CC} = 3.0V, V_{out} = 0V V_{CC} = 4.5V, V_{out} = 0V V_{CC} = 3.0V, V_{out} = 0V	 1.2 0.2 0.5 0.1 30 8	 440 200	 mA mA mA mA µA µA
CKO Current Levels (as clock out) Sink ÷ 4 ÷ 8 ÷ 16 Source ÷ 4 ÷ 8 ÷ 16	 V_{CC} = 4.5V, CKI = V_{CC}, V_{out} = V_{CC} V_{CC} = 4.5V, CKI = 0V, V_{out} = 0V 	 0.3 0.6 1.2 0.3 0.6 1.2	 	 mA mA mA mA mA mA
Allowable Loading on CKO (as HALT I/O pin)			100	pF
Current needed to override HALT (note 3) to continue to halt	 V_{CC} = 4.5V, V_{IN} = 0.2V_{CC} V_{CC} = 4.5V, V_{IN} = 0.7V_{CC}		 0.8 2.0	 mA mA
TRI-STATE or Open Drain Leakage Current		– 4	+ 4	µA

ETC9310/ETC9311

AC ELECTRICAL CHARACTERISTICS – 40°C ≤ T_A ≤ + 85°C (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Units
Instruction Cycle Time (t_c)	V_{CC} ≤ 4.5V	4	DC	µs
	4.5V > V_{CC} ≥ 3.0V	16	DC	µs
Operating CKI Frequency ÷ 4 Mode		DC	1.0	MHz
÷ 8 Mode	V_{CC} ≥ 4.5V	DC	2.0	MHz
÷ 16 Mode		DC	4.0	MHz
÷ 4 Mode		DC	250	kHz
÷ 8 Mode	4.5V > V_{CC} ≥ 3.0V	DC	500	kHz
÷ 16 Mode		DC	1.0	MHz
Instruction Cycle Time RC Oscillator (note 4)	R = 30k ± 5%, V_{CC} = 5V C = 82pF ± 5% (÷ 4 mode)	8	16	µs
Inputs (see figure 3)				
t_{SETUP}	G Inputs	tc/4 = + 0.7		µs
	SI Input V_{CC} ≥ 4.5V	0.3		µs
	All Others	1.7		µs
t_{HOLD}	V_{CC} ≥ 4.5V	0.25		µs
	V_{CC} ≥ 3.0V	1.0		µs
Output Propagation Delay	V_{out} = 1.5V, C_L = 100pF, R_L = 5K			
t_{PD1}, t_{PD0}	V_{CC} ≥ 4.5V		1.0	µs
t_{PD1}, t_{PD0}	V_{CC} ≥ 3.0V		4.0	µs

Note : 1. Supply current is measured after running for 2000 cycle times with a square-ware clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors.
2. The HALT mode will stop CKI from oscillating in the RC and crystal configurations.
3. When forcing HALT, current is only needed for a short time (approximately 200ns) to flip the HALT flip-flop.
4. This parameter is only sampled and not 100% tested.
5. Voltage change must be less than 0.5 volt in a 1ms period.
6. SO output sink current must be limited to keep V_{OL} below 0.2V_{CC} when port is running in order to prevent entering test mode.

FUNCTIONAL DESCRIPTION

To ease reading of this description, only ETC9410 and/or ETC9411 are referenced ; however, all such references apply equally to ETC9310 and/or ETC9311.

A block diagram of the ETC9410 is given in figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is logic "1" when a bit is reset, it is a logic "0".

PROGRAM MEMORY

Program memory consists of a 512-byte ROM. As can be seen by an examination of the ETC9410/C 9411 instruction set, these words may be program instructions, program data, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of being organized into 8 pages of 64 words (bytes) each.

ROM ADDRESSING

ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by two 9-bit subroutine save registers, SA and SB.

ROM instruction words are fetched, decoded, and executed by the Instruction Decode, Control and Skip Logic circuitry.

DATA MEMORY

Data memory consists of a 128-bit RAM, organized as 4 data registers of 8 x 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper 2 bits (Br) select 1 of 4 data registers and lower 3 bits of the 4-bit Bd select 1 of eight 4-bit digits in the selected data register. While the 4-bit contents of

the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3, 15 instruction. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

The most significant bit of Bd is not used to select a RAM digit. Hence, each physical digit of RAM may be selected by two different values of Bd as shown in figure 4 below. The skip condition for XIS and XDS instructions will be true if Bd changes between 0 and 15, but NOT between 7 and 8 (see table 3).

Figure 2 : Pin Connections.

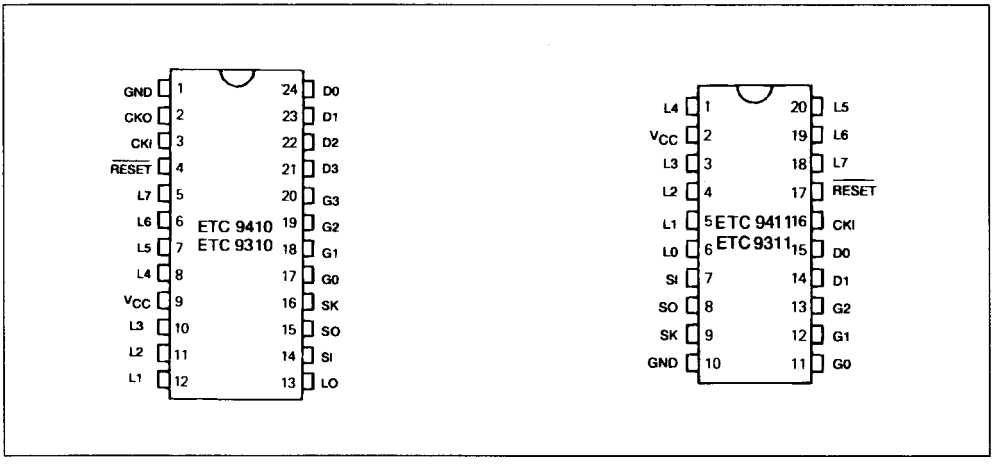
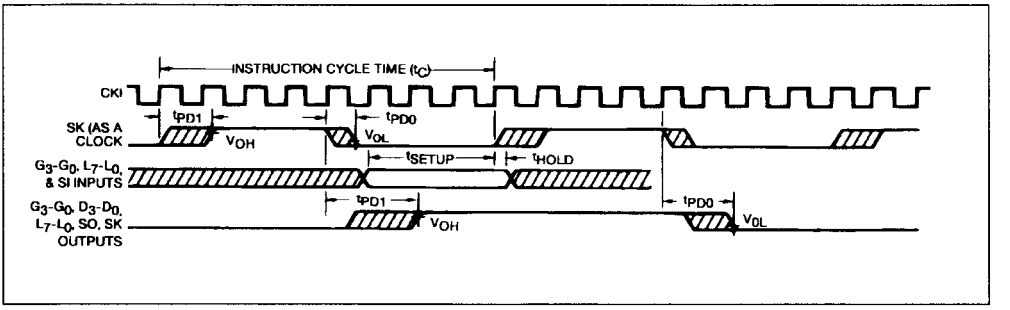


Figure 2 : Pin Connections.

Pin	Description
L_7-L_0	8 Bidirectional I/O Ports with TRI-STATE®
G_3-G_0	4 Bidirectional I/O Ports (G_2-G_0 for 20 pin package)
D_3-D_0	4 General Purpose Outputs (D_1-D_0 for 20 pin package)
SI	Serial Input (or counter input)
SO	Serial Output (or general purpose output)
SK	Logic-controlled Clock (or general purpose output)
CKI	System Oscillator Input
CKO	Crystal Oscillator Output (or HALT mode I/O port) (24 pin package only)
$\overline{\text{RESET}}$	System Reset Input
V_{CC}	System Power Supply
GND	System Ground

Figure 3 : Input/output Timing Diagrams (divide-by-8 mode).



The D register provides 4 general purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The XAS instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL ; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0".

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, DECREMENTING its value by one upon each low going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least 2 (two) instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN3. With EN0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each instruction cycle time. (See 4 below). The SK output becomes a logic controlled clock.
2. EN1 is not used, it has NO effect on the ETC9410/C9411.
3. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN2 disables the L drivers, placing the L I/O ports in a hight impedance input state.
4. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected), SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected, disables SO as the shift register output : data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

ENABLE REGISTER MODES - BITS EN_3 AND EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

INTERNAL LOGIC

The internal logic of the ETC9410/C9411 is designed to insure fully static operation of the device.

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the register, to load 4 bits of the 8-bit Q latch data and to perform data exchanges with the SIO register.

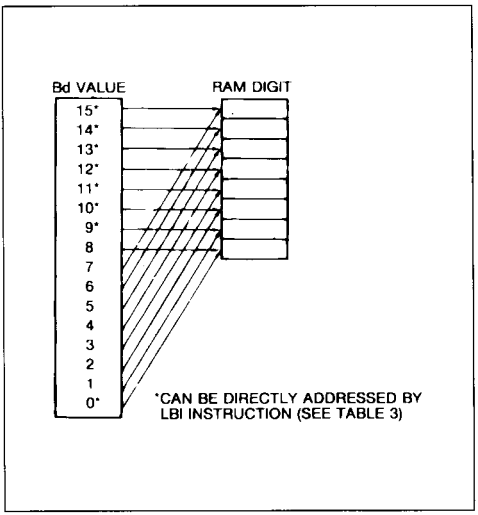
A 4-bit adder performs the arithmetic and logic functions of the ETC9410/C9411, storing its results in A. It also outputs the carry information to a 1-bit carry register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be output directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description below).

The G register contents are outputs to 4 general-purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from RAM and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction).

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and RAM.

Figure 4 : RAM Digit Address to Physical RAM Digit Mapping.



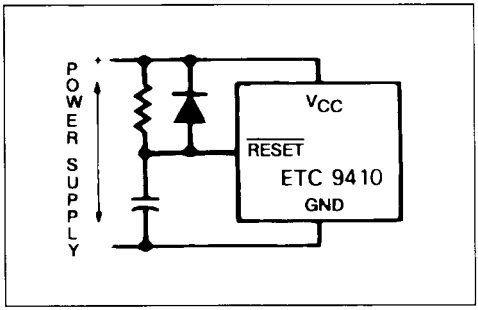
The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending upon the contents of the EN register. (See EN register description above). Its contents can be exchanged with A, allowing it to input or output continuous serial data stream. With SIO functioning as a serial-in/serial-out shift register and SK as a sync-clock, the ETC9410/C9411 is MICROWIRE® compatible.

INITIALIZATION

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1ms and if the operating frequency at CKI is greater than 32kHz, otherwise the external RC network shown in figure 5 must be connected to the RESET pin. The RESET pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the RESET input, providing it stays low for at least three instruction cycle times.

Note : If CKI clock is less than 32kHz, the internal reset logic (option 25 = I) MUST be disabled and the external RC network must be present.

Figure 5 : Power-up Clear Circuit.



RC > 5 x Power Supply Rise Time and RC > 100 x CKI period.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

HALT MODE

The ETC9410/C9411 is a FULLY STATIC circuit ; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may also be halted

by the HALT instruction or by forcing CKO high when it is used as an HALT I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The HALT mode is the minimum power dissipation state.

The HALT mode has slight differences depending upon the type of oscillator used.

a) One-pin oscillator - (RC or External)

The HALT mode may be entered into by either program control (HALT instruction) or by forcing CKO to a logic "1" state.

The circuit may be awakened by one of two different methods :

1. Continue function - by forcing CKO to a logic "0", the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.
2. Restart - forcing the RESET pin to a logic "0" will restart the chip regardless of HALT or CKO (see Initialization).

b) Two-pin oscillator - (Crystal)

The HALT mode may be entered into by program control (HALT instruction) which forces CKO to a logic "1" state. The circuit can be awakened only by the RESET function.

ETC9411

If the ETC9410 is bonded as a 20-pin package, it becomes the ETC9411 illustrated in figure 2, ETC9410/C9411 Connection Diagrams. Note that the ETC9411 does not contain D2, D3, G3, or CKO. Use of this option of course precludes use of D2, D3, G3, and CKO options. All other options are available for the ETC9411.

CKO PIN OPTIONS

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. CKO will be forced high during the execution of a HALT instruction, thus inhibiting the crystal network. If a one pin oscillator system is chosen (RC or external), CKO will be a selected as HALT and is an I/O flip-flop which is an indicator of the HALT status. An external signal can over ride this pin to start and stop the chip. By forcing a high level to CKO ; the chip wil stop as soon as CKI is high and the CKO output will go high to keep the chip stopped. By forcing a low level to CKO, the chip will continue and CKO output will go low.

All features associated with the CKO I/O pin are available with the 24-pin package only.

OSCILLATOR OPTIONS

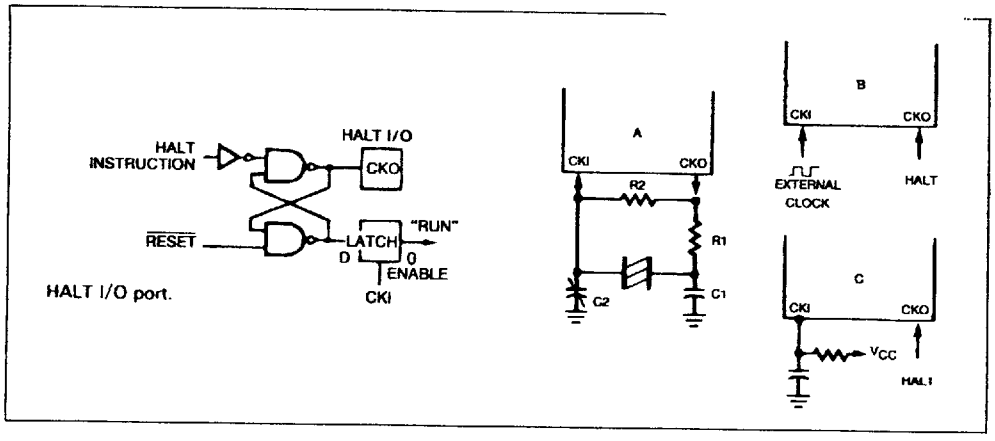
There are three options available that define the use of CKI and CKO.

a) Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optionally by 8 or 4).

b) External Oscillator. CKI is configured as a LSTTL compatible input accepting an external clock signal. The external frequency is divided by 16 (optionally by 8 or 4) to give the instruction cycle time. CKO is the HALT I/O port.

c) RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port.

Figure 6 : ETC9410C Oscillator.



CRYSTAL OR RESONATOR

Crystal Value	Component Values R1	R2	C1(pF)	C2(pF)
32kHz	220k	20M	30	5.36
455kHz	5k	10M	80	40
2.096MHz	2k	1M	30	5.36
4MHz	1k	1M	30	5.36

This circuit and these values are for indication only. As the oscillator characteristics are not guaranteed, please consider and examine the circuit constants carefully on your application

R/C CONTROLLED OSCILLATOR

R	C	Cycle Time	V_{CC}
15k	82pF	4 to 9µs	≥ 4.5V
30k	82pF	8 to 16µs	≥ 4.5V
60k	100pF	16 to 32µs	2.4 to 4.5V

Note : 15k ≤ R ≤ 150k
50pF ≤ C ≤ 150pF

I/O OPTIONS

ETC9410/C9411 outputs have the following optional configurations, illustrated in figure 7 :

a) Standard - A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b) Low Current - This is the same configuration as a) above except that the sourcing current much less.

c) Open Drain - An N-channel device to ground only, allowing external pull-up as required by the user's application.

d) Standard TRI-STATE® L Output - A CMOS output buffer similar to a) which may be disabled by program control.

e) Low-Current TRI-STATE® L Output - This is the same as d) above except that the sourcing current is much less.

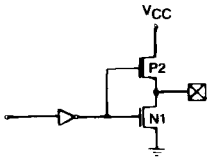
f) Open-Drain TRI-STATE® L Output - This has the N-channel device to ground only.

The SI and RESET inputs are Hi-Z inputs (fig. 7g).

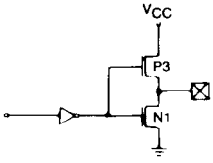
When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available : Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction.

All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{out} V_{out} curves are given in figure 8 for each of these devices to allow the designer to effectively use these I/O configurations.

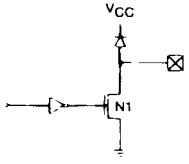
Figure 7 : Input and Output Configurations.



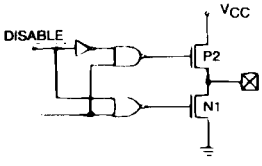
a) Standard Push Pull Output



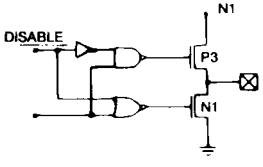
b) Low Current Push Pull Output



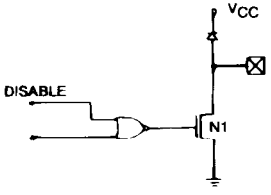
c) Open Drain Output



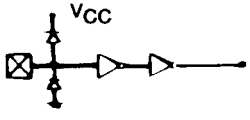
d) Standard TRI-STATE® "L" Output



e) Low Current TRI-STATE® "L" Output

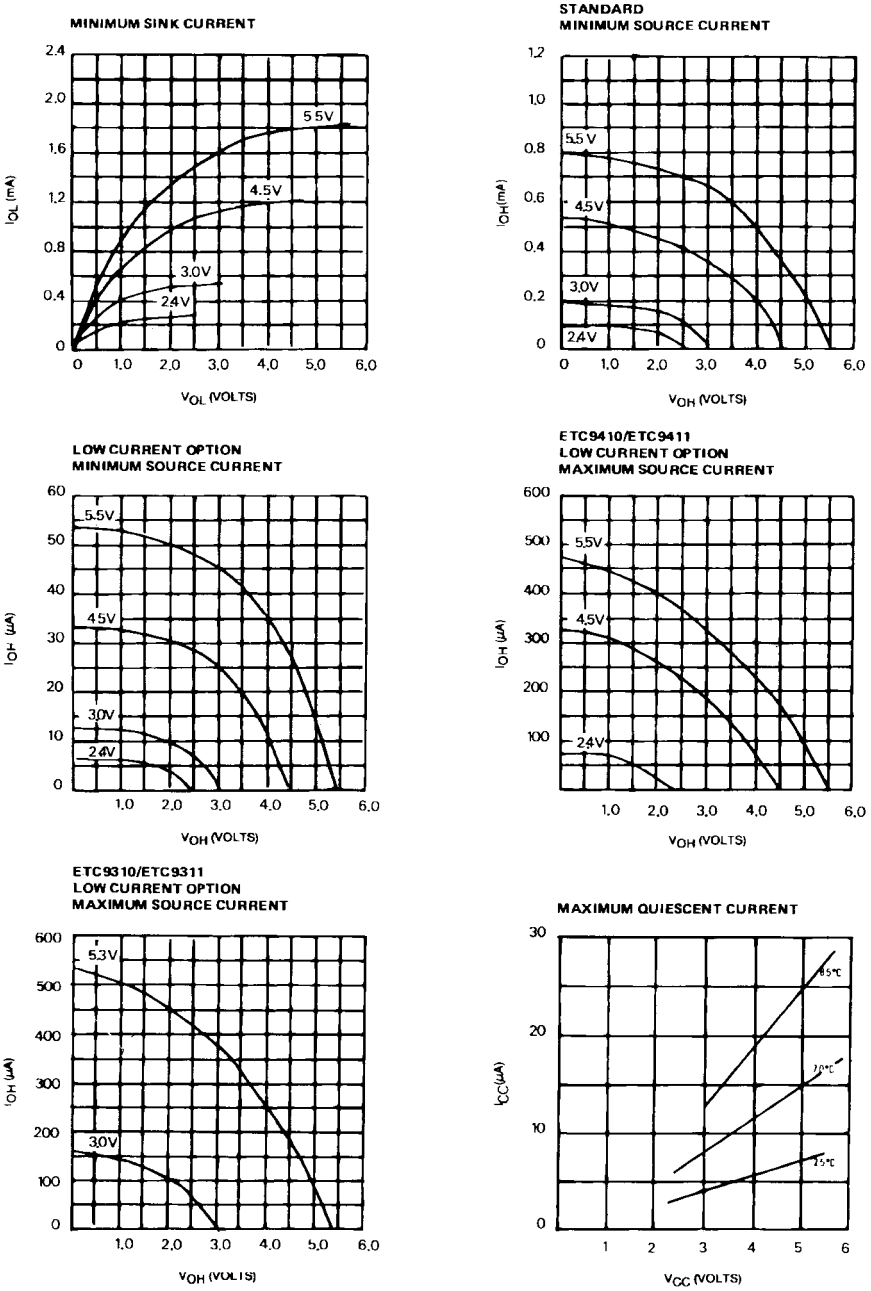


f) Open Drain TRI-STATE® "L" Output



g) Hi-Z Input

Figure 8 : Input/output Characteristics.



ETC9410/C9411 INSTRUCTION SET

Table 2 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine, code, data flow, skip conditions and description associated with each instruction in theETC9410/C9411 instruction set.

Table 2 : ETC9410/C9411 Instruction Set Table Symbols.

INTERNAL ARCHITECTURE SYMBOLS

Symbol	Definition
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 Bits of B (register address)
Bd	Lower 4 Bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to Latch Data for G I/O Port
L	8-bit TRI-STATE I/O Port
M	4-bit Contents of RAM Memory Pointed to by B Register
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to Latch Data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-controlled Clock Output

INSTRUCTION OPERAND SYMBOLS

Symbol	Definition
d	4-bit Operand Field, 0-15 Binary (RAM digit select)
r	2-bit Operand Field, 0-3 Binary (RAM register select)
a	9-bit Operand Field, 0-511 Binary (ROM address)
y	4-bit Operand Field, 0-15 Binary (immediate data)
RAM(s)	Contents of RAM location addressed by s.
ROM(t)	Contents of RAM location addressed by t.

OPERATIONAL SYMBOLS

Symbol	Definition
+	Plus
-	Minus
→	Replaces
‹ ›	Is exchanged with.
=	Is equal to.
$\bar{A}$	The one's complement of A.
⊕	Exclusive-OR
:	Range of Values

Table 3 : ETC9410/C9411 Instruction Set.

ARITHMETIC INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ASC		30	0 0 1 1 | 0 0 0 0	A + C RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0 0 1 1 | 0 0 0 1	A + RAM(B) → A	None	Add RAM to A
AISC	y	5-	0 1 0 1 | Y	A + y → A	Carry	Add Immediate Skip on Carry (y ≠ 0)
CLRA		00	0 0 0 0 | 0 0 0 0	0 → A	None	Clear A
COMP		40	0 1 0 0 | 0 0 0 0	$\bar{A}$ → A	None	One's Complement of A to A
NOP		44	0 1 0 0 | 0 1 0 0	None	None	No Operation
RC		32	0 0 1 1 | 0 0 1 0	"0" → C	None	Reset C
SC		22	0 0 1 0 | 0 0 1 0	"1" → C	None	Set C
XOR		02	0 0 0 0 | 0 0 1 0	A ⊕ RAM(B) → A	None	Exclusive-OR Ram with A

TRANSFER OF CONTROL INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
JID		FF	1 1 1 1 | 1 1 1 1	ROM (PC_8 A, M) → $PC_{7:0}$	None	Jump Indirect
JMP	a	6–	0 1 1 0 | 0 0 0 | a_8 $a_{7:0}$	a → PC	None	Jump
JP	a		1 | $a_{6:0}$ (pages 2,3 only) or 1 1 | $a_{5:0}$	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (note 1)
JSRP	a		1 0 | $a_{5:0}$	PC + 1 → SA → SB 010 → $PC_{8:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (note 2)
JSR	a	6–	0 1 1 0 | 1 0 0 | a $a_{7:0}$	PC + 1 → SA → SB a → PC	None	Jump to Subroutine
RET		48	0 1 0 0 | 1 0 0 0	SB → SA → PC	None	Return from Subroutine
RETSK		49	0 1 0 0 | 1 0 0 1	SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33 38	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 0 0 0		None	Halt Processor

MEMORY REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAMQ		33 3C	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 1 0 0	A → $Q_{7:4}$ RAM (B) → $Q_{3:0}$	None	Copy A, RAM to Q
LD	r	-5	0 0 r | 0 1 0 1	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LQID		BF	1 0 1 1 | 1 1 1 1	ROM ($PC_{8A.M}$) → Q SA → SB	None	Load Q Indirect
RMB	0 1 2 3	4C 45 42 43	0 1 0 0 | 1 1 0 0 0 1 0 0 | 0 1 0 1 0 1 0 0 | 0 0 1 0 0 1 0 0 | 0 0 1 1	0 → RAM $(B)_0$ 0 → RAM $(B)_1$ 0 → RAM $(B)_2$ 0 → RAM $(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0 1 0 0 | 1 1 0 1 0 1 0 0 | 0 1 1 1 0 1 0 0 | 0 1 1 0 0 1 0 0 | 1 0 1 1	1 → RAM $(B)_0$ 1 → RAM $(B)_1$ 1 → RAM $(B)_2$ 1 → RAM $(B)_3$	None	Set RAM Bit
STII	y	7-	0 1 1 1 | y	y → RAM (B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	-6	0 0 | r | 0 1 1 0	RAM (B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3,15	23 BF	0 0 1 0 | 0 0 1 1 1 0 1 1 | 1 1 1 1	RAM (3,15) ↔ A	None	Exchange A with RAM (3,15)
XDS	r	7	0 0 | r | 0 1 1 1	RAM (B) ↔ A Bd - 1 → Bd Br ⊕ r → Br	Bd Decrements Past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	4	0 0 | r | 0 1 0 0	RAM (B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd Increments Past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

REGISTER REFERENCE INSTRUCTION

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAB		50	0 1 0 1 | 0 0 0 0	A → Bd	None	Copy A to Bd
CBA		4E	0 1 0 0 | 1 1 1 0	Bd → A	None	Copy Bd to A
LBI	r.d	5-	0 0 | r | (d-1) (d = 0.915)	r.d → B	Skip until not a LBI	Load B Immediate with r.d
LEI	y	33 6-	0 0 1 1 | 0 0 1 1 0 1 1 0 | y	y → EN	None	Load EN Immediate

TEST INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
SKC		20	0010 0000		C = "1"	Skip if C is true.
SKE		21	0010 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011 0011 0010 0001		$G_{3:0} = 0$	Skip if G is zero (all 4 bits).
SKGBZ		33	0011 0011	1st Byte		Skip if G Bit is zero.
	0	01	0000 0001	2nd Byte	$G_0 = 0$	
	1	11	0001 0001		$G_1 = 0$	
	2	03	0000 0011		$G_2 = 0$	
	3	13	0001 0011		$G_3 = 0$	
SKMBZ	0	01	0000 0001		$RAM(B)_0 = 0$	Skip if RAM Bit is zero.
	1	11	0001 0001		$RAM(B)_1 = 0$	
	2	03	0000 0011		$RAM(B)_2 = 0$	
	3	13	0001 0011		$RAM(B)_3 = 0$	

INPUT/OUTPUT INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ING		33 2A	0011 0011 0010 1010	G → A	None	Input G Ports to A
INL		33 2E	0011 0011 0010 1110	$L_{7:4}$ → RAMB(B) $L_{3:0}$ → A	None	Input L Ports to RAM. A
OBD		33 3E	0011 0011 0011 1110	Bd → D	None	Output Bd to D Outputs
OMG		33 3A	0011 0011 0011 1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100 1111	A ↔ SIO, C → SKL	None	Exchange A with SIO

Note : 1. The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

2. A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing ETC9410 C9411.

XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM Addressed by the 9-bit word, PC_8, A, M, PC_8 is not affected by this instruction.

Note : That JID requires 2 instruction cycles to execute.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 9-bit word PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1→SA→SB) and replaces the least significant 8 bits of PC as follows : A→$PC_{7:4}$ RAM (B)→$PC_{3:0}$ leaving PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SB→SA→PC), restoring the saved value of PC to continue sequential program execution. Since LQID pusches SA→SB, the previous contents of SB are lost. Also, when LQID pops the stack, the previously pushed contents of SA are left in SB. The net result is that the contents of SA are placed in SB (SA→SB). Note that LQID takes two instruction cycle times to execute.

INSTRUCTION SET NOTES

a) The first word of a ETC9410/C9411 program (ROM address 0) must be a CLRA (Clear A) instruction.

b) Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c) The ROM is organized into 8 pages of 64 words each. The Program Counter is a 9-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example : a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3 or 7 will access data in the next group of 4 pages.

OPTION LIST

The ETC9410/ETC9411 mask-programmable options are assigned numbers which correspond with the ETC9410 pins.

The following is a list of ETC9410 options. When specifying a ETC9411 chip, Options 20, 21, and 22 must be set to 0. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 : = 0 : Ground Pin. No options available.

Option 2 : CKO I/O Port. Determined by Option 3.

Option 3 : CKI Input
- = 0 : Crystal controlled oscillator input (- 4).
- = 1 : Single-pin RC-controlled oscillator (- 4).
- = 2 : External oscillator input (- 4).
- = 3 : Crystal oscillator input (- 8).
- = 4 : External oscillator input (- 8).
- = 5 : Crystal oscillator input (- 16).
- = 6 : External oscillator input (- 16).

Option 4 : RESET Input = 1 : Hi-Z input. No option available

Option 5 : L_7 Driver
- = 0 : Standard TRI-STATE push-pull output
- = 1 : Low-current TRI-STATE push-pull output
- = 2 : Open-drain TRI-STATE output

Option 6 : L_6 Driver. (Same as Option 5.)

Option 7 : L_5 Driver (Same as Option 5.)

Option 8 : L_4 Driver : (Same as Option 5.)

Option 9 : V_{CC} Pin.

Option 10 : L_3 Driver. (Same as Option 5.)

Option 11 : L_2 Driver. (Same as Option 5.)

Option 12 : L_1 Driver. (Same as Option 5.)

Option 13 : L_0 Driver. (Same as Option 5.)

Option 14 : SI Input.
- No option available.
- = 1 : Hi-Z input

Option 15 : SO Output.
- = 0 : Standard push-pull output.
- = 1 : Low-current push-pull output.
- = 2 : Open-drain output.

Option 16 : SK Driver. (Same as Option 15.)

Option 17 : G_0 I/O Port. (Same as Option 15.)

Option 18 : G_1 I/O Port. (Same as Option 15.)

Option 19 : G2 I/O Port. (Same as Option 15.)

Option 20 : G_3 Output. (Same as Option 15.)

Option 21 : D_3 Output. (Same as Option 15.)

Option 22 : D_2 Output. (Same as Option 15.)

Option 23 : D_1 Output. (Same as Option 15.)

Option 24 : D_0 Output. (Same as option 15.)

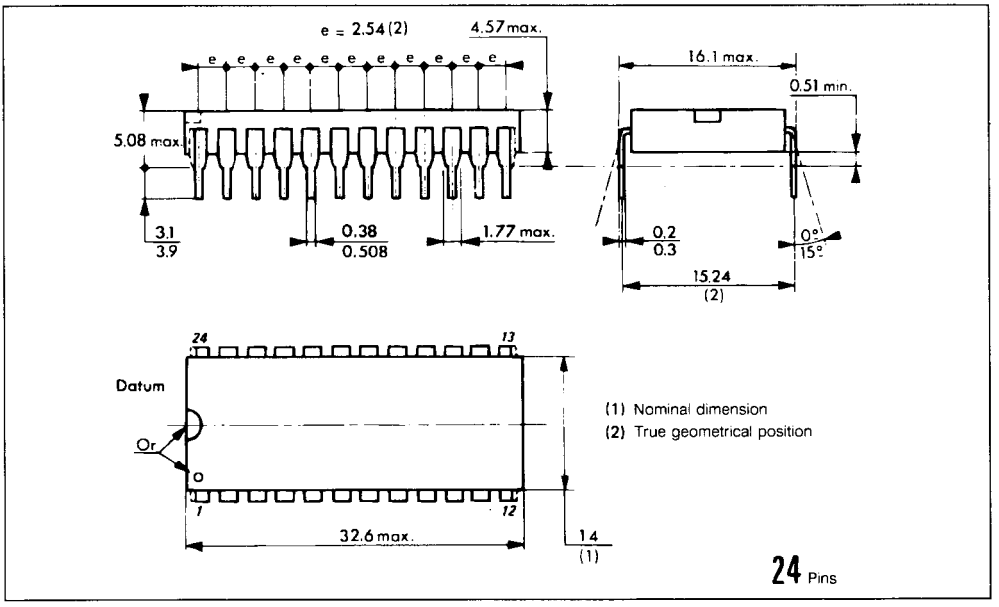
Option 25 : Internal Initialization logic.
- = 0 : Normal operation.
- = 1 : No internal initialization Logic

Option 26 : No option available.

Option 27 : Chip Bonding
- = 0 : ETC9410 (24-pin device).
- = 1 : ETC9411 (20-pin device).
- = 2 : ETC9410 and ETC9411.

PHYSICAL DIMENSIONS

24–PINS – PLASTIC PACKAGE



20–PINS – PLASTIC PACKAGE