

54F/74F373

Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'F373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

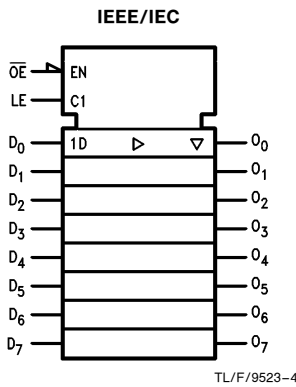
Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

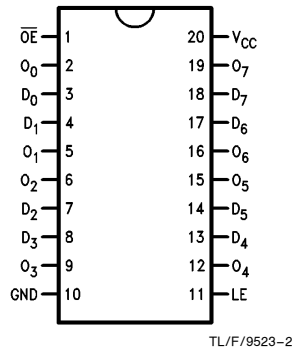
| Commercial | Military | Package Number | Package Description |
|--------------------|---------------|----------------|---|
| 74F373PC | | N20A | 20-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F373DM (QB) | J20A | 20-Lead Ceramic Dual-In-Line |
| 74F373SC (Note 1) | | M20B | 20-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74F373SJ (Note 1) | | M20D | 20-Lead (0.300" Wide) Molded Small Outline, EIAJ |
| 74F373MSA (Note 1) | | MSA20 | 20-Lead Molded Shrink Small Outline, EIAJ Type II |
| | 54F373FM (QB) | W20A | 20-Lead Cerpack |
| | 54F373LM (QB) | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX, and MSAX.

Logic Symbols

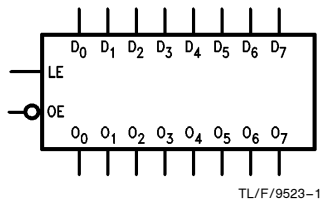
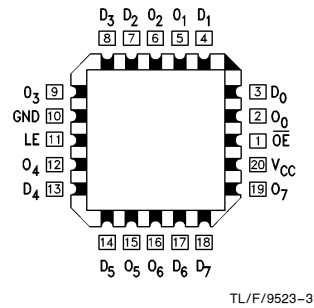


Pin Assignment for DIP, SOIC, SSOP and Flatpak



Connection Diagrams

Pin Assignment for LCC



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54F/74F373 Octal Transparent Latch with TRI-STATE Outputs

Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|-----------------|----------------------------------|------------------|---|
| | | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
| D_0-D_7 | Data Inputs | 1.0/1.0 | 20 μA / -0.6 mA |
| LE | Latch Enable Input (Active HIGH) | 1.0/1.0 | 20 μA / -0.6 mA |
| \overline{OE} | Output Enable Input (Active LOW) | 1.0/1.0 | 20 μA / -0.6 mA |
| O_0-O_7 | TRI-STATE Latch Outputs | 150/40 (33.3) | -3 mA / 24 mA (20 mA) |

Functional Description

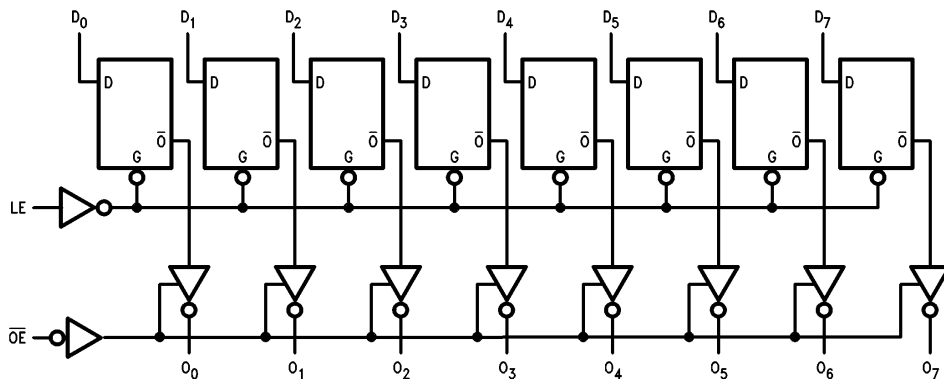
The 'F373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

| Inputs | | | Output |
|--------|-----------------|-------|-------------------|
| LE | \overline{OE} | D_n | O_n |
| H | L | H | H |
| H | L | L | L |
| L | L | X | O_n (no change) |
| X | H | X | Z |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance State

Logic Diagram



TL/F/9523-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +175°C |
| Plastic | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

| | |
|---|--------------------------------------|
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| TRI-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | -55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

DC Electrical Characteristics

| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|--|--|-------------|-------|-----------------|--|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC} | 2.5 2.4 2.5 2.4 2.7 2.7 | | V | Min | I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} 74F 10% V _{CC} | | 0.5 0.5 | V | Min | I _{OL} = 20 mA I _{OL} = 24 mA |
| I _{IH} | Input HIGH Current | 54F 74F | | 20.0 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F 74F | | 100 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | 54F 74F | | 250 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V |
| I _{OZH} | Output Leakage Current | | | 50 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | -50 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | | | -60 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCZ} | Power Supply Current | | 38 | 55 | mA | Max | V _O = HIGH Z |

AC Electrical Characteristics

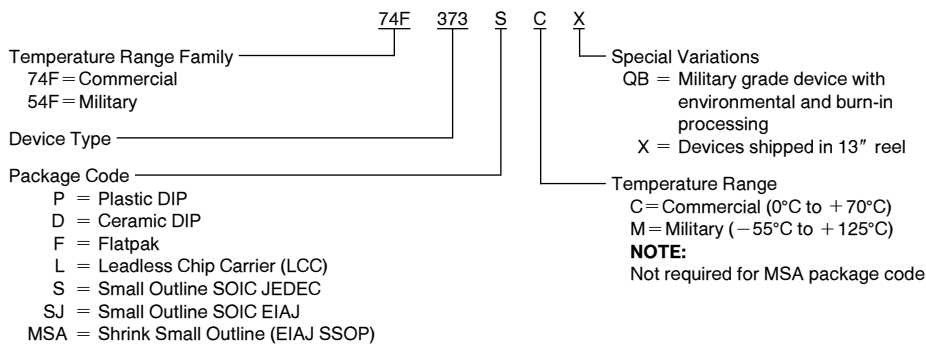
| Symbol | Parameter | 74F | | | 54F | | 74F | | Units |
|--------------------------------------|---|---|-----|------|--|------|--|------|-------|
| | | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A , V _{CC} = Mil C _L = 50 pF | | T _A , V _{CC} = Com C _L = 50 pF | | |
| | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} t _{PHL} | Propagation Delay D _n to O _n | 3.0 | 5.3 | 7.0 | 3.0 | 8.5 | 3.0 | 8.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay LE to O _n | 5.0 | 9.0 | 11.5 | 5.0 | 15.0 | 5.0 | 13.0 | |
| t _{PZH} t _{PZL} | Output Enable Time | 2.0 | 5.0 | 11.0 | 2.0 | 13.5 | 2.0 | 12.0 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time | 1.5 | 4.5 | 6.5 | 1.5 | 10.0 | 1.5 | 7.5 | |
| | | 1.5 | 3.8 | 5.0 | 1.5 | 7.0 | 1.5 | 6.0 | ns |

AC Operating Requirements

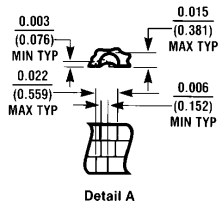
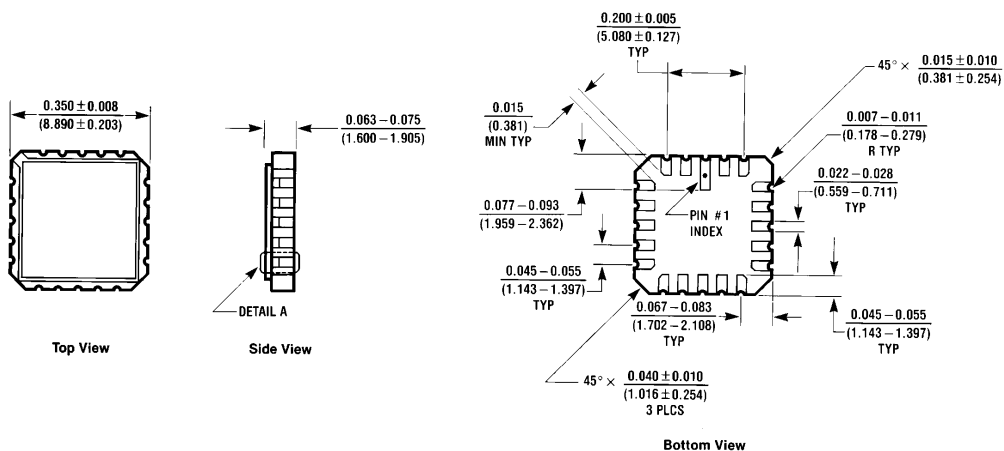
| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|--|---|---|-----|--|-----|--|-----|-------|
| | | T _A = +25°C V _{CC} = +5.0V | | T _A , V _{CC} = Mil | | T _A , V _{CC} = Com | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _s (H) t _s (L) | Setup Time, HIGH or LOW D _n to LE | 2.0 | | 2.0 | | 2.0 | | ns |
| t _h (H) t _h (L) | Hold Time, HIGH or LOW D _n to LE | 3.0 | | 3.0 | | 3.0 | | |
| t _w (H) | LE Pulse Width, HIGH | 6.0 | | 6.0 | | 6.0 | | ns |

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

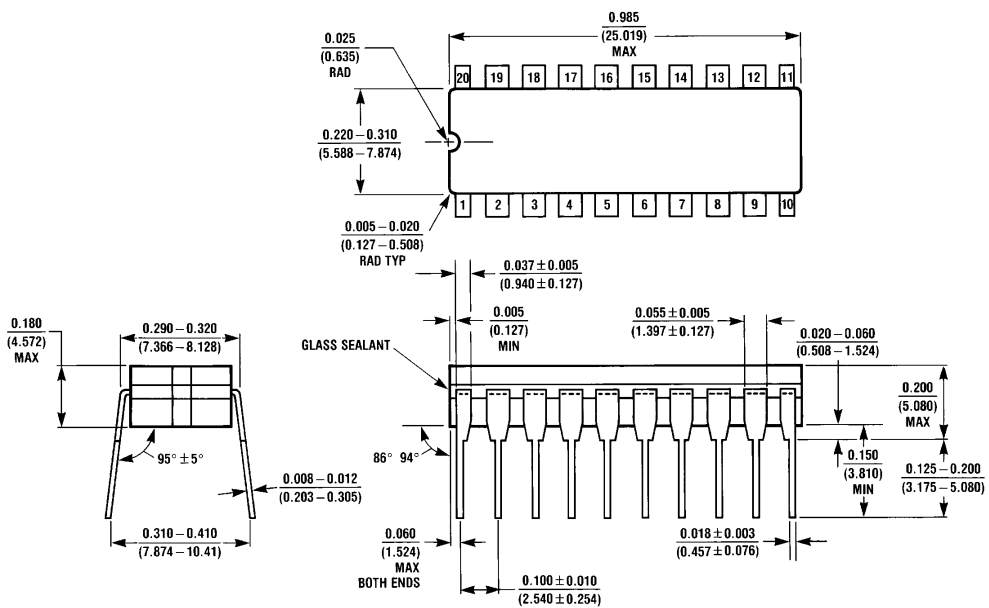


Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A

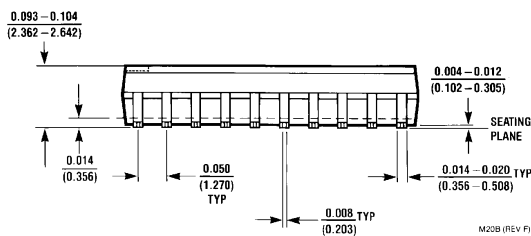
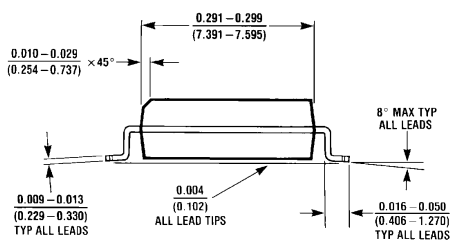
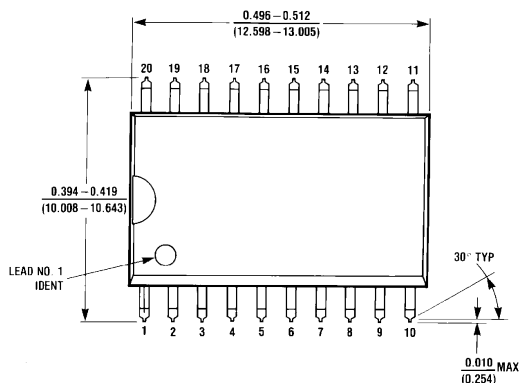
E20A (REV D)



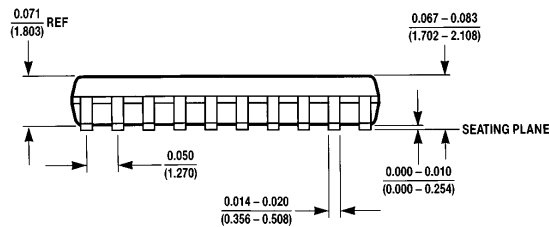
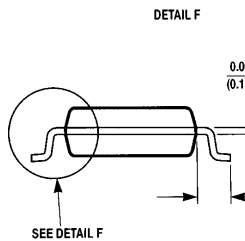
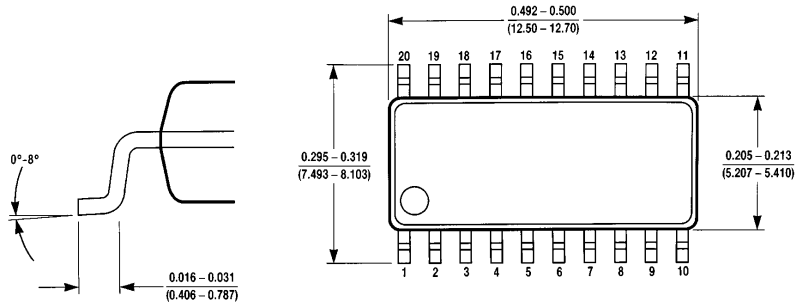
20-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J20A

J20A (REV M)

Physical Dimensions inches (millimeters) (Continued)

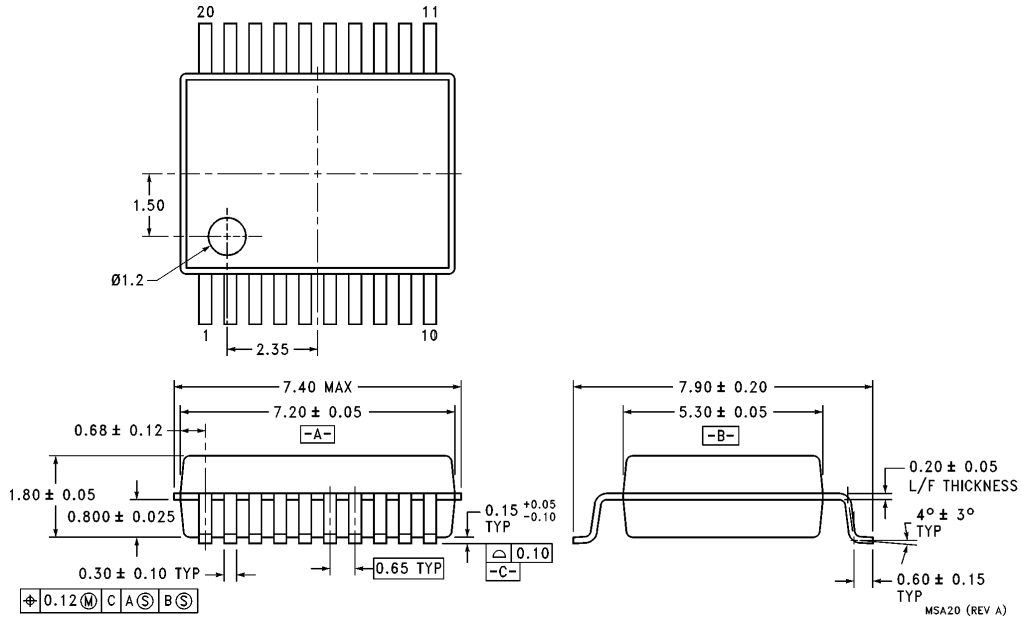


**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B**

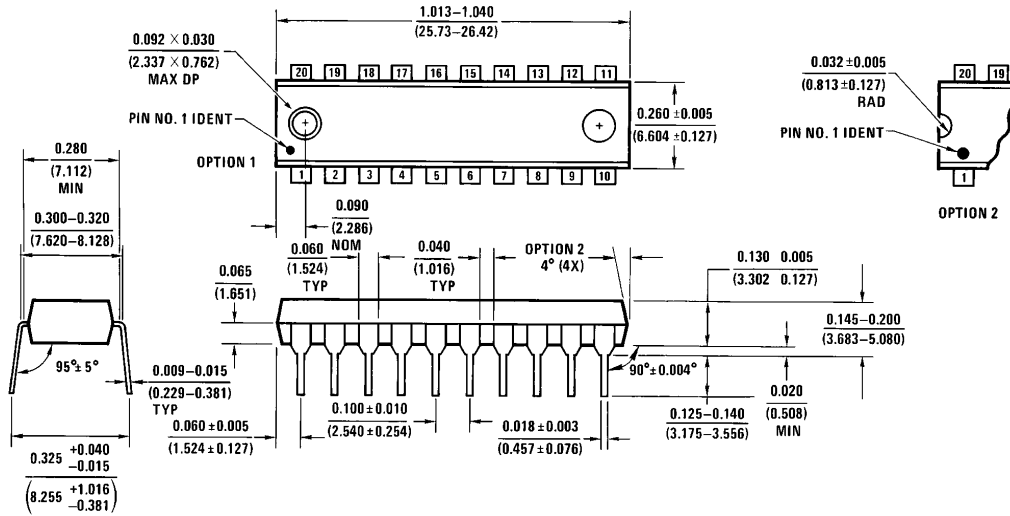


**20-Lead (0.300" Wide) Small Outline Package, EIAJ (SJ)
NS Package Number M20D**

Physical Dimensions inches (millimeters) (Continued)

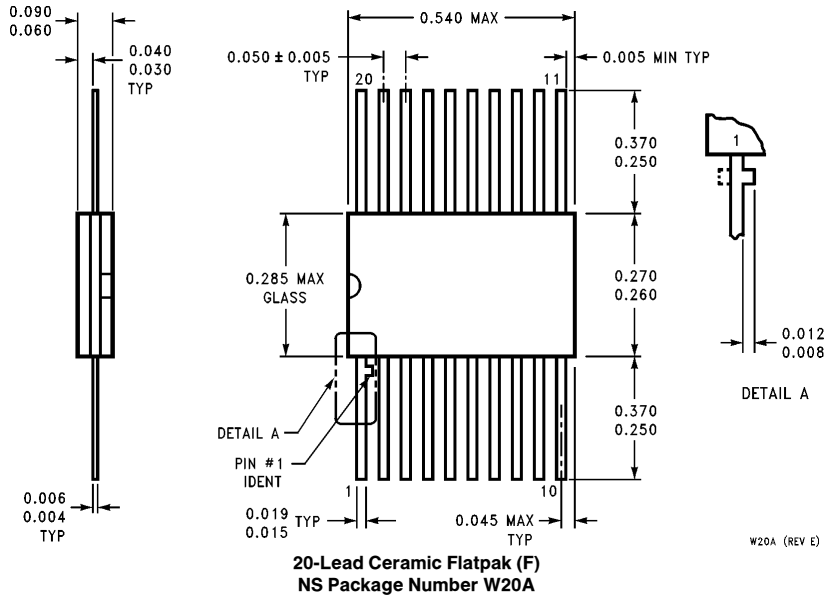


20-Lead Molded Shrink Small Outline Package, EIAJ, Type II (MSA)
NS Package Number MSA20



20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



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