1024 BIT (256 X 4) STATIC MOS RAM WITH SEPARATE I/O

DESCRIPTION

The μPD2101AL is a 256 word by 4 bit static random access memory requiring no clocks or refreshing. It features high speed, low cost, and simplicity of interfacing.

It is directly TTL compatible in all respects; inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system. Output data is the same polarity as input data, and readout is non-destructive.

The μPD2101AL family of devices offers access times from 450 ns to 250 ns with a typical standby mode power dissipation of only 36 mW.

The use of NEC's N-channel silicon gate MOS process, with its excellent protection from contamination, permits the use of a low cost 22 pin plastic package in providing a high performance, high reliability MOS circuit at a most cost effective price level. The μPD2101AL is pin-compatible with the μPD5101 CMOS static RAM.

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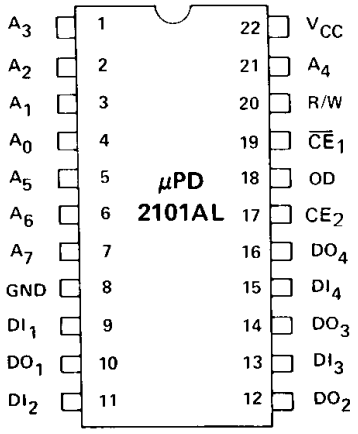
FEATURES

- 256 x 4 Organizations to Meet Needs for Small System Memories
- Access Time – 250 to 450 nsec max
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Chip Enable Input
- Low Standby Power – 36 mW typ.
- Low Cost Packaging – 22 Pin Plastic Dual-In-Line Configuration
- Low Operating Power
- Three-State Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

PIN CONFIGURATION



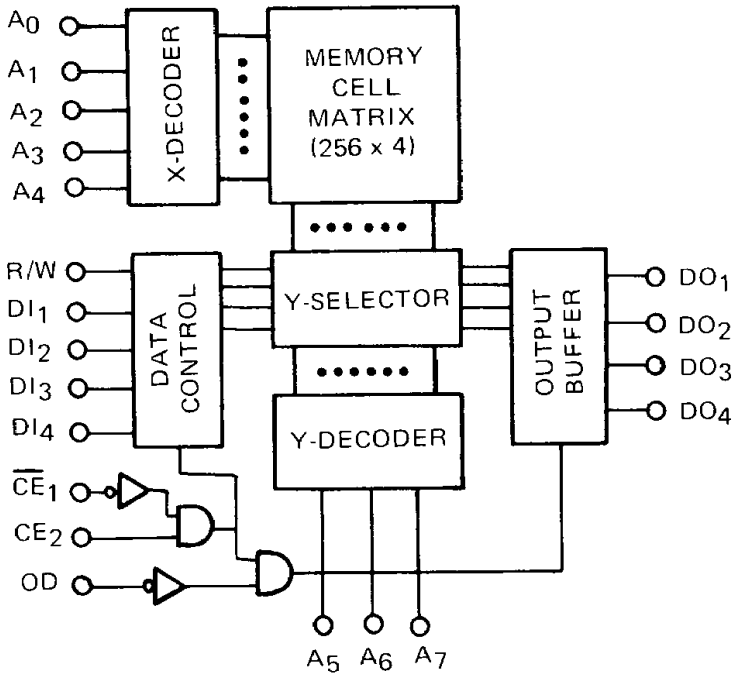
PIN NAMES

DI_1 DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0- A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1 DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

OPERATION MODES

$\overline{CE}_1$	CE_2	OD	CHIP	OUTPUT MODE
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			No Selected	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	V_O = +2.4V to V_{CC} $\overline{CE}_1$ = +2.0V
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}_1$ = +2.0V
Power Supply Current	I_{CC1}			+60	mA	V_I = +5.25V I_O = 0 mA T_a = +25°C
Power Supply Current	I_{CC2}			+70	mA	V_I = +5.25V I_O = 0 mA T_a = −10°C to +70°C

AC CHARACTERISTICS

READ CYCLE

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			180			150			130	ns
Output Disable to Output	t_{OD}			150			130			120	ns
Data Output to High Z State	t_{DF}*	0		130	0		115	0		100	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

*t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.

WRITE CYCLE

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write Cycle Time	t_{WC}	450			350			250			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	180			150			130			ns
Data Setup Time	t_{DW}	180			150			130			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	160			130			120			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			10			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY CHARACTERISTICS

T_a = −10°C to +70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.①	MAX.		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby	V_{CES}	2.0			V	$2.0V \leq V_{PD} \leq 5.25V$
		V_{PD}			V	$1.5V \leq V_{PD} < 2.0V$
Standby Current Drain	I_{PD1}		24	36	mA	All Inputs = V_{PD1} = 1.5V
Standby Current Drain	I_{PD2}		30	45	mA	All Inputs = V_{PD2} = 2.0V
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC}②			ns	

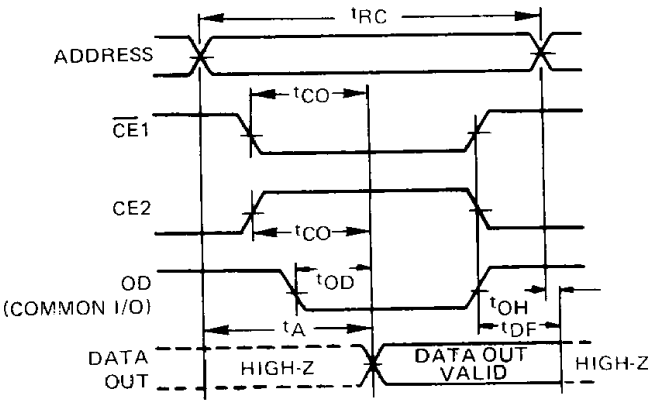
Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.
② $t_R = t_{RC}$ (Read Cycle Time).

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			8	pf	V_I = 0V
Output Capacitance	C_{OUT}			12	pf	V_O = 0V

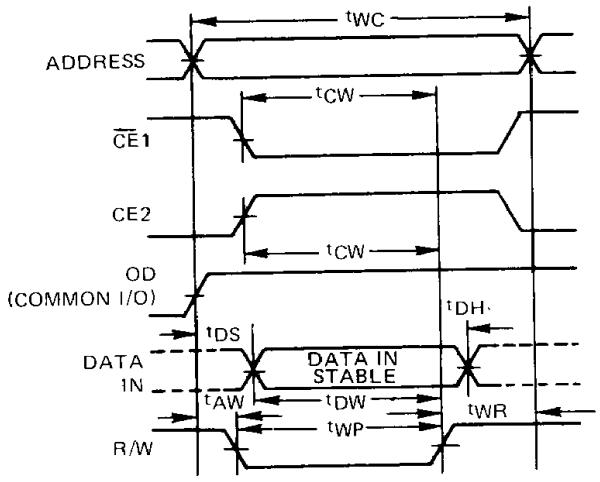
TIMING WAVEFORMS

READ CYCLE



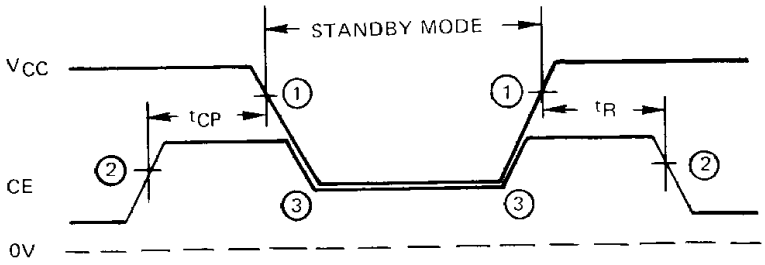
Notes: (1) OD should be tied low for separate I/O operation.
(2) R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



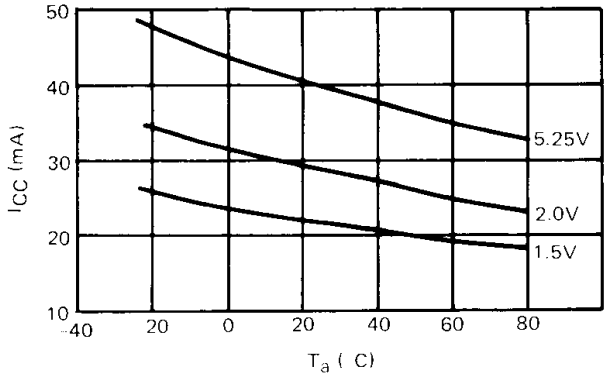
Notes: (1) 4.75V
(2) 2.0V
(3) 1.5V

AC CONDITIONS OF TEST

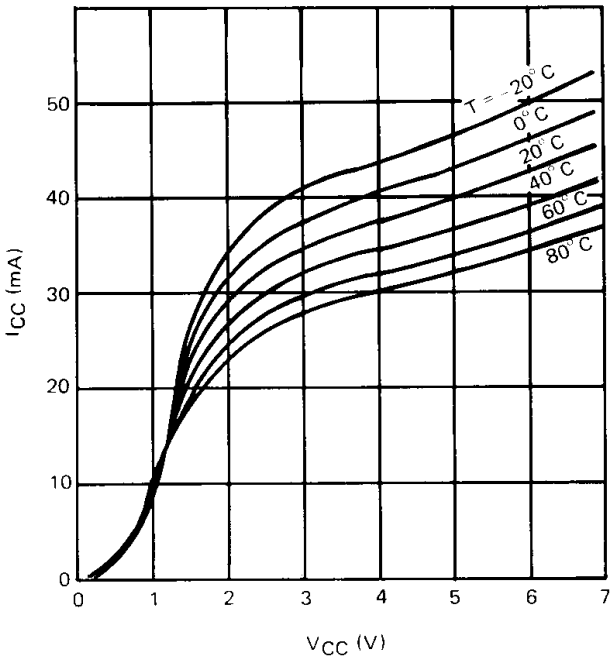
Input Pulse Levels	+0.8V to +2.0V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.5V
Output Load	1 TTL + 100 pF

TYPICAL OPERATING CHARACTERISTICS

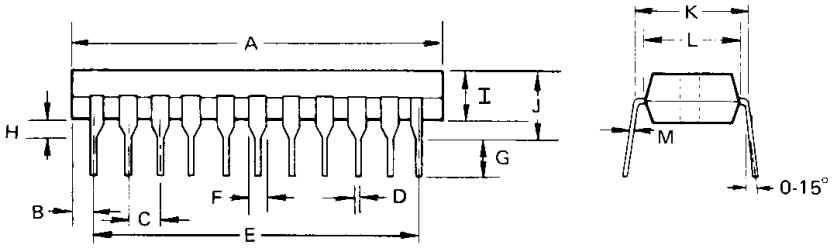
I_{CC} VS T_a



I_{CC} VS V_{CC}



PACKAGE OUTLINE μPD2101ALC



ITEM	MILLIMETERS	INCHES
A	28.0 MAX.	1.10 MAX.
B	1.4 MAX.	0.025
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.7 MAX.	0.18 MAX.
J	5.2 MAX.	0.20 MAX.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$