

# HM6267 Series

## 16384-word x 1-bit High Speed CMOS Static RAM

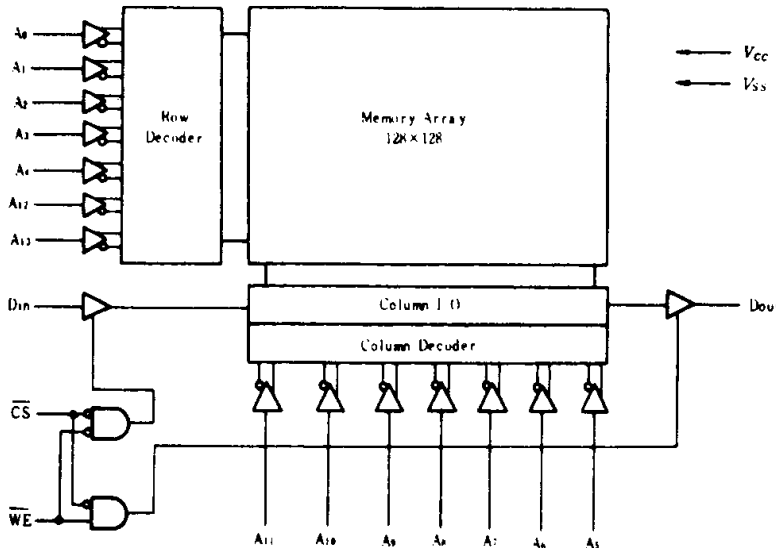
### ■ FEATURES

- High Speed: Fast Access Time 35/45/55ns (max.)
- Low Power Standby and Low Power Operation  
Standby: 0.1mW (typ.)/5 $\mu$ W (typ.) (L-version),  
Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

### ■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plastic DIP
HM6267P-45	45ns	
HM6267P-55	55ns	
HM6267LP-35	35ns	300 mil 20 pin Plastic DIP
HM6267LP-45	45ns	
HM6267LP-55	55ns	

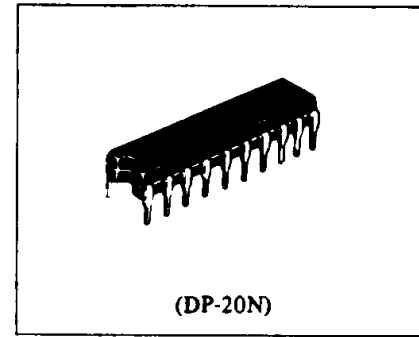
### ■ BLOCK DIAGRAM



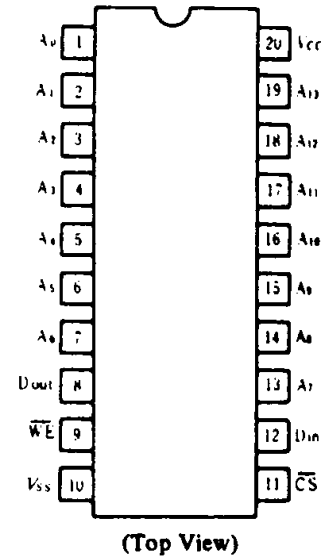
### ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*1	$V_T$	-0.5*2 to +7.0	V
Power Dissipation	$P_T$	1.0	W
Operating Temperature	$T_{opr}$	0 to +70	$^{\circ}$ C
Storage Temperature	$T_{stg}$	-55 to +125	$^{\circ}$ C
Storage Temperature Under Bias	$T_{bias}$	-10 to +85	$^{\circ}$ C

- Notes) \*1. With respect of  $V_{SS}$ .  
\*2. -3.5V for pulse width  $\leq$  20ns.



### ■ PIN ARRANGEMENT



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■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	$V_{CC}$ Current	Dout Pin	Ref. Cycle
H	x	Not selected	$I_{SA}, I_{SB1}$	High-Z	
L	H	Read	$I_{CC}$	Dout	Read Cycle
L	L	Write	$I_{CC}$	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS ( $T_a = 0$  to  $+70^\circ\text{C}$ )

Item	Symbol	min	typ	max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input Voltage	$V_{IH}$	2.2	-	6.0	V
	$V_{IL}$	$-0.5^{*1}$	-	0.8	V

Note) \*1.  $-3.0\text{V}$  for pulse width  $\leq 20\text{ns}$

■ DC AND OPERATING CHARACTERISTICS ( $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ ,  $T_a = 0$  to  $+70^\circ\text{C}$ )

Item	Symbol	Test Conditions	HM6267-35			HM6267-45/55			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}, V_{IN}=V_{SS}$ to $V_{CC}$	-	-	10	-	-	10	$\mu\text{A}$
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}, V_{OUT}=V_{SS}$ to $V_{CC}$	-	-	10	-	-	10	$\mu\text{A}$
Operating Power Supply Current	$I_{CC}$	$\overline{CS}=V_{IL}, I_{OUT}=0\text{mA}$ , min. cycle	-	40	100	-	40	80	$\text{mA}$
Stand by Power Supply Current	$I_{SB}$	$\overline{CS}=V_{IH}$ , min cycle	-	10	20	-	10	20	$\text{mA}$
	$I_{SB1}$	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ , $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN}$	-	0.02	2	-	0.02	2	$\text{mA}$
Output Voltage	$V_{OL}$	$I_{OL} = 8\text{mA}$	-	-	0.4	-	-	0.4	V
	$V_{OH}$	$I_{OH} = -4\text{mA}$	2.4	-	-	2.4	-	-	V

Notes) \*1. Typical limits are at  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$  and specified loading.  
\*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	$C_{IN}$	-	5	pF	$V_{IN} = 0\text{V}$
Output Capacitance	$C_{OUT}$	-	7	pF	$V_{OUT} = 0\text{V}$

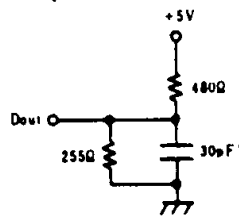
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ( $V_{CC} = 5\text{V} \pm 10\%$ ,  $T_a = 0$  to  $+70^\circ\text{C}$ , unless otherwise noted)

● AC TEST CONDITIONS

Input pulse levels:  $V_{SS}$  to  $3.0\text{V}$   
 Input rise and fall times:  $5\text{ns}$   
 Input and Output timing reference levels:  $1.5\text{V}$   
 Output load: See Figure

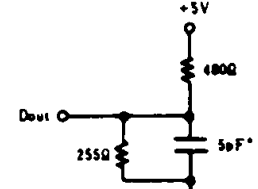
Output Load A



\* Including scope and jig.

Output Load B

(for  $t_{rz}$ ,  $t_{Lz}$ ,  $t_{wz}$  &  $t_{ow}$ )



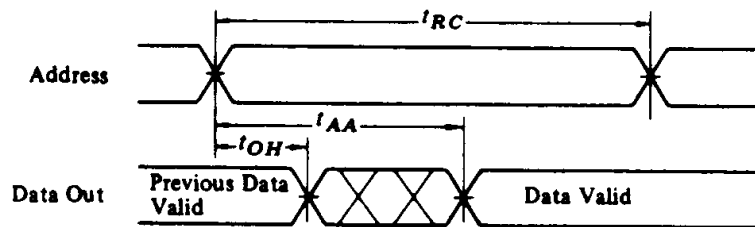
\* Including scope and jig.



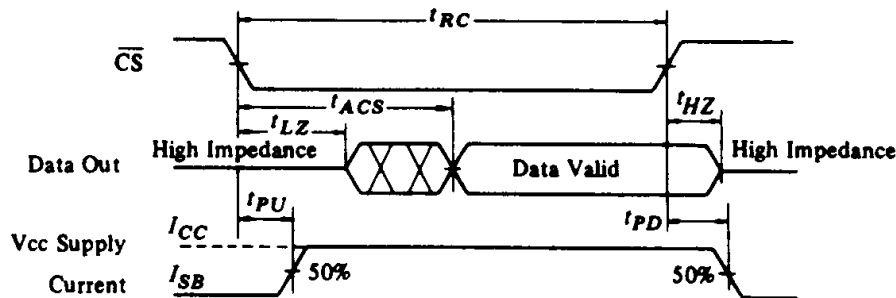
● Read Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	$t_{RC}$	35	-	45	-	55	-	ns	1
Address Access Time	$t_{AA}$	-	35	-	45	-	55	ns	
Chip Select Access Time	$t_{ACS}$	-	35	-	45	-	55	ns	
Output Hold from Address Change	$t_{OH}$	5	-	5	-	5	-	ns	
Chip Selection to Output in Low Z	$t_{LZ}$	5	-	5	-	5	-	ns	2,3,7
Chip Deselectio to Output in High Z	$t_{HZ}$	0	30	0	30	0	30	ns	2,3,7
Chip Selectio to Power Up Time	$t_{PU}$	0	-	0	-	0	-	ns	
Chip Deselection to Power Down Time	$t_{PD}$	-	20	-	30	-	30	ns	

● TIMING WAVEFORM OF READ CYCLE NO. 1 <sup>4) 5)</sup>



● TIMING WAVEFORM OF READ CYCLE NO. 2 <sup>4) 6)</sup>



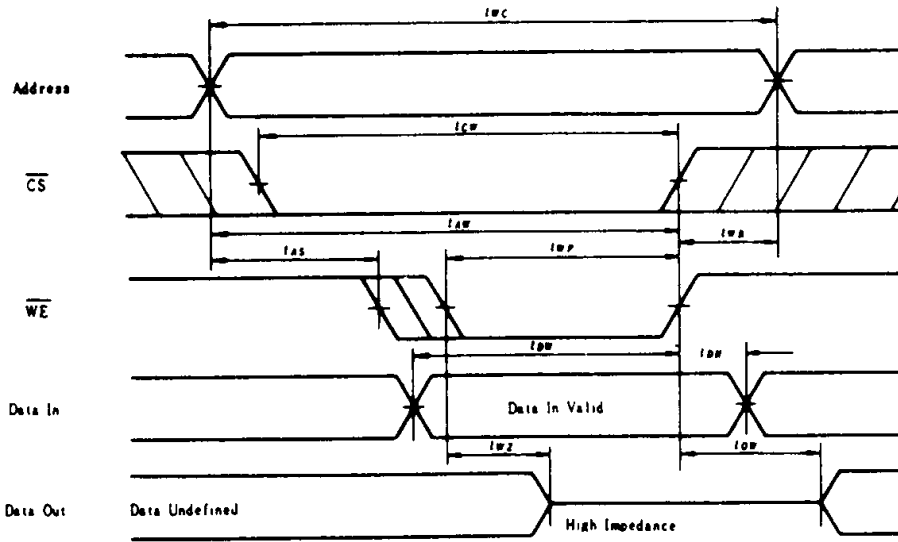
- Notes)
1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
  2. At any given temperature and voltage condition,  $t_{HZ}$  max. is less than  $t_{LZ}$  min. both for a given device and from device to device.
  3. Transition is measured  $\pm 500$ mV from steady state voltage with specified loading in Load B.
  4. WE is High for READ cycle.
  5. Device is continuously selected,  $\overline{CS} = V_{IL}$ .
  6. Addresses valid prior to or coincident with  $\overline{CS}$  transition low.
  7. This parameter is sampled and not 100% tested.

● Write Cycle

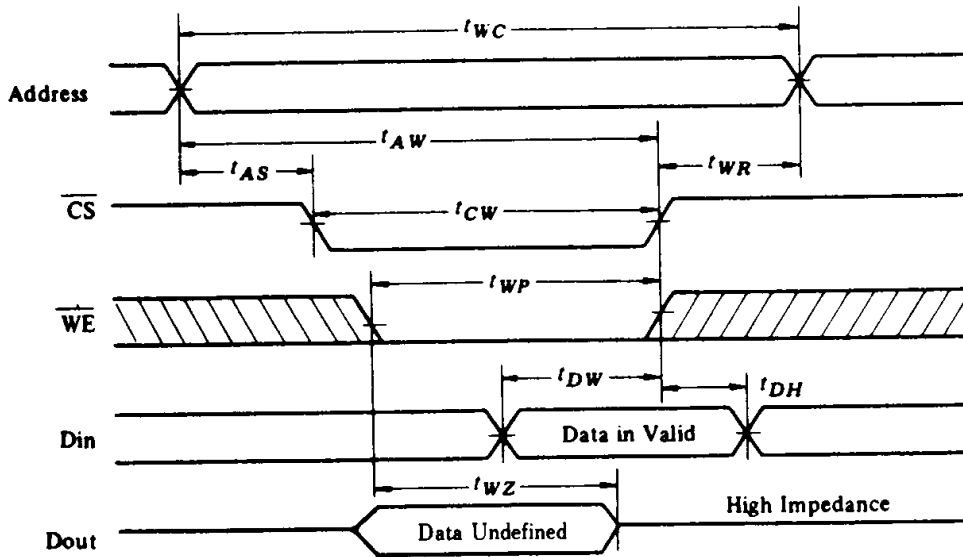
Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	$t_{WC}$	35	-	45	-	55	-	ns	2
Chip Selection to End of Write	$t_{CW}$	30	-	40	-	50	-	ns	
Address Valid to End of Write	$t_{AW}$	30	-	40	-	50	-	ns	
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	ns	
Write Pulse Width	$t_{WP}$	20	-	25	-	35	-	ns	
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	ns	
Data Valid to End of Write	$t_{DW}$	20	-	25	-	25	-	ns	
Data Hold Time	$t_{DH}$	0	-	0	-	0	-	ns	
Write Enabled to Output in High Z	$t_{WZ}$	0	20	0	25	0	25	ns	3,4
Output Active from End of Write	$t_{OW}$	0	-	0	-	0	-	ns	3,4



● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  Controlled)



- Notes) 1. If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance states.  
 2. All Write Cycle timings are referenced from the last valid address to the first transitions address.  
 3. Transition is measured  $\pm 500mV$  from steady state voltage with specified loading in Load B.  
 4. This parameter is sampled and not 100% tested.

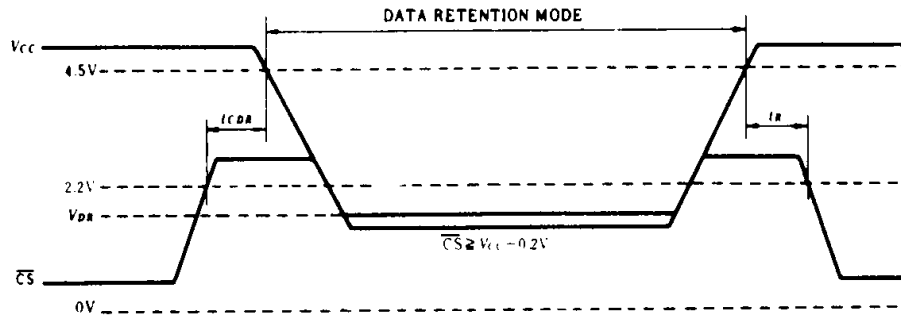
**LOW V<sub>CC</sub> DATA RETENTION CHARACTERISTICS (0°C ≤ T<sub>a</sub> ≤ 70°C)**

This characteristics is guaranteed only for L-version.

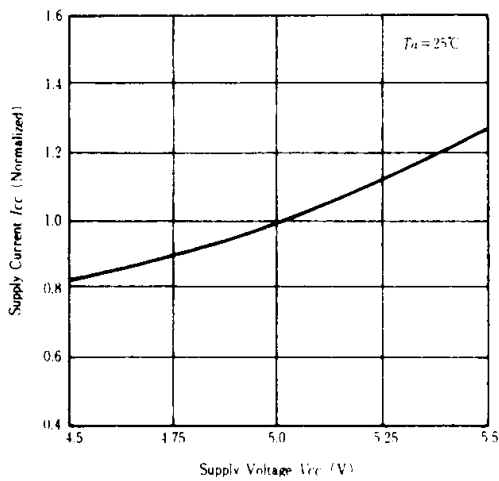
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I <sub>CCDR</sub>	$V_{i1} \geq V_{CC} - 0.2V$ or $0V \leq V_{i1} \leq 0.2V$	—	—	30 <sup>+2</sup> 20 <sup>+3</sup>	μA
Chip Deselect to Data Retention Time	t <sub>CDR</sub>	see retention waveform	0	—	—	ns
Operation Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *1	—	—	ns

Notes) \*1. t<sub>RC</sub> = Read Cycle Time.      \*2. V<sub>CC</sub> = 3.0V  
 \*3. V<sub>CC</sub> = 2.0V

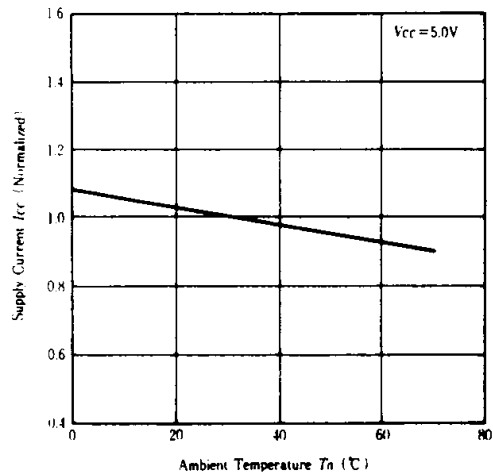
**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM**



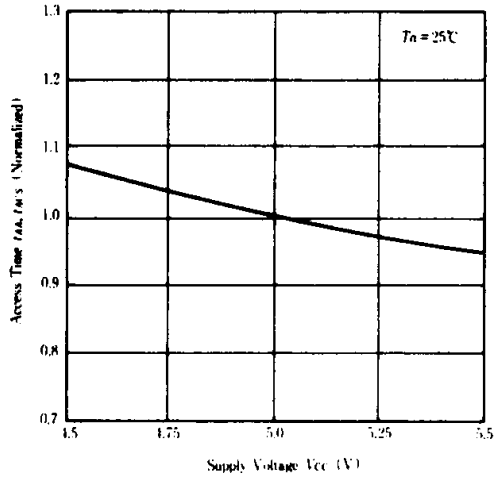
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**



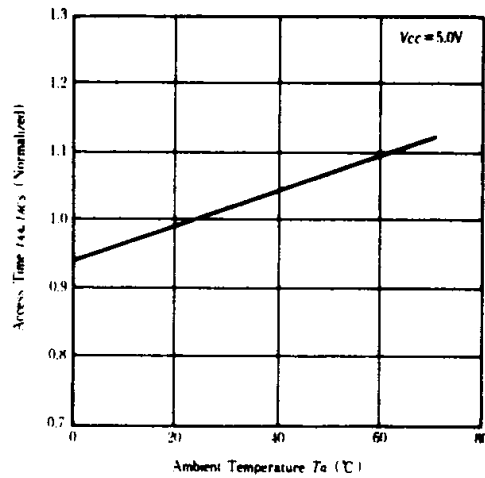
**SUPPLY CURRENT VS. AMBIENT TEMPERATURE**



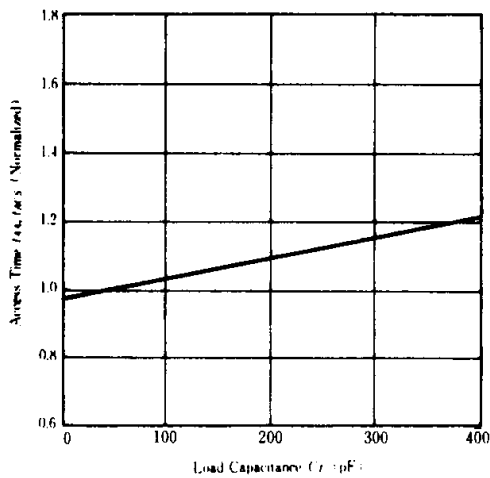
ACCESS TIME VS. SUPPLY VOLTAGE



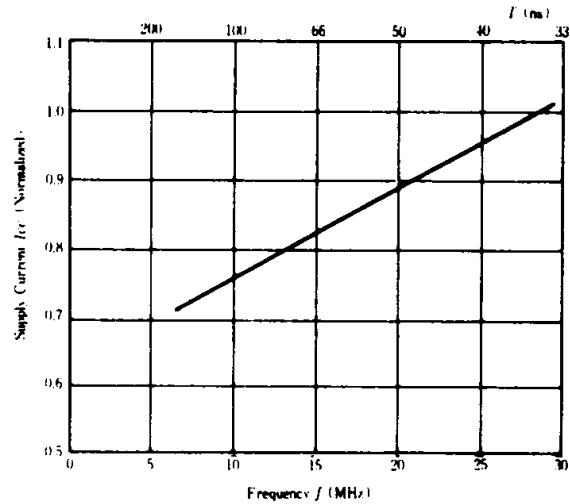
ACCESS TIME VS. AMBIENT TEMPERATURE



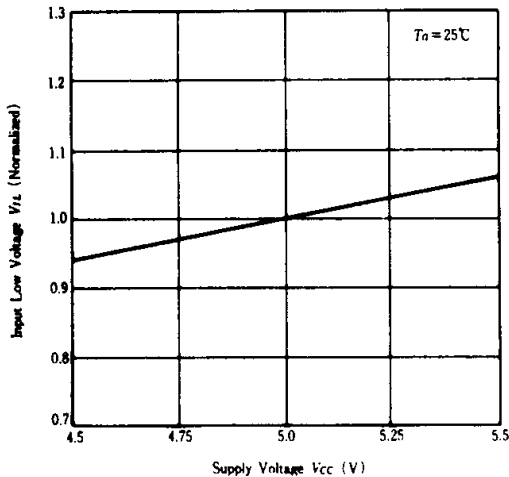
ACCESS TIME VS. LOAD CAPACITANCE



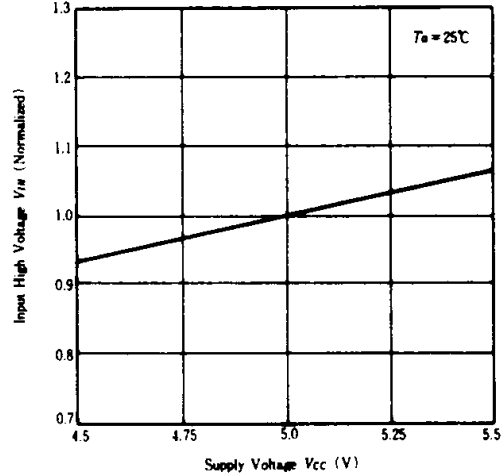
SUPPLY CURRENT VS. FREQUENCY



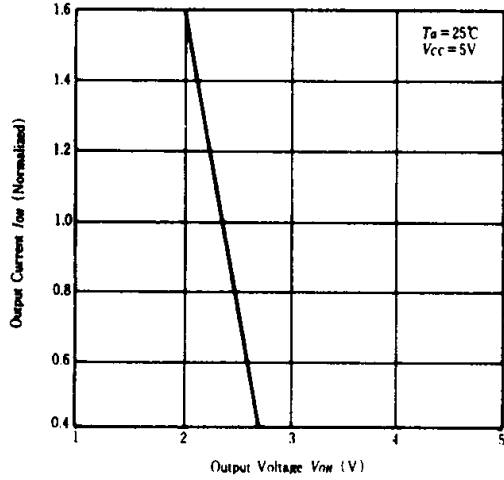
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



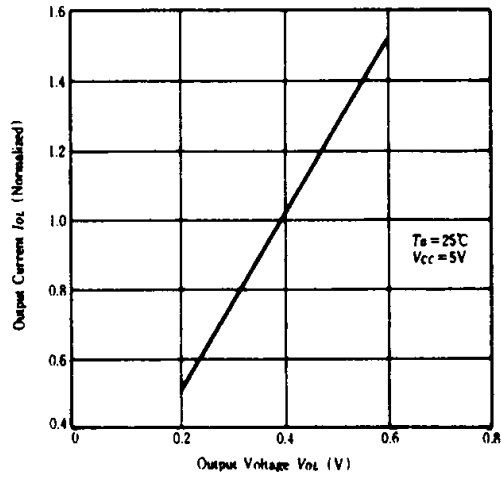
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



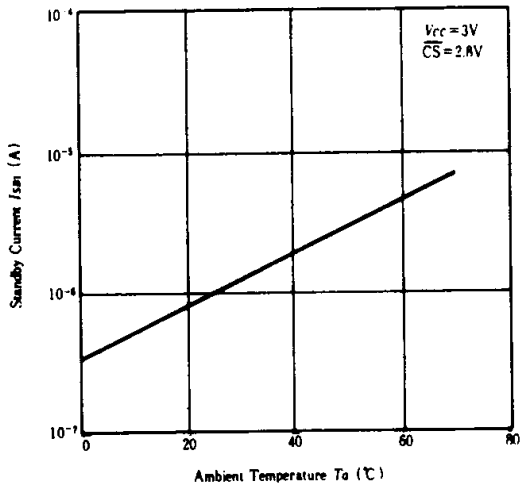
**OUTPUT CURRENT VS. OUTPUT VOLTAGE**



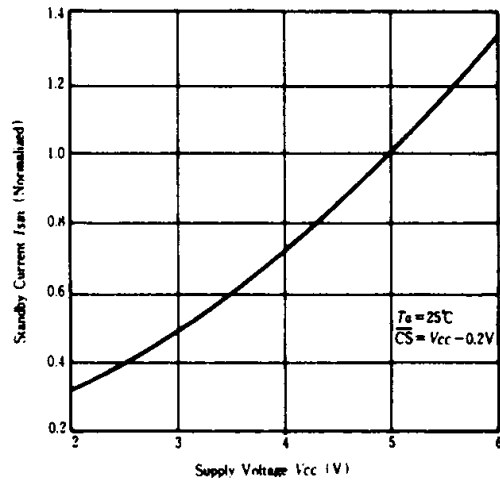
**OUTPUT CURRENT VS. OUTPUT VOLTAGE**



**STANDBY CURRENT VS. AMBIENT TEMPERATURE**



**STANDBY CURRENT VS. SUPPLY VOLTAGE**



2

