1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58657P is a serial input/output 1400 bit electrically erasable and reprogrammable ROM organized as 100 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . 10 years (min)
- Write/erase time . . . . 20ms word
- Typical power supply voltages . . . . -30V, +5V
- Number of erase-write cycles . . . . 10^5 times (min)
- Number of read access unrefreshed. . .10^9 times (min)
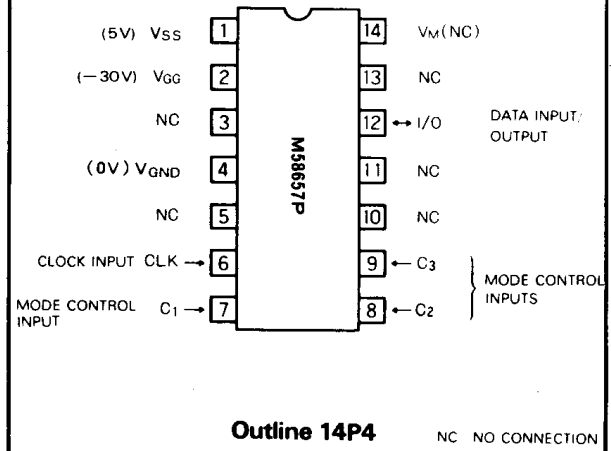- 5V I/O interface

APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems
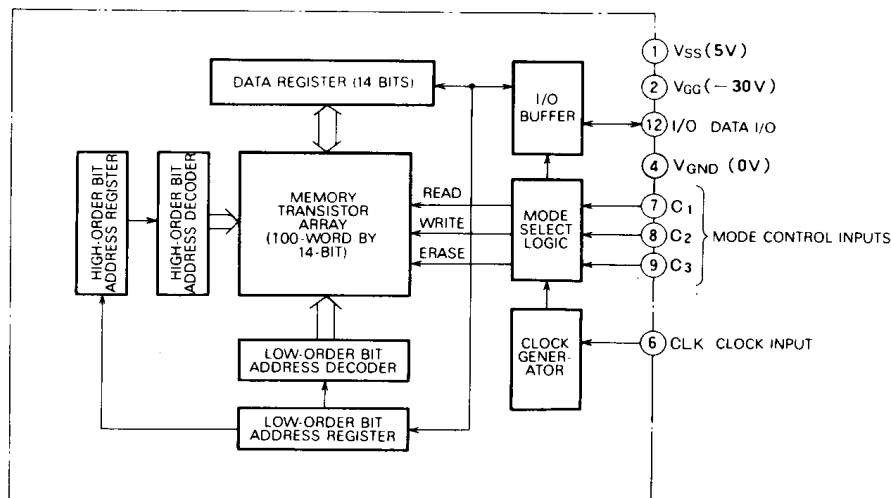
FUNCTION

The address is designated by two consecutive one-of-ten-coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2–Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

PIN CONFIGURATION (TOP VIEW)

(5V) V_{SS}	1	14 V_M(NC)
(−30V) V_{GG}	2	13 NC
NC	3	12 ↔ I/O DATA INPUT/OUTPUT
(0V) V_{GND}	4	11 NC
NC	5	10 NC
CLOCK INPUT CLK →	6	9 ← C_3 MODE CONTROL INPUTS
MODE CONTROL INPUT C_1 →	7	8 ← C_2

M58657P

Outline 14P4   NC   NO CONNECTION

BLOCK DIAGRAM

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PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state.
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation
V_{SS}	Chip substrate voltage	Normally connected to +5V
V_{GG}	Power supply voltage	Normally connected to −30V
CLK	Clock input	14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode
$C_1 \sim C_3$	Mode control input	Used to select the operation mode
V_{GND}	Ground voltage	Connected to ground (0V)

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode. The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Not used.
H	L	H	Erase mode. The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode. Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-ten-coded digits
L	H	H	Read mode. The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode. The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse
L	L	H	Write mode. The data contained in the data register is written into the location designated by the address registers
L	L	L	Accept data mode. The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	$0.3 \sim -40$	V
V_I	Input voltage		$0.3 \sim -20$	V
V_O	Output voltage		$0.3 \sim -20$	V
T_{stg}	Storage temperature		$-40 \sim 125$	℃
T_{opr}	Operating temperature		$-10 \sim 70$	℃

RECOMMENDED OPERATING CONDITIONS (Ta $= -10 \sim 70$℃. unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{GG}-V_{SS}$	Supply voltage	-32.2	-35	-37.8	V
$V_{SS}-V_{GND}$	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-6.5$		$V_{SS}-4.25$	V

Note 1:
The order of V_{SS} V_{GG} with on or off.
With on, V_{GG} is turned on after V_{SS} is done.
With off, V_{SS} is turned off after V_{GG} is done.

ELECTRICAL CHARACTERISTICS (Ta $= -10 \sim 70$℃. $V_{GG}-V_{SS} = -35V \pm 8$ %, $V_{SS}-V_{GND} = 5V \, {}^{+20\%}_{-5\%}$. unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		$V_{SS}-6.5$		$V_{SS}-4.25$	V
I_{IL}	Low-level input current	$V_I - V_{SS} = -6.5V$			± 10	μA
I_{OZL}	Off-state output current, low-level voltage applied	$V_O - V_{SS} = -6.5V$			± 10	μA
V_{OH}	High-level output voltage	$I_{OH} = -200\mu A$	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	$I_{OL} = 10\mu A$			$V_{GND}+0.5$	V
I_{GG}	Supply current from V_{GG}	$I_O = 0\mu A$		5.5	8.8	mA

Note 2: Typical values are at Ta$=25$°C and nominal supply voltage.

TIMING REQUIREMENTS (Ta $= -10 \sim 70$℃. $V_{GG}-V_{SS} = -35V \pm 8$ %, $V_{SS}-V_{GND} = 5V \, {}^{+20\%}_{-5\%}$. unless otherwise noted)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
$f(\phi)$	Clock frequency	$f\phi$		10	14	17	kHz
$D(\phi)$	Clock duty cycle	$D\phi$		30	50	55	%
$t_{w(W)}$	Write time	t_w		16	20	24	ms
$t_{w(E)}$	Erase time	t_e		16	20	24	ms
t_r, t_f	Risetime. fall time	t_r, t_f				1	μs
$t_{su(c-\phi)}$	Control setup time before the fall of the clock pulse	t_{CS}		0			ns
$t_{h(\phi-c)}$	Control hold time after the rise of the clock pulse	t_{CH}		0			ns

SWITCHING CHARACTERISTICS (Ta $= -10 \sim 70$℃. $V_{GG} = -35V \pm 8$ %. unless otherwise noted)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(c)}$	Read access time	t_{PW}	$C_L = 100pF$ $V_{OH} = V_{SS}-2V$ $V_{OL} = V_{GND}+1.5V$			20	μs
t_s	Unpowered nonvolatile data retention time	T_S	$N_{EW} = 10^4$. $t_{w(W)} = 20ms$ $t_{w(E)} = 20ms$	10			Year
		T_S	$N_{EW} = 10^5$ $t_{w(W)} = 20ms$ $t_{w(E)} = 20ms$	1			
N_{EW}	Number of erase/write cycles	N_w		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^9			Times
t_{dv}	Data valid time	t_{PW}				20	μs

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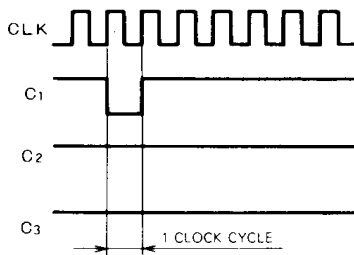## 1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM
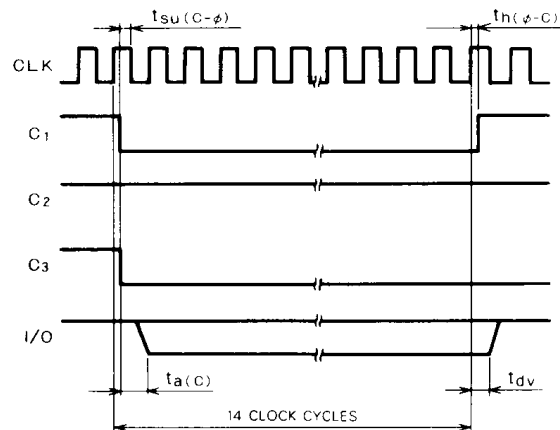
TIMING DIAGRAM
Accept Data Mode
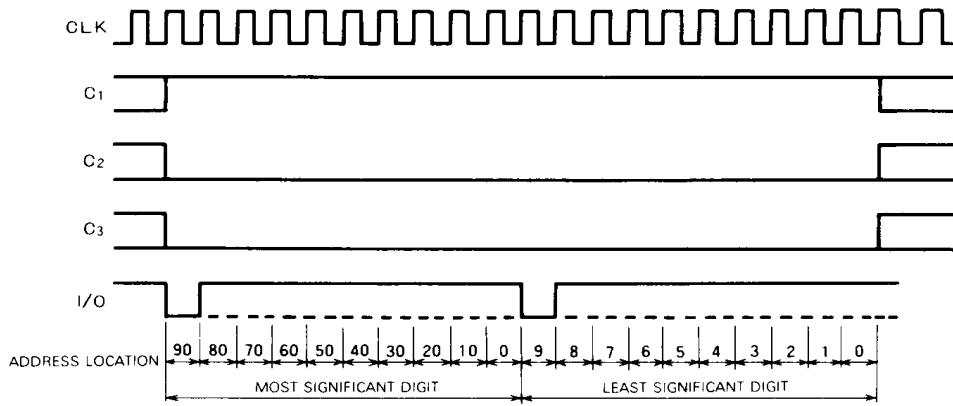
Note 3: The address is designated by two one-of-ten-coded digits. The figure shows designation of the address 99.
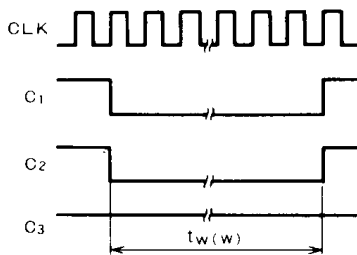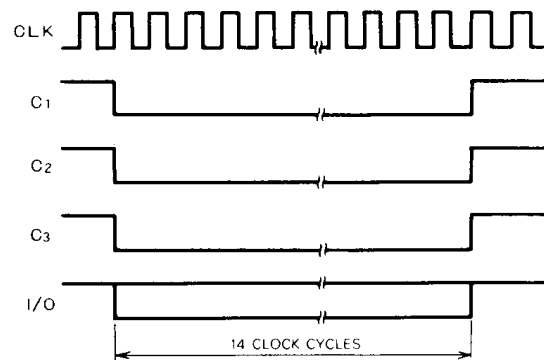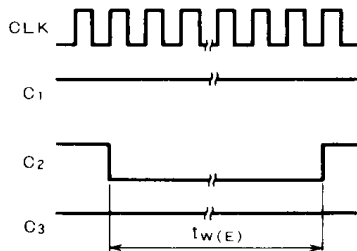
Read Mode

Write Mode

Erase Mode

Shift Data Output Mode

Accept Data Mode

12—28

The difinition of clock duty cycle, D (φ)

$$D_{(\phi)} = T_{(L)} / T_{(\phi)}$$
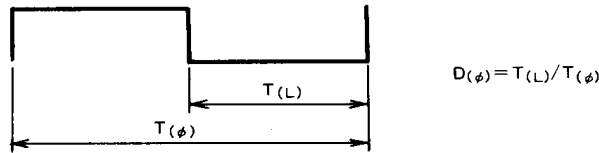
Timing of data input and mode control inputs

Mode control inputs, C_1, C_2, C_3 and input signal my change, when clock is 'H' level.
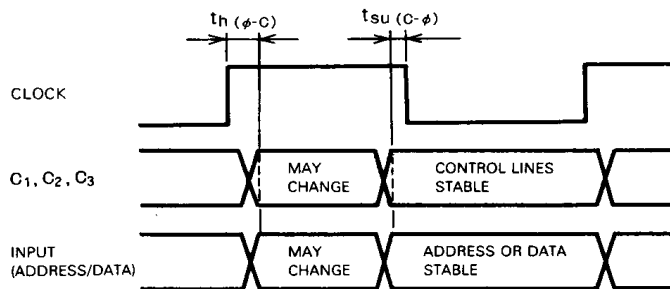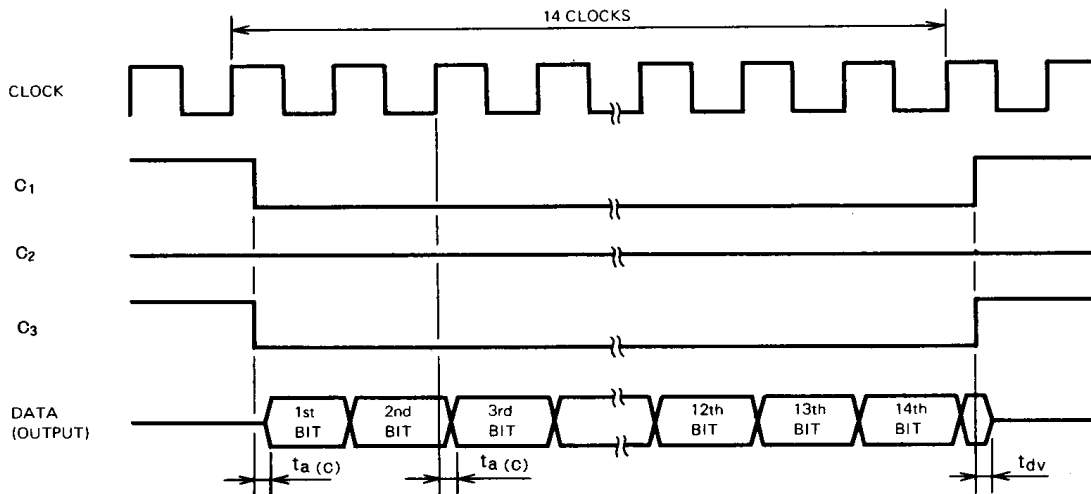

Timing of data output

The 1st bit of output data is output after access time of $t_{a(C)}$ from the mode control transition. And other bits are output after $t_{a(C)}$ from positive edge of clock.

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Operating sequential flow

(a) Read Sequence

| STANDBY MODE (WITH CLOCK) |
| ACCEPT ADDRESS MODE (20 CLOCKS) |
| STANDBY MODE (WITH CLOCK) |
| READ MODE (1 CLOCK) |
| STANDBY MODE (WITH CLOCK) |
| SHIFT DATA OUT MODE (14 CLOCKS) |
| STANDBY MODE (WITH CLOCK) |

(b) Erase/write Sequence

| STANDBY MODE (WITH CLOCK) |
| ACCEPT ADDRESS MODE (20 CLOCKS) |
| STANDBY MODE (WITH CLOCK) |
| ERASE MODE ($t_{w(E)}$) |
| STANDBY MODE (WITH CLOCK) |
| ACCEPT DATA MODE (14 CLOCKS) |
| STANDBY MODE (WITH CLOCK) |
| WRITE MODE ($t_{w(w)}$) |
| STANDBY MODE (WITH CLOCK) |

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