M56620AP

Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER

DESCRIPTION

The M56620AP is a semiconductor integrated circuit fabricated using Bi-CMOS technology. It contains bipolar 8 output drivers of CMOS latch.

FEATURES

- Enable input for output control
- Low supply current .....$I_{CC} \leq 10\mu A$ at standby
- Input level is compatible with standard CMOS
- Driver: Withstand voltage .....$BV_{CEO} \geq 50V$
  Large drive current ..... ($I_{O(max)}$=500mA)
- Wide operating temperature range ..... Ta=-20 – +75°C

APPLICATION

Thermal printer head dot driver, Relay driver, Solenoid driver

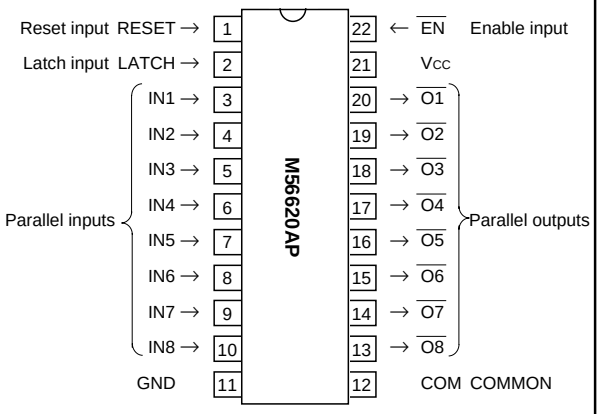
FUNCTION

When data is applied to inputs IN1 – IN8 and LATCH input is set to "H", the data will be latchedance with the truth table. Note that when an "H" signal is applied to the RESET input, the latch will maintain the reset state.

When the $\overline{EN}$ input is set to "L" and the data maintained in the latch are "H", the corresponding output will be ON and become "L".

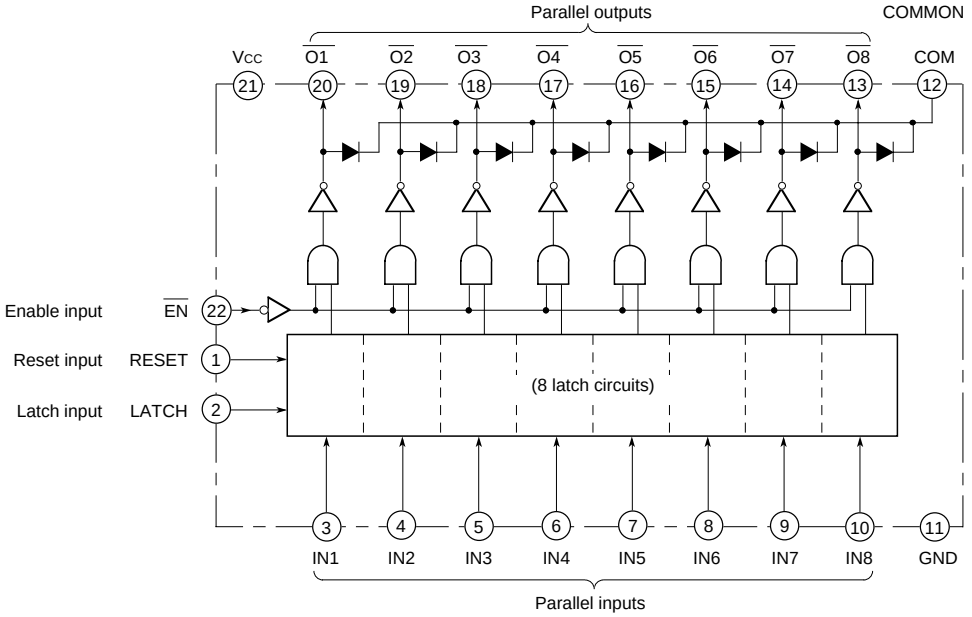
When both the LATCH and RESET inputs are "L", the latch will maintain the prior state irrespective of input signals IN1 – IN8.

PIN CONFIGURATION (TOP VIEW)



Outline 22P4

BLOCK DIAGRAM

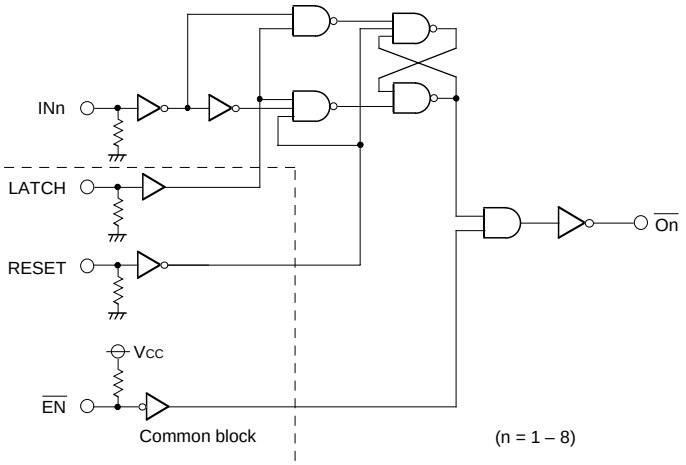


TRUTH TABLE

Input				Output $\overline{On}$	
INn	LATCH	RESET	$\overline{EN}$	t-1	t
L	H	L	L	x	H
H	H	L	L	x	L
x	x	H	x	x	H
x	x	x	H	x	H
x	L	L	L	L	L
x	L	L	L	H	H

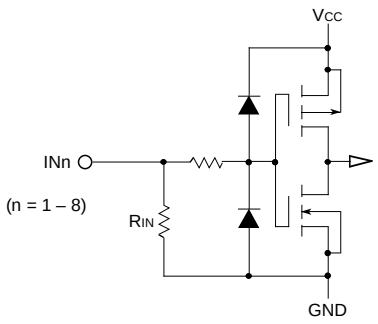
L: low level
H: high level
x: low level or high level
t-1: previous state
t: current state
H output: OFF state
L output: ON state

LOGIC DIAGRAM (One circuit)

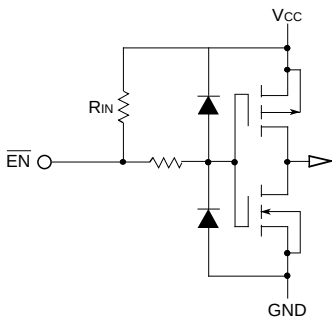


INPUT/OUTPUT EQUIVALENT CIRCUITS

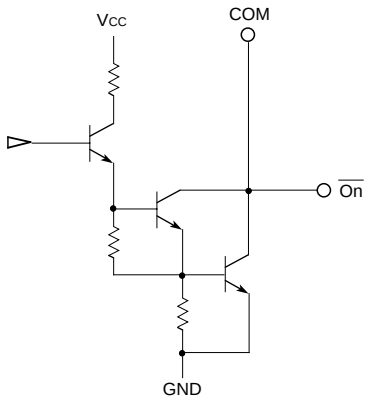
1 Input circuits
(INn, LATCH, RESET)



2 Input circuit ($\overline{EN}$)



3 Output circuits
($\overline{O1}$ – $\overline{O8}$)



ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3 – +8	V
V_I	Input voltage		-0.3 – V_{CC}+0.3	V
V_O	Output voltage	Output: OFF	0 – +50	V
I_O	Output current	Output: ON	500	mA
P_d	Power dissipation	Ta=25°C	1.25	W
T_{opr}	Operating temperature		-20 – 75	°C
T_{stg}	Storage temperature		-55 – 125	°C

RECOMMENDED OPERATING CONDITION (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4	5	6	V
V_O	Output apply voltage	Output: OFF			50	V
I_O	Output current (per circuit)	All outputs go in ON state simultaneously. Duty cycle < 15%			350	mA

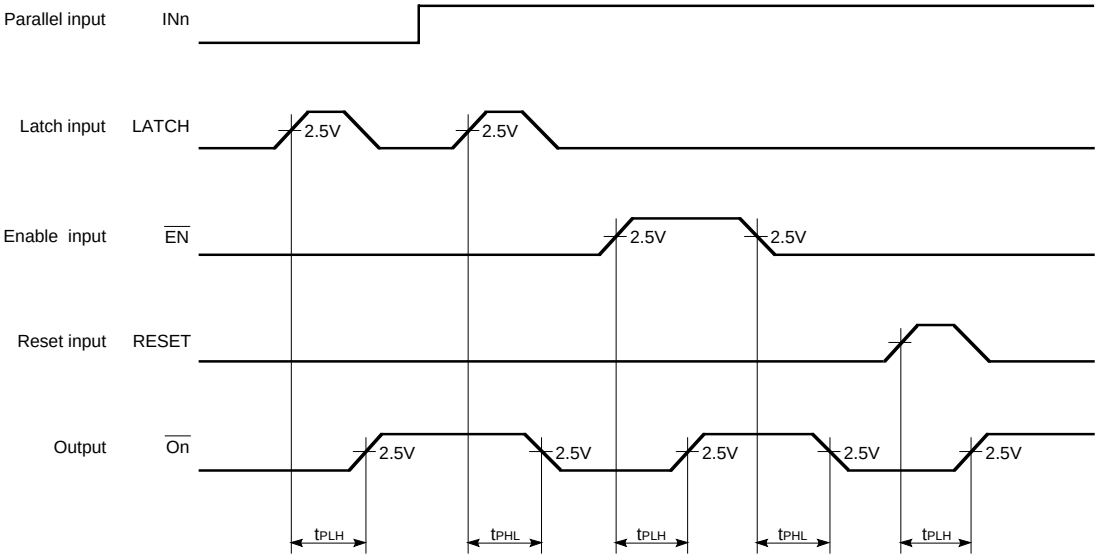
ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	High-level input voltage	Ta=-20 – 75°C	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.3V_{CC}	V
R_{IN}	Input resistance	V_{IN}=1.5 – 3.5V	50		2000	kΩ
V_{OL1}	Low-level output voltage	I_{OL}=100mA			1.1	V
V_{OL2}		I_{OL}=200mA			1.3	V
V_{OL3}		I_{OL}=350mA			1.6	V
I_{OLK}	Output leak current	V_O=50V			50	µA
V_F	Clamping diode forward voltage	I_F=350V			2	V
I_R	Clamping diode reverse current	V_R=50V			50	µA
I_{CC1}	Supply current	$\overline{EN}$=5V, All other inputs = 0V			10	µA
I_{CC2}		$\overline{EN}$=0V, One output is ON.		1.0	1.5	mA

SWITCHING CHARACTERISTICS (Ta=25°C, Vcc=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{PLH}	Low-to-high-level output propagation time From input LATCH to output $\overline{On}$	V_{IH}=5V V_{IL}=0V R_L=100Ω C_L=15pF			5	µs
t_{PHL}	High-to-low-level output propagation time From input LATCH to output $\overline{On}$				0.5	µs
t_{PLH}	Low-to-high-level output propagation time From input $\overline{EN}$ to output $\overline{On}$				5	µs
t_{PHL}	High-to-low-level output propagation time From input $\overline{EN}$ to output $\overline{On}$				0.5	µs
t_{PLH}	Low-to-high-level output propagation time From input RESET to output $\overline{On}$				5	µs

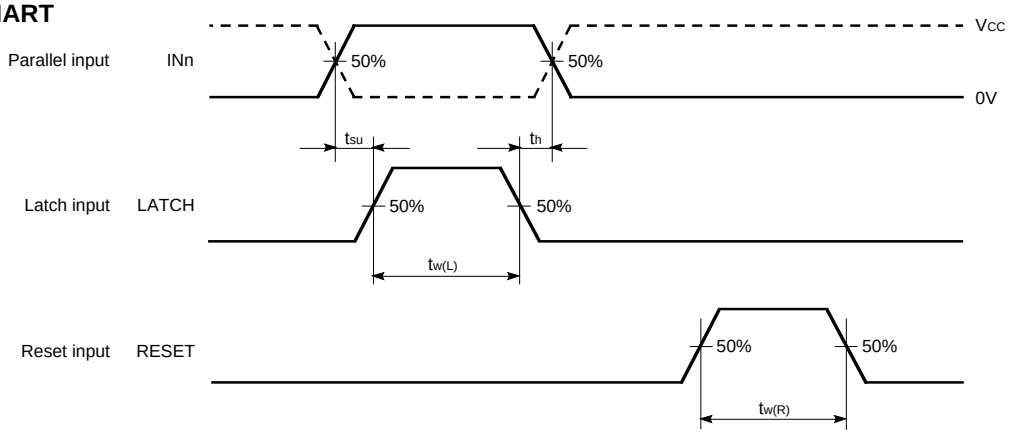
TIMING CHART



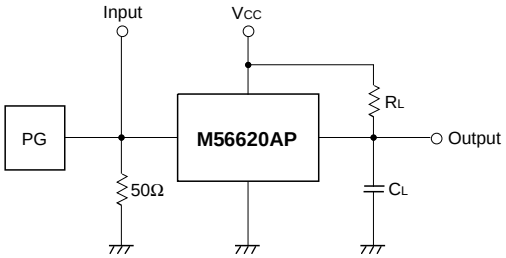
TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{w(L)}$	Latch pulse width		0.1			µs
$t_{w(R)}$	Reset pulse width		0.1			µs
t_{su}	Data setup time		0.05			µs
t_h	Data hold time		0.1			µs

TIMING CHART



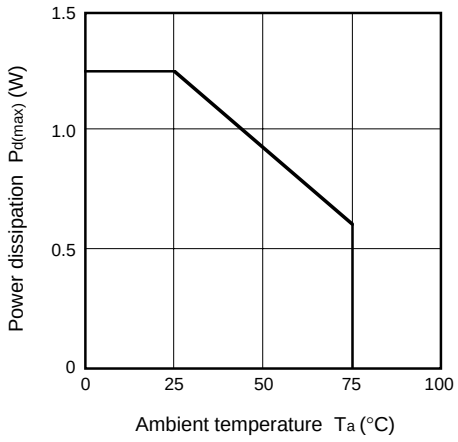
TEST CIRCUIT



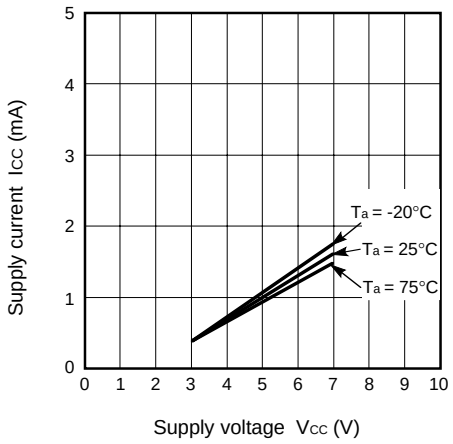
- The input waveform: $t_r \leq 20ns$, $t_f \leq 20ns$
- The capacitance C_L includes the wiring stray capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

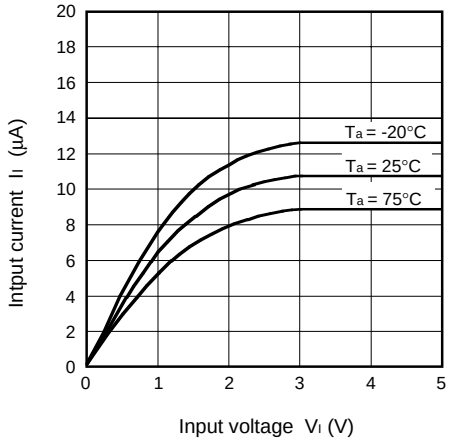
Thermal derating
(Absolute maximum rating)



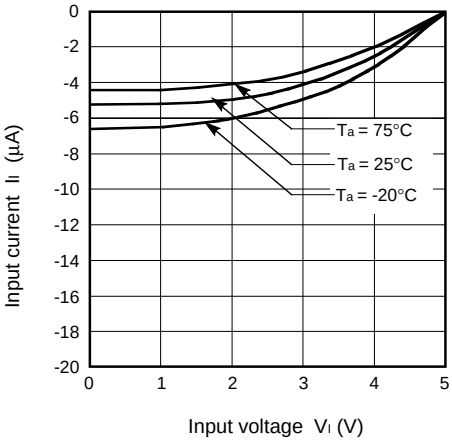
Supply voltage vs. supply current
(one circuit : ON)



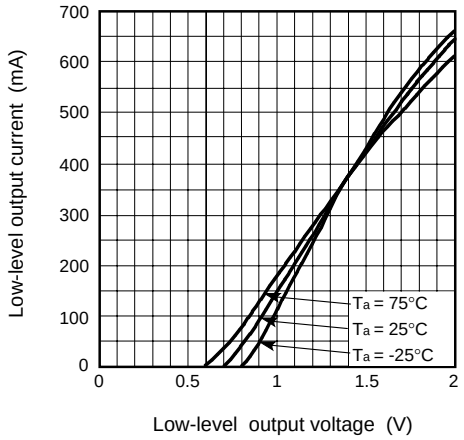
Input voltage vs. input current
(INn, LATCH and RESET)



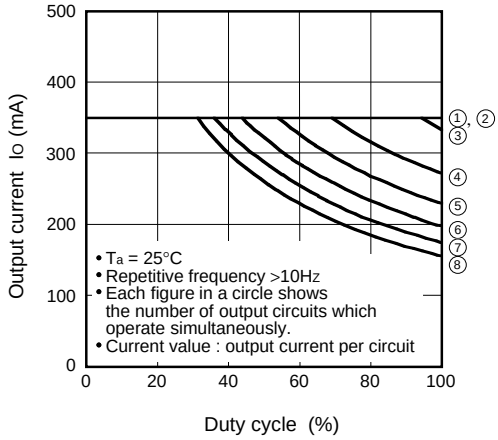
Input voltage vs. input current ($\overline{EN}$)



Low-level output voltage vs. current



Duty cycle vs. allowable output current



Duty cycle vs. allowable output current