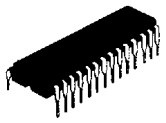
LC7522



3029A

SANYO SEMICONDUCTOR CORP

CMOS LSI

Electronic Volume Control for Graphic Equalizer

Functions

- On-chip electronic volume control for graphic equalizer with 7 bands each of right/left
- 2dB/step variable in each band
- Maximum boost of +12dB, maximum cut of −12dB, and 13 positions in each band
- Simultaneous drive of right/left band
- Band setting by serial data input, 2 control lines
- CMOS LSI of 16V breakdown voltage

Features

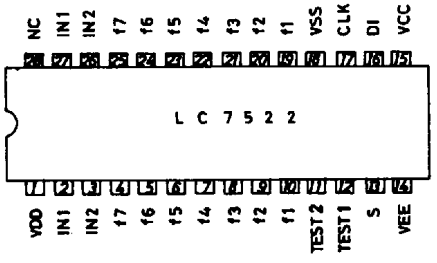
By using 3 chips of the LC7522, a controller (LC7060 or general-purpose microcomputer LC6502C), and a display LSI (LC7560→LCD, LC7565→FLT, LED), an electronic graphic equalizer system with the following features can be formed.

- The gain in each band can be increased/decreased with one touch.
- Since the preset memory contents can be called with one touch, your desired frequency characteristic to the music can be selected.
  (Example) User option 2 modes + maker option 3 modes + last channel memory
- ' 0dB in each band (flat function) ', ' The frequency characteristic in each band is reversed with respect to 0dB (reverse function) '. - - - - These functions can be software-controlled with one touch.
- Spectrum analyzing display can be used to provide recording equalization easily.
- Since 2 control lines can be also used for a display LSI, wiring between microcomputer and LSI is facilitated.

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

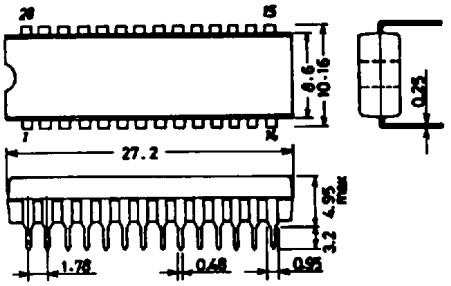
		Pin Name	Conditions		unit
Maximum Supply Voltage	V_{DD} max	V_{DD}, V_{EE}	$-8V \leqq V_{EE} \leqq V_{SS} \leqq V_{DD}$	16	V
	V_{EE} max	V_{DD}, V_{EE}	$-8V \leqq V_{EE} \leqq V_{SS} \leqq V_{DD}$	16	V
	V_{CC} max	V_{CC}		V_{SS} to $V_{SS}+7$	V
Maximum Input Voltage	V_{I1}	CLK, DI		0 to $V_{CC}+0.3$	V
	V_{I2}	f1 to f7, IN1, IN2		$V_{EE}-0.3$ to $V_{DD}+0.3$	V
	V_{I3}	S		$V_{EE}-0.3$ to $V_{DD}+0.3$	V
Allowable Power Dissipation	Pd max		Ta = 75°C	200	mW
Operating Temperature	Topg			−30 to +75	°C
Storage Temperature	Tstg			−40 to +125	°C

Pin Assignment



Case Outline 3029A

(unit : mm)



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Recommended Operating Conditions at Ta = 25°C, V_{SS} = 0V

		Pin Name	Conditions		unit
Supply Voltage	V_{DD}	V_{DD}, V_{EE}	$-7.0V \leqq V_{EE} \leqq V_{SS} \leqq V_{DD}$	14	V
	V_{EE}	V_{DD}, V_{EE}	$-7.0V \leqq V_{EE} \leqq V_{SS} \leqq V_{DD}$	14	V
	V_{CC}	V_{CC}		5.0	V

Allowable Operating Conditions at Ta = 25°C, V_{SS} = 0V, $V_{DD} \geqq V_{CC}$

		Pin Name	Conditions		unit
Supply Voltage	V_{DD}	V_{DD}, V_{EE}	$-7.5V \leqq V_{EE} \leqq V_{SS} \leqq V_{DD}$	7.5 to 15.0	V
	V_{EE}	V_{DD}, V_{EE}	externally connect a capacitor of 1000pF or greater across $V_{DD} - V_{SS}$, $V_{CC} - V_{SS}$ and $V_{EE} - V_{SS}$.	7.5 to 15.0	V
	V_{CC}	V_{CC}	$V_{CC} \leqq V_{DD}$	4.5 to 5.5	V
Input 'H'-Level Voltage	V_{IH1}	CLK, DI		$0.8V_{CC}$ to V_{CC}	V
	V_{IH2}	S		$0.9(V_{DD} - V_{EE}) + V_{EE}$ to V_{DD}	V
Input 'L'-Level Voltage	V_{IL1}	CLK, DI		$0.2V_{CC}$	V
	V_{IL2}	S		V_{EE} to $0.1(V_{DD} - V_{EE}) + V_{EE}$	V
Input Pulse Width	tøW	CLK		1 min.	μs
Setup Time	t set up	DI		1 min.	μs
Hold Time	t hold	DI		1 min.	μs
Operating Frequency	fopg	CLK		up to 330	kHz

Electrical Characteristics at Ta = 25°C

		Pin Name	Conditions	min	typ	max	unit
Total Harmonic Distortion	THD 1		V_{OUT} = 1V, flat mode, f = 20kHz, Test Circuit 1		0.005	0.01	%
	THD 2		V_{OUT} = 1V, flat mode, f = 1kHz, Test Circuit 1		0.0015	0.003	%
	THD 3		V_{OUT} = 1V, boost mode, f = 20kHz, Test Circuit 1		0.04	0.1	%
	THD 4		V_{OUT} = 1V, boost mode, f = 1kHz, Test Circuit 1		0.015	0.03	%
Crosstalk between Channels	Xtalk		V_{OUT} = 1V, f = 20kHz, Test Circuit 2		55		dB
Setting Error	ΔB		Other band flat, $V_{DD} - V_{EE}$ = 14V, Test Circuit 1	−1		+1	dB
Current Dissipation	I_{DD}		$V_{DD} - V_{EE}$ = 15V			1	mA
	I_{CC}		V_{CC} = 5V			1	mA
Analog SW OFF Leakage Current	I_{OFF}		f1 to f7			10	μA

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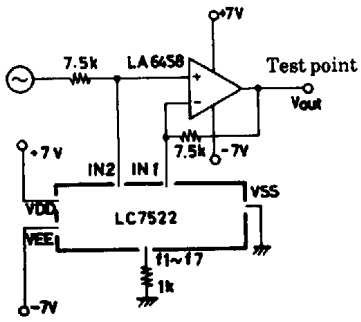
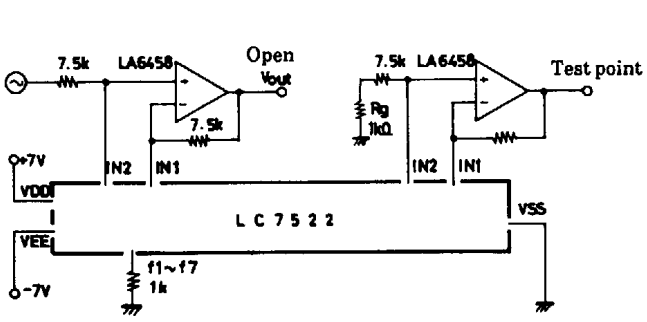
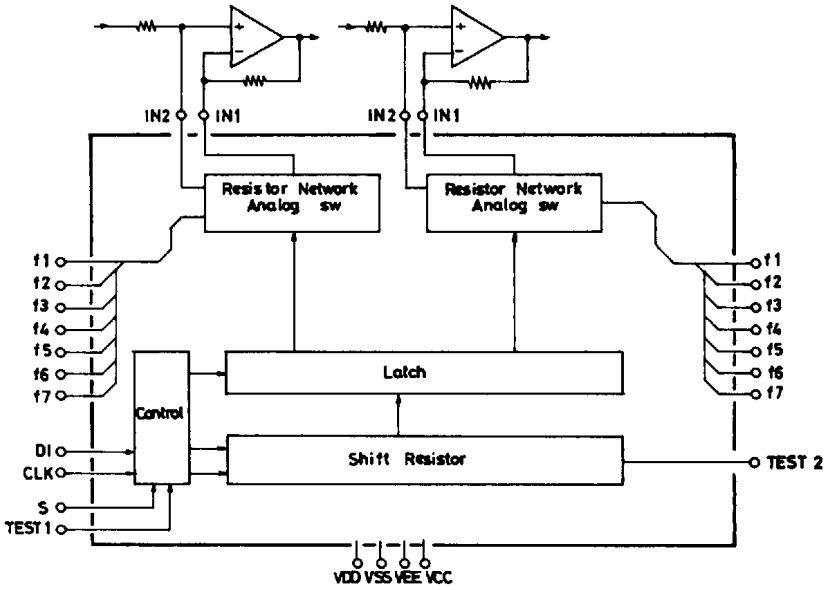
Test Circuit 1



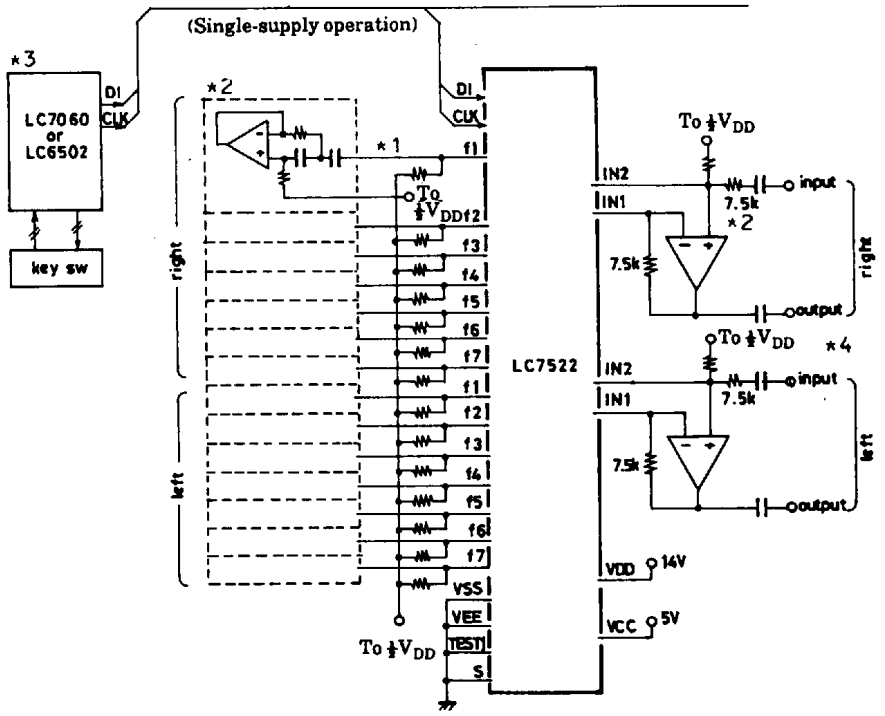
Test Circuit 2



Equivalent Circuit Block Diagram



Sample Application Circuit



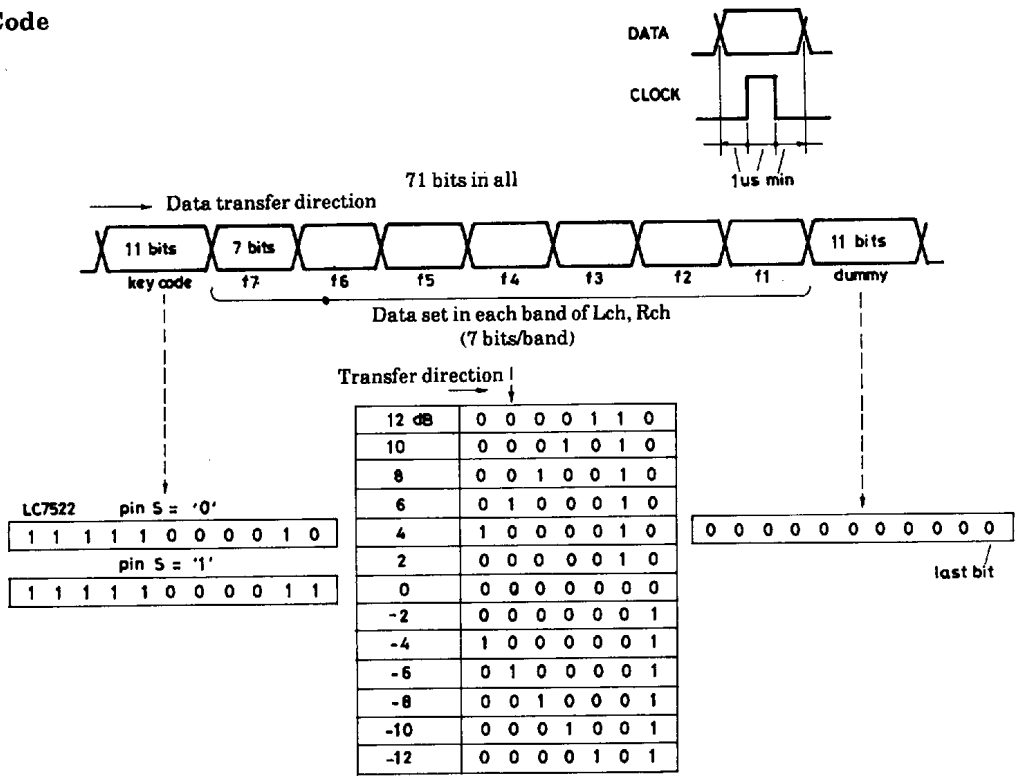
*1 It is recommended that $1/2V_{DD}$ is applied to pins f1 to f7 through resistors of 1MΩ so that noise is minimized at the select mode.

*2 The optimum conditions for 2dB/step are as follows :
V_{DD} = 14V, feedback resistance of OP amp : 7.5kΩ, equivalent LC resonance impedance : 1kΩ
(For V_{DD} = 8V, the LC7523 is recommended.)

*3 The LC7060 is available as a standard controller.

*4 The LC7560 (LCD driver), LC7565 (FLT, LED driver) are available as spectrum analyzing display drivers for graphic equalizer output signal.

Data Code

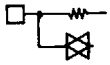
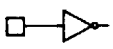


12 dB	0 0 0 0 1 1 0
10	0 0 0 1 0 1 0
8	0 0 1 0 0 1 0
6	0 1 0 0 0 1 0
4	1 0 0 0 0 1 0
2	0 0 0 0 0 1 0
0	0 0 0 0 0 0 0
-2	0 0 0 0 0 0 1
-4	1 0 0 0 0 0 1
-6	0 1 0 0 0 0 1
-8	0 0 1 0 0 0 1
-10	0 0 0 1 0 0 1
-12	0 0 0 0 1 0 1

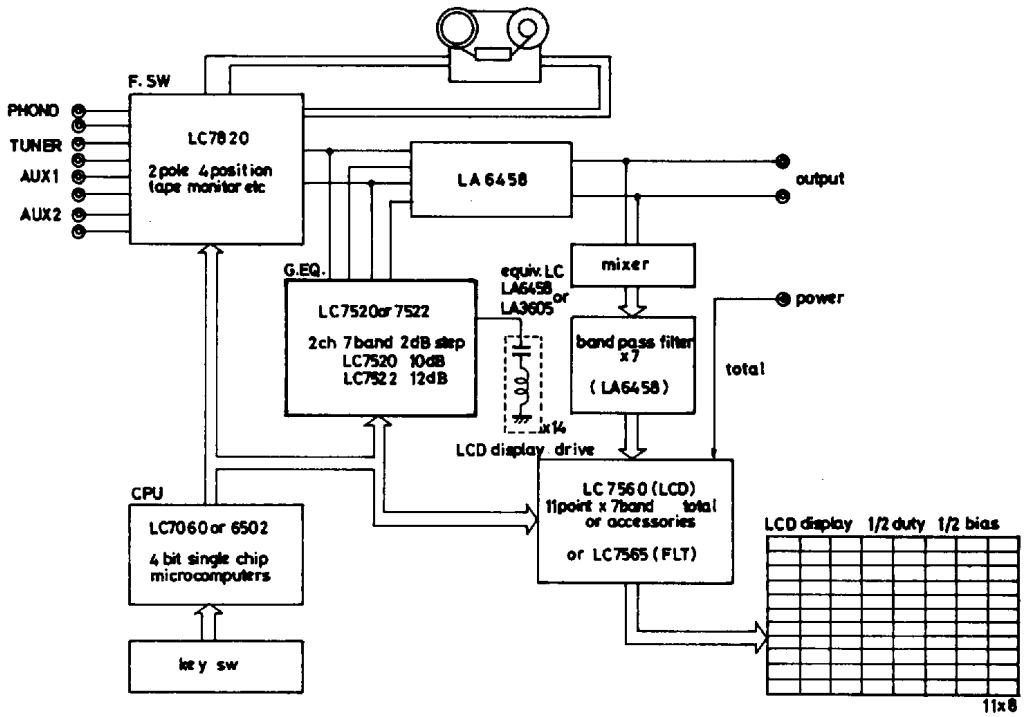
Note 1. When power is applied, data "0" must be first transferred for 60 clocks (initial clock) or more. If data transfer is stopped halfway, the transfer of the remaining data must be completed or data transfer must be started after the initial clocks have been transferred.

Note 2. When the DI, CLK pins are shared with the LC7560, etc., the maximum initial clocks for such device must be transferred.

Pin Description

Pin Name	Pin Configuration	Description
V_{DD} V_{SS} V_{EE} V_{CC}		Power supply pin +7V typ. power supply for audio signal Power supply pin 0V Power supply pin −7V typ. power supply for audio signal, connected to V_{SS} at single-supply operation Power supply pin +5V typ.
DI		Used to input data from CPU Schmitt inverter type
CLK		Used to input clock from CPU Schmitt inverter type
IN1 IN2		Audio signal input pin Normally, IN1 is connected to inverting input of OP amp. Normally, IN2 is connected to noninverting input of OP amp. Provided in Lch/Rch
f1 to f7		Band-pass filter connecting pin f1 to f7 × 2 (right/left) = 14(total) pins
S		Select pin at 2-chip used mode To accept data under key code 7C3, S must be set to '1'. →Connected to V_{DD} To accept data under key code 7C2, S must be set to '0'. →Connected to V_{EE}
TEST1 TEST2		IC test pin Open during operation

[Reference 1] ECS System/Graphic Equalizer Application Circuit Block Diagram



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[Reference 2] Main Specifications for LC7060 (CMOS LSI/Graphic Equalizer Controller)

Use

Controller LSI for graphic equalizer electronic volume control LSI : LC7520,7522, LCD driver : LC7560, FLT driver : LC7565.

Functions

- 7 bands, 2dB/step, ±10dB (±12dB) variable, ( ) : LC7522/7565-combined use.
- Max. 8 memories (user option 5 modes, maker option 3 modes) + last channel memory.
- Possible to control function switch (5 positions) and electronic volume control.
- 2 control lines for graphic equalizer electronic volume control and display IC
- Buzzer sound is generated when a key is operated.
- On-chip remote control reception program.

Features

- Any combination of graphic equalizer electronic volume control LSI LC7520,7522, and display driver LSI LC7560,7565 may be used. (Port-selectable)
- FLAT function to permit the FLAT mode to be entered with one touch.
- REVERSE function to permit the frequency characteristic to be reversed with respect to 0dB with one touch.
- Tuner band select and SCAN output.
- MUTE and MUTE output.
- Backup operation available.