TC5093AP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

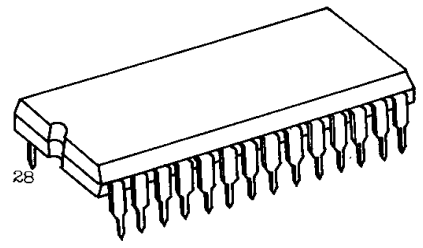
TC5093AP 8 BIT ANALOG TO DIGITAL CONVERTER

GENERAL DESCRIPTION

The TC5093AP is a monolithic CMOS 8 bit successive approximation A/D converter with 8 channel multiplex inputs. After an analog input channel is selected with channel select input (CH0 ∿ 2) and channel latch input (CHL), when STC is set high EOC goes low at the leading edge of STC and the conversion starts.
After the conversion is completed, EOC returns high and the new data replace the previous data at DB0 ∿ DB7.
The TC5093AP has features of high speed, high accuracy and very low power consumption which make the device well suited to a broad application field such as process and machine control and automotive equipment.

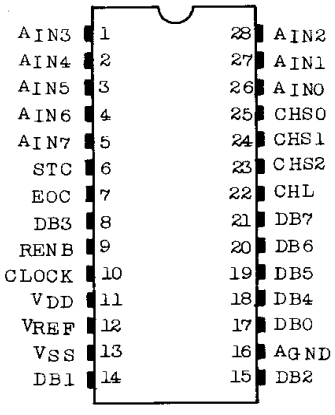
FEATURES

- High accuracy ..... $\pm\frac{1}{2}$ LSB TYP
- High speed conversion .... 100 μsec TYP @f_{cp}=640 kHz
- Single power supply ..... 5V ± 10%
- Low power consumption ..... 9mW MAX @T_a=25°C
- 8 channel analog multiplex input
- Easy interface to all microprocessors
- Zero or full scale adjustment free
- Latched 3-state output



DIP28 (6D28A-P)

PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{DD}	V_{SS}-0.5∿V_{SS} +7	V
DC Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD} +0.5	V
DC Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD} +0.5	V
Reference Volage	V_{REF}	V_{SS}-0.5∿V_{DD} +0.5	V
Analog Ground Voltage	AGND	V_{SS}-0.5∿V_{DD} +0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{STG}	-65 ∿150	°C
Lead Temperature 10 sec.	T_L	300	°C

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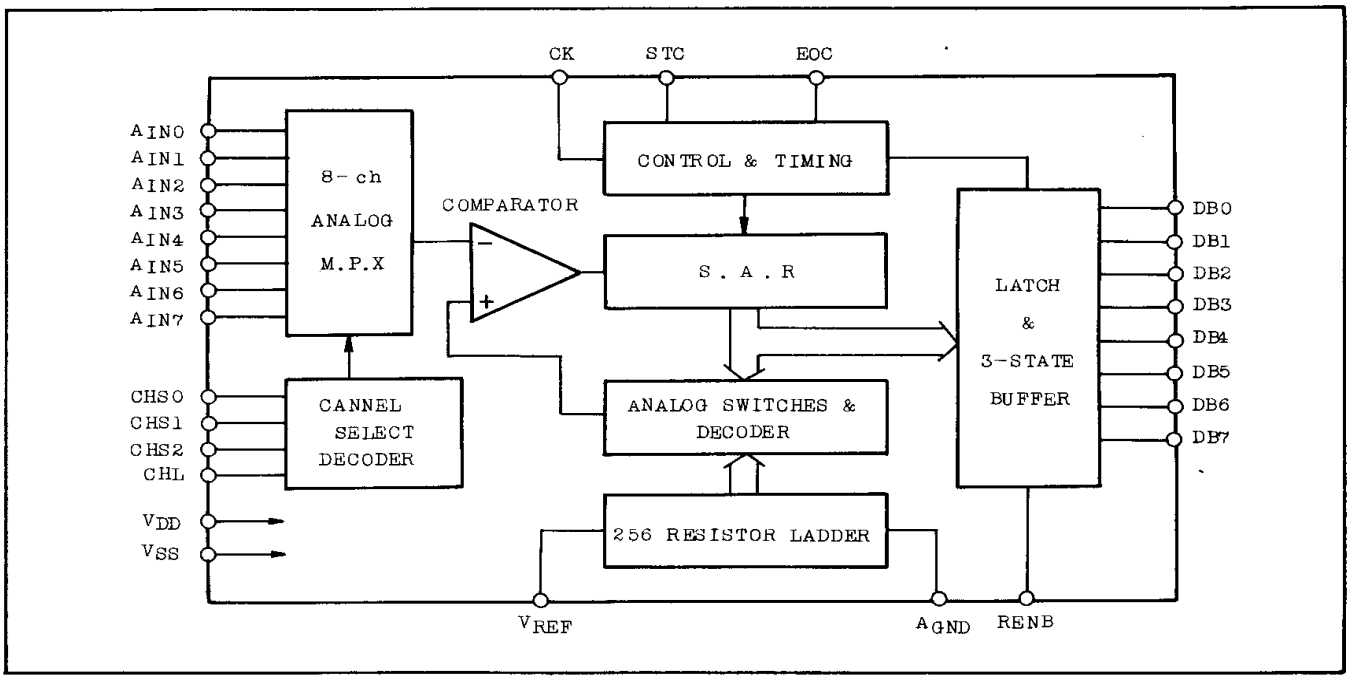
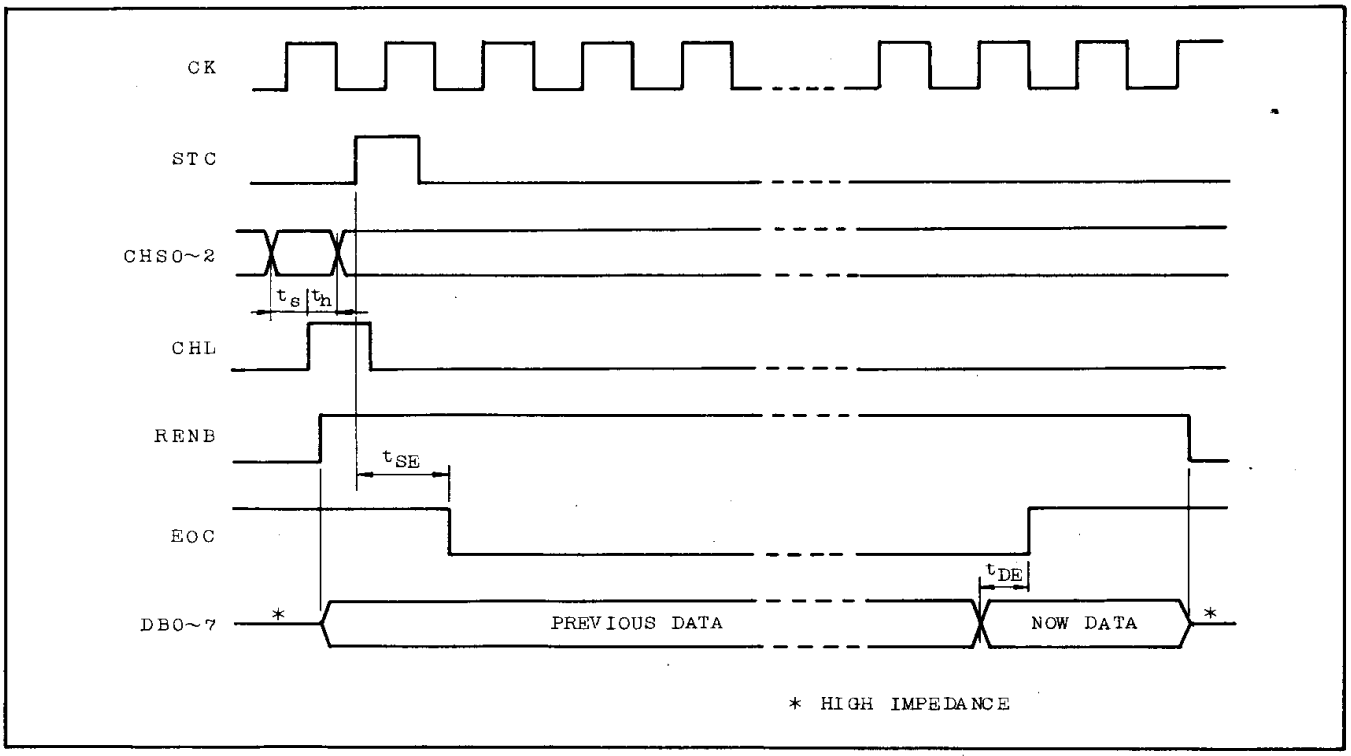
BLOCK DIAGRAM



TIMING CHART



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PIN & FUNCTION

PIN NO.	SYMBOL	PIN NAME & FUNCTION
1	A_{IN3}	[ANALOG INPUT] The analog input voltage applied to the selected channel is converted. Full range of input signal is to be from A_{GND} to V_{REF}.
2	A_{IN4}	
3	A_{IN5}	
4	A_{IN6}	
5	A_{IN7}	
6	STC	[START CONVERSION] Conversion starts at the falling edge of STC.
7	EOC	[END OF CONVERSION] EOC becomes low level at the rising edge of STC. And when the conversion is completed EOC returns to high level.
8	DB3	3-STATE PARALLEL DATA OUTPUT
9	RENB	[READ ENABLE] Output enable signal "H" = DB0 ∿7 enable "L" = DB0 ∿7 high impedance
10	CLOCK	[CLOCK INPUT] Basic system clock
11	V_{DD}	[SYSTEM POWER SUPPLY] V_{DD}=5V ±10%
12	V_{REF}	[REFERENCE VOLTAGE] V_{REF}defines the full scale of A_{IN}.
13	V_{SS}	[SYSTEM GROUND] V_{SS}=0V
14	DB1	3-STATE PARALLEL DATA OUTPUT
15	DB2	3-STATE PARALLEL DATA OUTPUT
16	A_{GND}	[ANALOG GROUND] A_{GND} defines the zero level of A_{IN}.
17	DB0	3-STATE PARALLEL DATA OUTPUT DB0 : LSB DB7 : MSB
18	DB4	
19	DB5	
20	DB6	
21	DB7	
22	CHL	[CHANNEL LATCH INPUT] The channel select signals CHS0 ∿2 are latched at the rising edge of CHL.
23	CHS2	[CHANNEL SELECT INPUT] One of A_{IN0} ∿A_{IN7} is selected according to the status of CH0 ∿CH2.
24	CHS2	
25	CHS0	
26	A_{IN0}	[ANALOG INPUT]
27	A_{IN1}	
28	A_{IN2}	

CHS2	CHS1	CHS0	ON CHANNEL
L	L	L	AIN0
L	L	H	AIN1
L	H	L	AIN2
L	H	H	AIN3
H	L	L	AIN4
H	L	H	AIN5
H	H	L	AIN6
H	H	H	AIN7

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RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Reference Voltage	V_{REF}	V_{DD}=5V, AGND=0V	3.5	V_{DD}	V_{DD}	V
Analog Ground Voltage	AGND	V_{DD}=5V, V_{REF}=5V	0.0	0.0	3.0	V
Voltage Between V_{REF} and AGND		V_{DD}=5V ± 10%	2.0	V_{DD}	V_{DD}	V
Clock Frequency	f_{cp}	V_{DD}=5V ± 10% Duty Cycle=50%	10	640	1280	kHz
Operating Temperature	T_{opr}		-40	-	+85	°C

DC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

PARAMETER	SYMBOL	TEST CONDITION		-40°C		25°C			85°C		UNIT
			V_{DD}	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5.0	4.95	-	4.95	5.00	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5.0	-	0.05	-	0.00	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS}, V_{DD}	5.0	-1.2	-	-	-	-	-0.7	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V V_{IN}=V_{SS}, V_{DD}	5.0	2.4	-	2.0	-	-	1.6	-	mA
High Level Input Voltage	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V, 4.5V	5.0	3.5	-	3.5	-	-	3.5	-	V
Low Level Input Voltage	V_{IL}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V, 4.5V	5.0	-	1.5	-	-	1.5	-	1.5	V
3-State Output Disable Current	I_{DH} I_{DL}	V_{OH}=5.5V or V_{OL}=0.0V	5.5	-	±0.5	-	-	±0.5	-	±1	μA
Digital Input Current	I_{IH} I_{IL}	V_{IH}=5.5V or V_{IL}=0.0V	5.5	-	±0.3	-	-	±0.3	-	±1	μA
On Channel Input Current	I_{ON}	V_{IH}=5.5V or V_{IL}=0.0V f_{cp}= kHz	5.5	-	±2	-	-	±2	-	±5	μA
OFF Channel Input Current	I_{OFF}	V_{IH}=5.5V or V_{IL}=0.0V	5.5	-	±0.2	-	-	±0.2	-	±1	μA
Operating Current	I_{DD}	f_{cp}=1 MHz	5.0	-	2.0	-	-	1.8	-	2.0	mA
Reference Resistance	R_{REF}		-	4.0	1.7	4.3	7.5	17	4.3	19	kΩ

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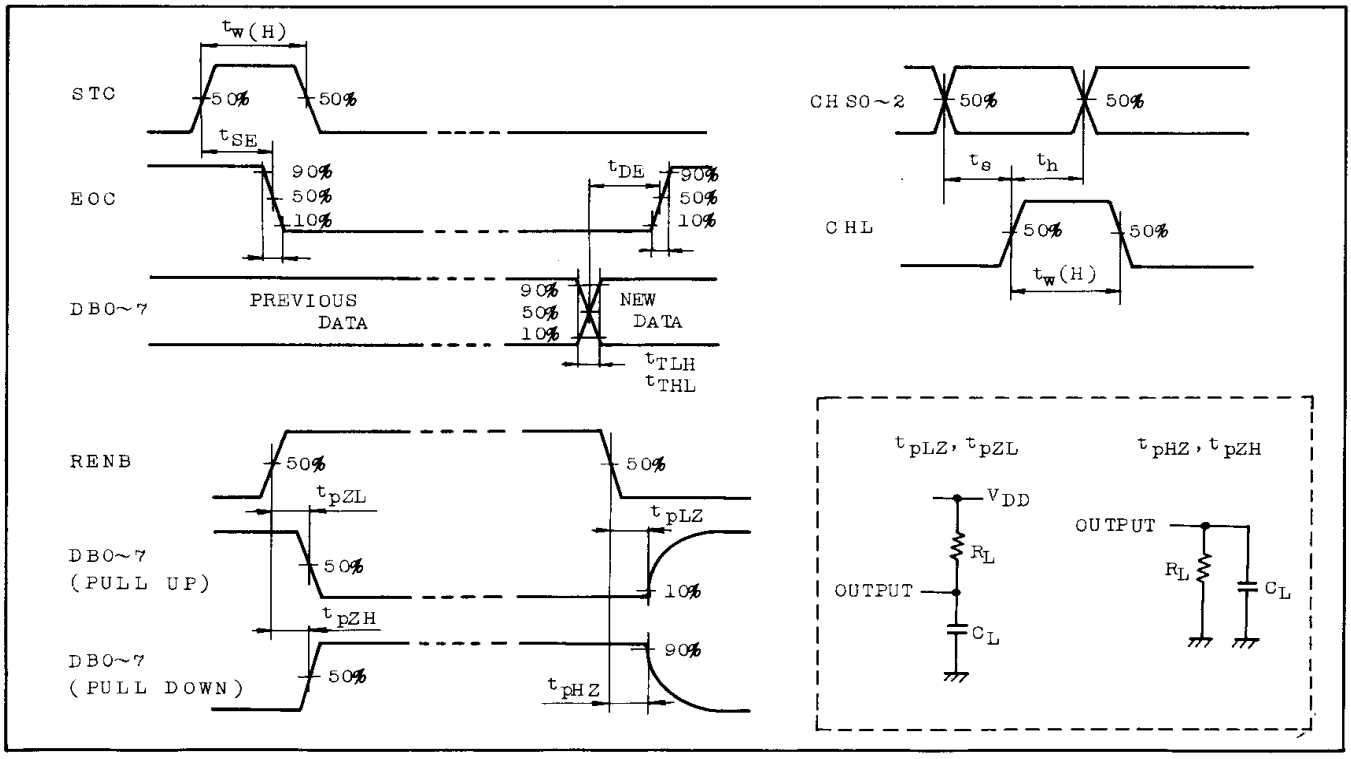
SWITCHING CHARACTERISTICS (V_{DD}=5.0V, T_a=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	C_L=50pF	-	50	100	nS
Propagation Delay Time (STC - EOC)	t_{SE}	C_L=50pF	10	1/2 CLOCK + 200	1/2 CLOCK + 600	
Data-EOC Time	t_{DE}	C_L=50pF	1 CLOCK -300	1 CLOCK -70	1 CLOCK	
3-State Output Enable Time	tpZH tpZL	C_L=50pF R_L=1k	-	85	200	
3-State Output Disable Time	tpHZ		-	85	200	
	tpLZ			65	200	
Minimum Pulse Width (STC, CHL)	$t_{w(H)}$	C_L=50pF	-	40	100	
Minimum Set-up Time (CHS0 ∿2)	t_s	C_L=50pF	-	2	50	
Minimum Hold Time (CHS0 ∿2)	t_h	C_L=50pF	-	0	50	
Input Capacitance	C_{IN1}	Digital Input	-	5	-	pF
Input Capacitance	C_{IN2}	Analog In(ON)	-		-	
Input Capacitance	C_{IN3}	Analog In(OFF)	-		-	
Output Capacitance	C_{OUT}	3-State Out	-	10	-	

SWITCHING CHARACTERISTICS TEST WAVEFORM



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SYSTEM CHARACTERISTICS (T_a=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E_{ZR}	V_{DD}=5.0V V_{REF}=5.000V t_{cp}=1 MHz	-	$\pm\frac{1}{4}$	±1	LSB
Full Scale Error	E_{FS}		-	$\pm\frac{1}{2}$	±1	
Nonlinearity Error	E_{LI}		-	$\pm\frac{1}{2}$	±1	
Conversion Time	T_C	f_{cp}=640 kHz	-	100		µs
		f_{cp}=1280 kHz	-	50		

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