No:3042

LC7821N,7822N,7823N

CMOS LSI

Analog Function Switch

Use

· Serial data-controlled function select switch suited for use in amplifiers, receivers.

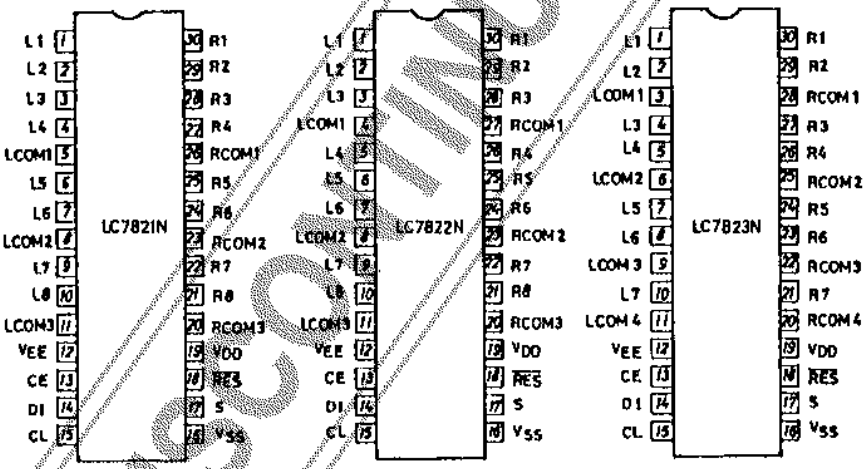
Features

· Analog switches of 8 channels × 2 (LC7823N : 7 channels × 2) are contained. Three types are available according to the internal connection.
· Control is exercised by serial data. The LC7821N,7822N,7823N may be interfaced with a microcomputer (5V supply) easily.
· Even if two ICs of the same type are used, they may be connected to the common bus line because the S (selector) pin is provided.
· Reset pin used to turn OFF all analog switches
· Wide dynamic range because of ±20V breakdown voltage

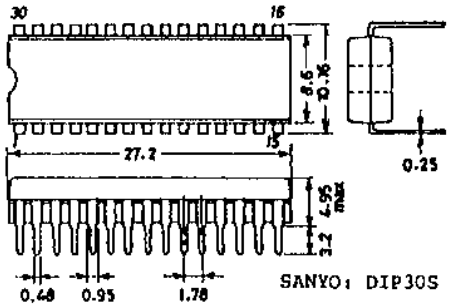
Absolute Maximum Ratings at Ta = 25°C

				unit
Maximum Supply Voltage	V_{DD} max	V_{DD}	−0.3 to +20	V
	V_{EE} max	V_{EE}	−20 to +0.3	V
Maximum Input Voltage	V_I1	DI,CL,CE,S,$\overline{RES}$	−0.3 to +20	V
	V_I2	L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	V_{EE} −0.3 to V_{DD} +0.3	V
Analog Switch ON-State Voltage Difference	ΔV_{ON}	Switch ON	0.5	V
Allowable Power Dissipation	Pd max	Ta≦75°C	100	mW
Operating Temperature	Topg		−30 to +75	°C
Storage Temperature	Tstg		−40 to +125	°C

Pin Assignment



Case Outline 3047A-D30SIC
(unit : mm)



Specifications and information herein are subject to change without notice.

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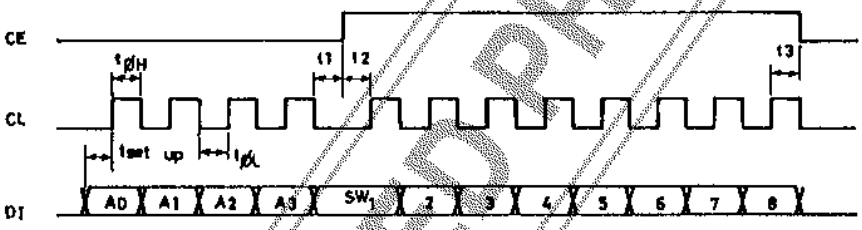
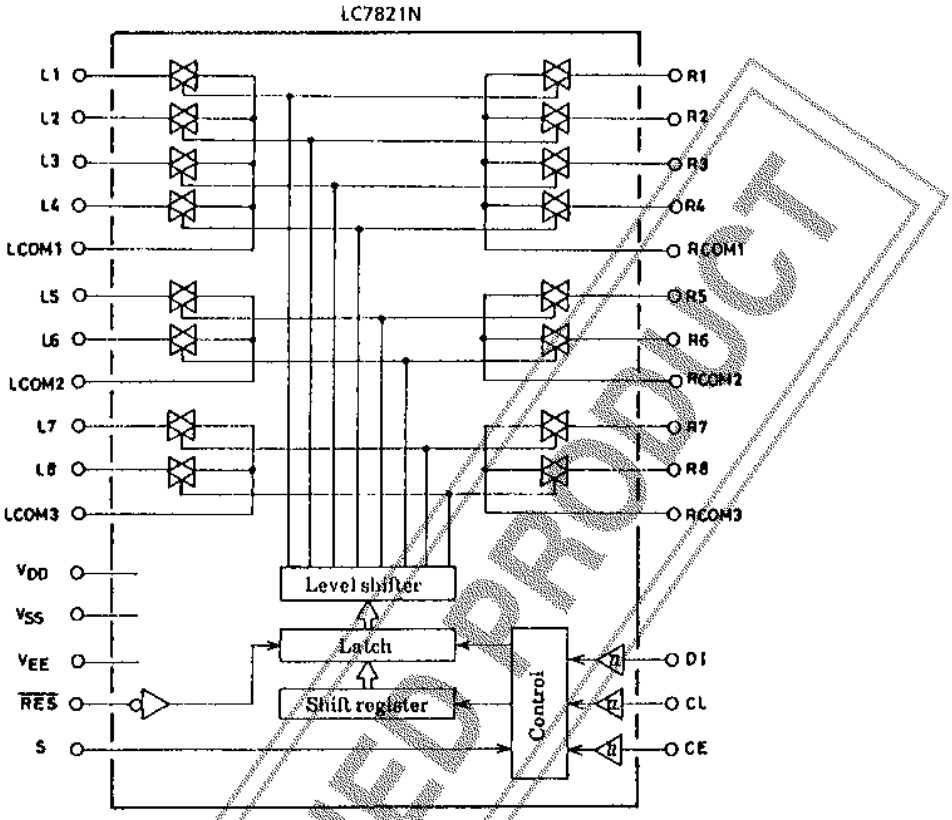
Allowable Operating Conditions at Ta = 25°C, V_{SS} = 0V, $\|V_{DD}\| \geqq \|V_{EE}\|$			min	typ	max	unit
Maximum Supply Voltage	V_{DD}	$V_{DD} - V_{EE} \geqq 12V$: V_{DD}	6.0		18.5	V
	V_{EE}	$V_{DD} - V_{EE} \geqq 12V$: V_{EE}	−18.5		0	V
Input "H"-Level Voltage	$V_{IH}1$	DI,CL,CE,S	4.0		18.5	V
	$V_{IH}2$	$\overline{RES}$	$0.7V_{DD}$		V_{DD}	V
Input "L"-Level Voltage	$V_{IL}1$	DI,CL,CE,S	0		0.7	V
	$V_{IL}2$	$\overline{RES}$	0		$0.3V_{DD}$	V
Analog Switch Input Voltage Range	V_{IN}	L1 to L8,R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	V_{EE}		V_{DD}	V
"L"-Level Clock Pulse Width	$t_{\phi L}$	C_L	0.5			μsec
"H"-Level Clock Pulse Width	$t_{\phi H}$	C_L	0.5			μsec
Setup Time	t_{setup}	CL,DI	0.5			μsec
	t_1*	CL,CE	0.5			μsec
	t_2*	CL,CE	0.5			μsec
	t_3*	CL,CE	0.5			μsec
Reset Minimum Pulse Width	t_{wRES}	$V_{DD} \geqq 6V$: $\overline{RES}$	1.0			μsec
Hysteresis Width	V_H	CL,CE,DI	0.3			V

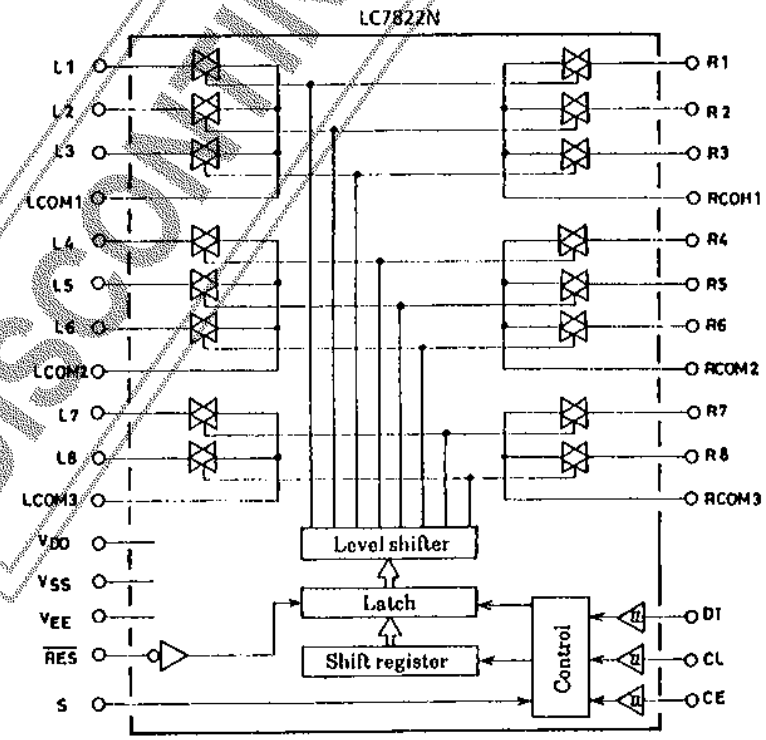
* : CE,CL,DI waveforms



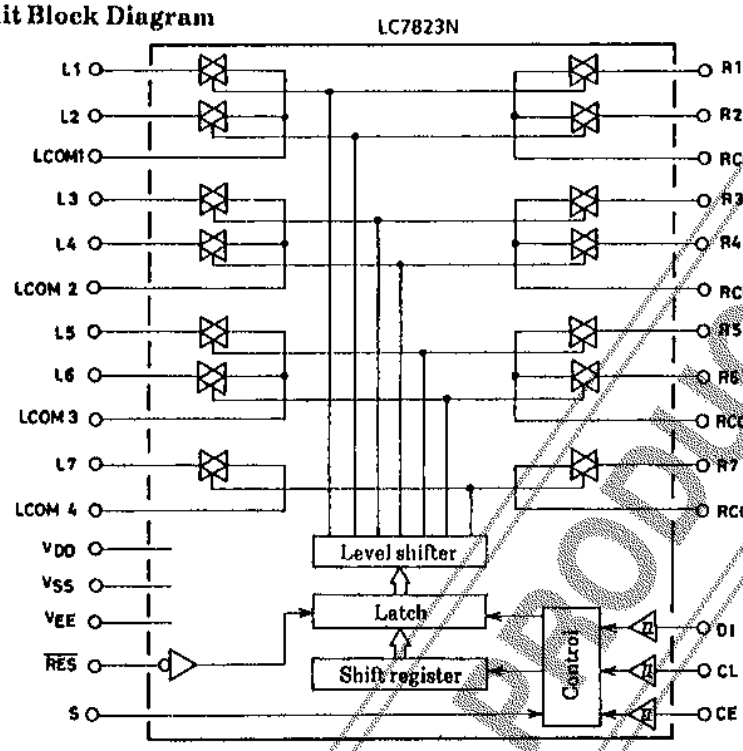
Electrical Characteristics at Ta = 25°C, V_{SS} = 0V			min	typ	max	unit
Analog Switch ON-State Resistance	$R_{ON}1$	I = 1mA, $V_{DD} - V_{EE}$ = 12V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		150		Ω
	$R_{ON}2$	I = 1mA, $V_{DD} - V_{EE}$ = 37V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		70		Ω
Total Harmonic Distortion	THD1	V_{IN} = 1Vrms, f = 1kHz, $V_{DD} - V_{EE}$ = 37V : L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		0.0015	0.01	%
	THD2	V_{IN} = 0.1Vrms, f = 1kHz $V_{DD} - V_{EE}$ = 37V : L1 to L8, R1 to R8 LCOM1 to LCOM4, RCOM1 to RCOM4		0.01	0.05	%
Feedthrough	F_{TH}	V_{IN} = 0dBV, f = 10kHz, V_{DD-EE} = 37V : L1 to L8, R1 to R8 LCOM1 to LCOM4, RCOM1 to RCOM4		55		dB
Crosstalk	CT	V_{IN} = 0dBV, f = 10kHz, $V_{DD} - V_{EE}$ = 37V : L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		75		dB
Input "H"-Level Current	I_{IH}	V_I = 18.5V ; DI,CL,CE,S,$\overline{RES}$			10	μA
Input "L"-Level Current	I_{IL}	V_I = 0V: DI,CL,CE,S,$\overline{RES}$	−10			μA
Analog Switch OFF-State Leakage Current	I_{OFF}	$V_I = V_{EE}$ to V_{EE} + 37V : L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	−10		10	μA
Current Dissipation	I_{DD}	V_{DD}			1.0	mA

Equivalent Circuit Block Diagram





Equivalent Circuit Block Diagram



Pin Description

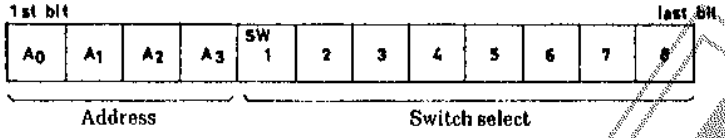
Pin Name	I/O	Internal Equivalent Circuit	Function
V_{DD},V_{SS},V_{EE}			Power supply pins
L1 to L8,R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		See Block Diagram.	Input/output pins for analog switches.
CL,DI,CE	I		Srial data input pins (Schmitt buffer) CL---Clock input pin DI---Data input pin CE---Chip enable pin
S	I		Select pin in the two ICs-used mode When the S pin is brought to "L" or "H" level, the address will become as shown below.
$\overline{RES}$	I		Reset pin When power is applied, the state of the analog switches will be indeterminate. When this pin is brought to "L" level, all analog switches will be turned OFF.

Type No.	S Pin	Address			
		A0	A1	A2	A3
LC7821N	L	0	1	0	1
	H	1	1	0	1
LC7822N	L	0	0	1	1
	H	1	0	1	1
LC7823N	L	0	1	1	1
	H	1	1	1	1

Operation Description

1. Data input method

The LC7821N,7822N,7823N are controlled by inputting serial data to the CL, DI, CE pins. Data consists of 12bits in all (address : 4 bits, data : 8 bits).



Each switch No. corresponds to analog switches L1 to L8, R1 to R8.
Set the bit of a switch to be turned ON to 1.

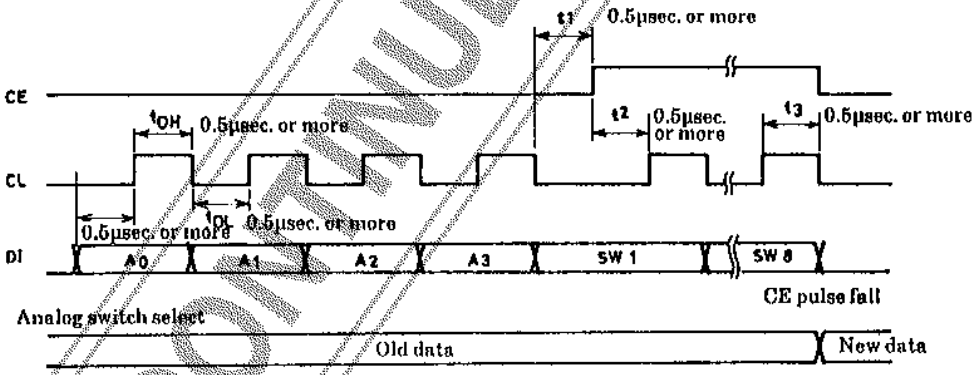
0 ------- OFF
1 ------- ON

The address is used for chip select when connected to the common bus line.
When the S pin is brought to "L" or "H" level, the transmit data will become as shown below.

Type No.	S Pin	Address			
		A0	A1	A2	A3
LC7821N	L	0	1	0	1
	H	1	1	0	1
LC7822N	L	0	0	1	1
	H	1	0	1	1
LC7823N	L	0	1	1	1
	H	1	1	1	1

Note : For the LC7823N, the bit of switch 8 becomes "don't care" (0 or 1).
The reason for this is that the LC7823N contains 7 channels × 2 of analog switches.

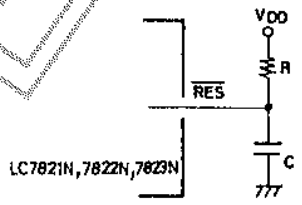
2. Timing of DI,CL,CE pulse signals

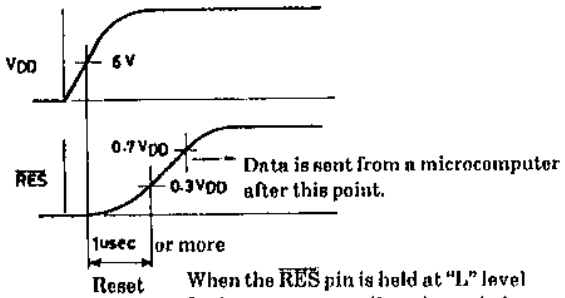


Data is fetched into the inside on the positive transition of the CL pulse and latched on the negative transition of the CE pulse.

3. Reset pin

When power is applied, the state of the analog switches will be indeterminate. All analog switches may be turned OFF by connecting C, R to this pin externally.

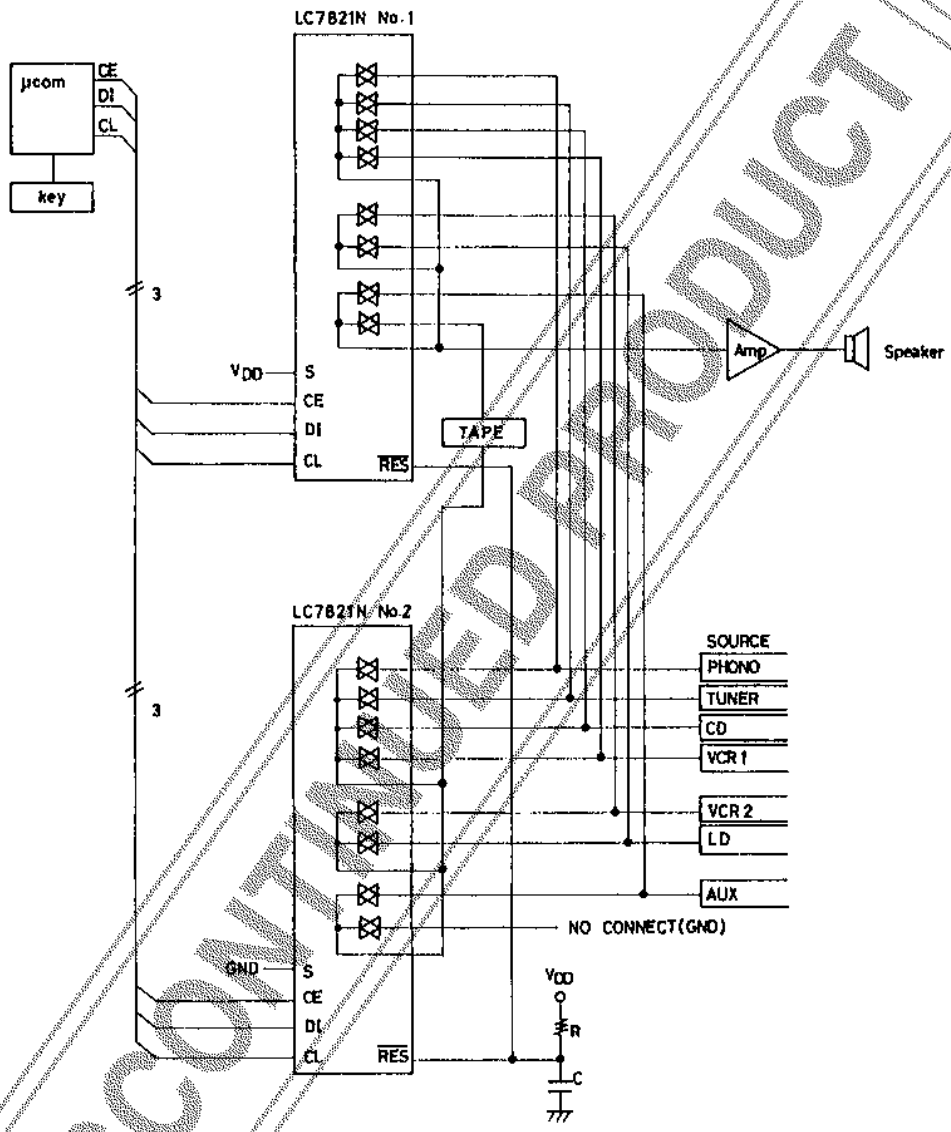




When the $\overline{RES}$ pin is held at "L" level for 1 μsec. or more, all analog switches will be turned OFF.

4. When the C²B is shared by plural ICs :
The state of the LC7821N,7822N,7823N remains unchanged until they receive the address data assgined to them.

Sample Application Circuit



Note) The other channel also has the same connection.