
HA19510/MP

High-Speed, Low-Power 8-bit Flash D/A Converter

HITACHI

November 1996

Description

The HA19510/MP consists of high-speed, low-power 8-bit D/A converters. The digital and clock inputs of these monolithic bipolar LSIs are fully TTL/CMOS compatible. The noise-minimizing internal reference voltage generator and high conversion rate ($f_{CLK} = 40 \text{ MHz Min}$) make these devices suitable for high-speed image processing applications.

Features

- 8-bit resolution
- Conversion rate: 40 MHz (Min)
- Single power supply: +5 V
- TTL/CMOS compatible clock and digital inputs
- Internal reference voltage: +3.0 V (Typ)
- Low power consumption: 225 mW (Typ)

Applications

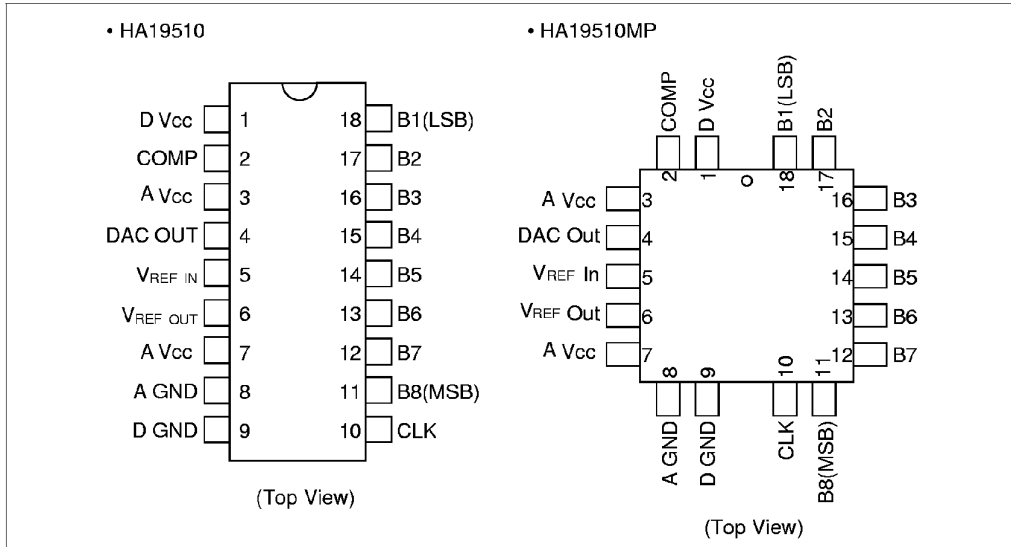
- Video signal processing
- Image processing, etc.

Ordering Information

Type No.	Package
HA19510	300mil 18-pin plastic DIP (DP-18A)
HA19510MP	18-pin plastic QFI (MP-18)

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Pin Arrangement

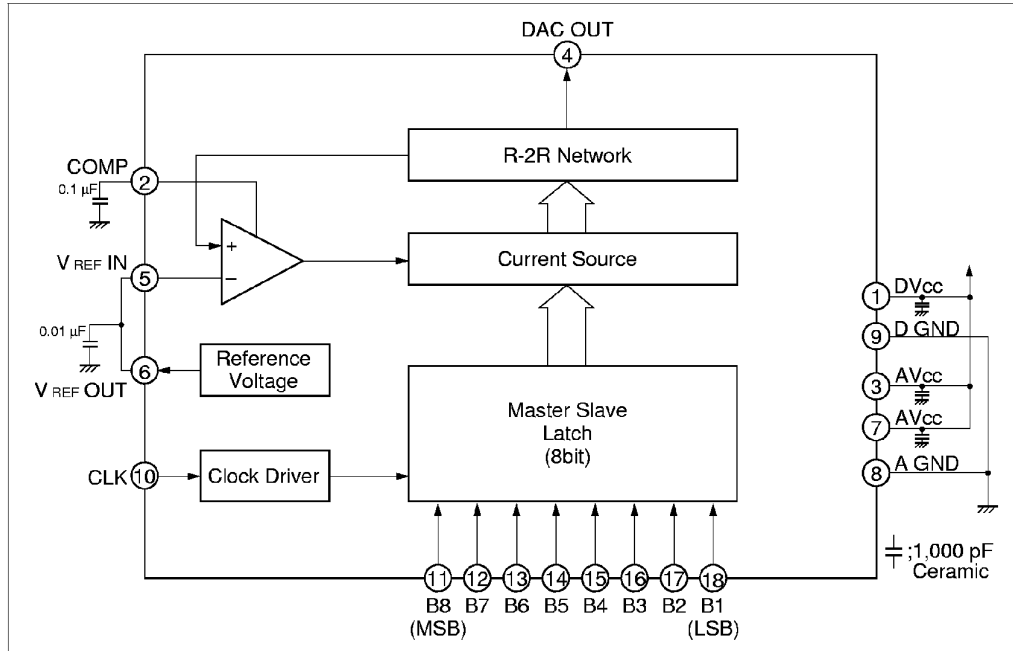


Pin Descriptions

Pin No.	Symbol	Function
1	D V _{CC}	Digital power supply (+5 V)
2	COMP	Phase compensation
3	A V _{CC}	Analog power supply (+5 V)
4	DAC OUT	Analog voltage output
5	V _{REF IN}	Reference voltage input
6	V _{REF OUT}	Reference voltage output
7	A V _{CC}	Analog power supply (+5 V)
8	AGND	Analog ground
9	DGND	Digital ground
10	CLK	Clock input
11	B8	Digital input (MSB)
12	B7	Digital input
13	B6	Digital input
14	B5	Digital input
15	B4	Digital input
16	B3	Digital input
17	B2	Digital input
18	B1	Digital input (LSB)

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Block Diagram



Absolute Maximum Ratings (Ta = 25°C, unless otherwise specified)

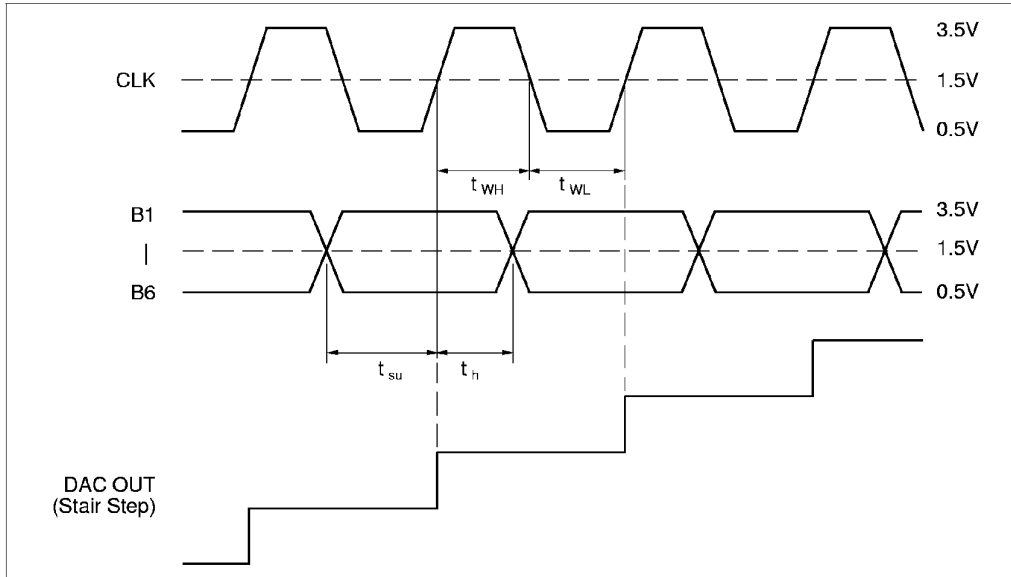
Item	Symbol	Rating	Unit
Power supply voltage	V _{CC}	+7.0	V
Digital input voltage	V _{IN}	0 to V _{CC}	V
Power dissipation	P _T	500	mW
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

Electrical Characteristics (Ta = 25°C, V_{CC} = 5.0 V, and pins 5 and 6 are shorted, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
Resolution		8	8	8	bit		
Conversion rate	f _{CLK}	40	—	—	MHz		
Linearity error	LE	-0.5	—	0.5	LSB		
Clock pulsewidth H-level	t _{WH}	12.5	—	—	ns	f _{CLK} = 40 MHz	
Clock pulsewidth L-level	t _{WL}	12.5	—	—	ns	f _{CLK} = 40 MHz	
Data setup time	t _{su}	10	—	—	ns	f _{CLK} = 40 MHz	
Data hold time	t _h	10	—	—	ns	f _{CLK} = 40 MHz	
Power supply voltage	V _{CC}	4.75	5.00	5.25	V		
Current consumption	I _{CC}	—	45	60	mA		
Digital input voltage	V _{IH}	2.0	—	V _{CC}	V		
	V _{IL}	0	—	0.8	V		
Digital input current	I _{IH}	—	—	20	μA	V _{IH} = 2.7 V	
	I _{IL}	-400	—	—	μA	V _{IL} = 0.4 V	
Reference input current	I _{REF IN}	-20	0	20	μA	V _{REF IN} = 3.0 V	
Reference input voltage	V _{REF IN}	2.0	3.0	4.0	V		
Reference output voltage	V _{REF OUT}	3.0	3.1	3.22	V		
Analog output voltage	Full Scale	V _{FS}	V _{CC} - 15 m	V _{CC}	V _{CC} + 15 m	V	V _{IH} ≥ 2.0 V
	Zero Scale	V _{ZS}	3.94	4.00	4.06	V	V _{IL} ≤ 0.8 V
Output Impedance	Z _{out}	55	75	95	Ω		

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Timing Chart



Input Code Table

B8	B7	B6	B5	B4	B3	B2	B1	Aout (V)
0	0	0	0	0	0	0	0	V_{ZS}
0	0	0	0	0	0	0	1	$V_{ZS} + 1 \text{ LSB}$
1	1	1	1	1	1	1	0	$V_{FS} - 1 \text{ LSB}$
1	1	1	1	1	1	1	1	V_{FS}

Note: $1 \text{ LSB} = (V_{FS} - V_{ZS})/255$

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HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071