Ordering number : EN4263B

Monolithic Digital IC

LB1823

Power Brushless Motor Predriver IC for OA Applications

Overview

The LB1823 is a predriver IC developed for driving power brushless motors in office automation applications. A motor driver circuit with the desired output power (current and voltage) can be constructed by attaching either a driver array or discrete components at the output. The LB1823 output supports direct PWM drive and thus allows the implementation of low-loss drive circuits. Additionally, the LB1823 includes several associated circuits, such as a speed control circuit, and FG amplifier, and an integrating amplifier, on chip.

Features

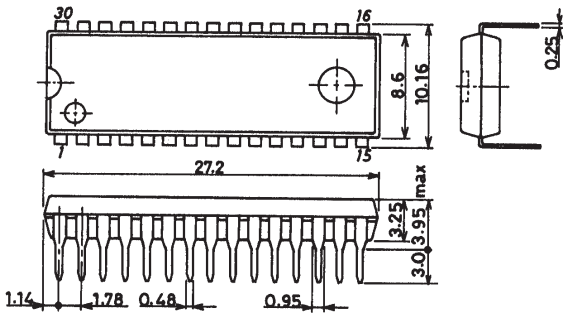
- Direct PWM drive output
- Crystal oscillator circuit
- Speed discriminator plus PLL speed control system
- Lock detector output
- Forward/reverse switching circuit
- Braking circuit (short braking technique)
- Start/stop switching circuit
- Over current limiter circuit (OCL)
- Thermal shutdown circuit (TSD)
- Built-in FG amplifier, integrating amplifier
- Shunt regulator output (7.0 V)

Package Dimensions

unit: mm

3196-DIP30SD

[LB1823]



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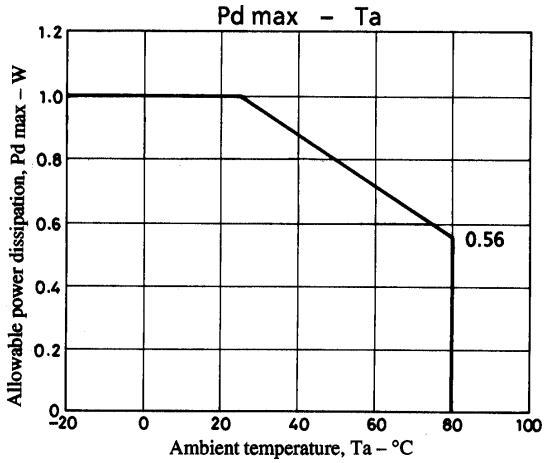

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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		9	V
Maximum input current	I_{REG}	V_{REG} pin	10	mA
Output current	I_O	UL, VL and WL outputs	30	mA
Allowable power dissipation	Pd max		1	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input current range	I_{REG}	V_{REG} pin (7 V)	1 to 5	mA
FG Schmitt output applied voltage	V_{FGS}		0 to 8	V
FG Schmitt output current	I_{FGS}		0 to 5	mA
Lock detector output current	I_{LD}		0 to 20	mA
Supply voltage	V_{CC}		4.5 to 7	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 6.3 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	$I_{CC}1$			33	50	mA
	$I_{CC}2$	When stopped		15	25	mA
Output saturation voltage	V_O sat	UL, VL and WL outputs: I_O = 20 mA		0.2	0.7	V
Output current	I_O	UH, VH and WH outputs: V_{OUT} = 1.4 V	8	12	16	mA
Output leakage current	I_O leak	UL, VL and WL outputs			100	µA
Output off voltage	V_O off	UH, VH and WH outputs			0.5	V
[Hall Amplifier]						
Input bias current	I_{HB}		–4	–1		µA
Common-mode input voltage range	V_{ICM}		1.5		4.4	V
Hall input sensitivity	ΔV_{IN}		60			mVp-p
Hysteresis	ΔV_{IN}		17	32	60	mV
Input voltage low to high	V_{SLH}			16		mV
Input voltage high to low	V_{SHL}			–16		mV
[Oscillator]						
Output high level voltage	$V_{OH\ (CR)}$		3.1	3.4	3.7	V
Output low level voltage	$V_{OL\ (CR)}$		1.2	1.5	1.8	V
Oscillator frequency	$f_{(CR)}$	R = 56 kΩ, C = 1500 pF		20		kHz
Amplitude	$V_{(CR)}$			2.0		Vp-p
[Current Limiter Operation]						
Limiter	V_{RF}		0.4	0.5	0.6	V
[Thermal Shutdown Operation]						
Thermal shutdown operating temperature	TSD	Design target	150	180		°C
Hysteresis	ΔTSD	Design target		30		°C
[V_{REG} Pin]						
V_{REG} pin voltage	V_{REG}		6.6	7.0	7.3	V

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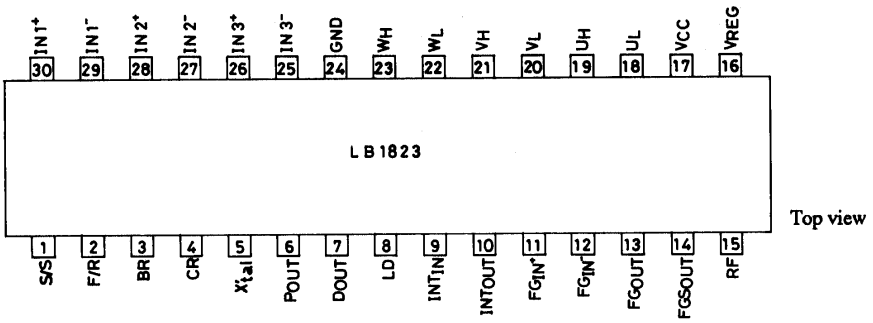
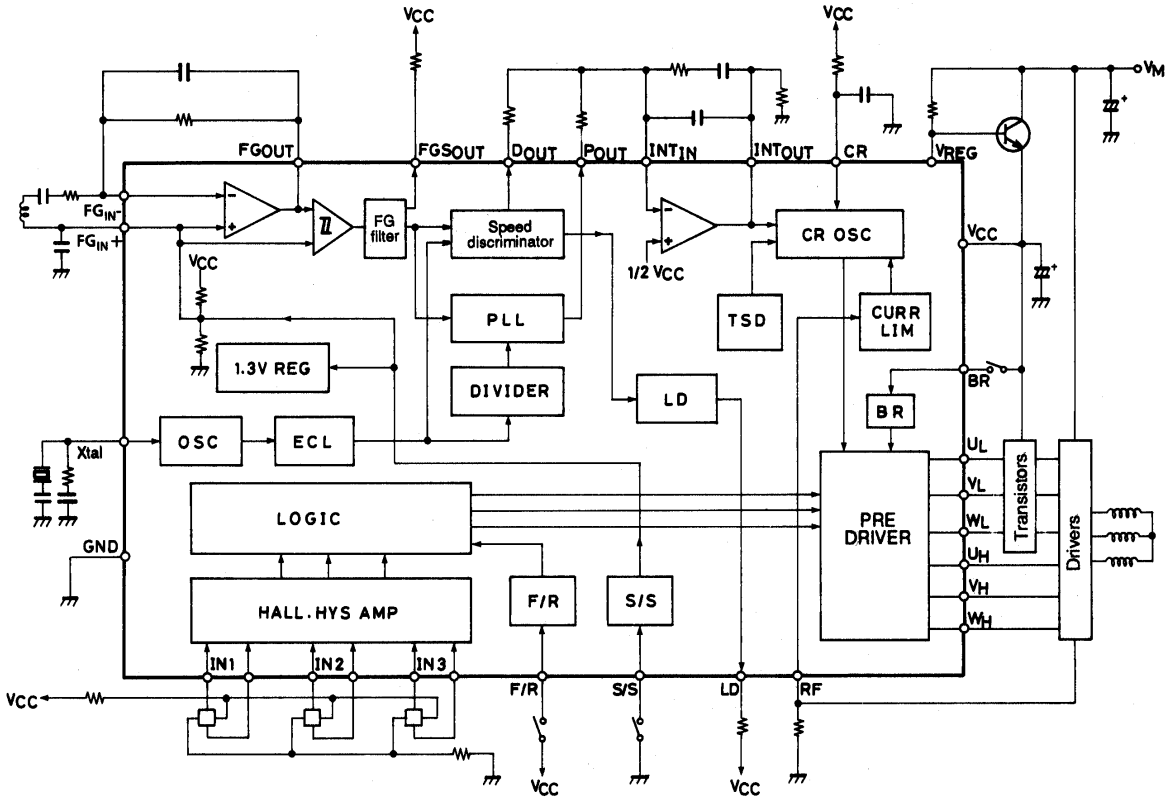
Parameter	Symbol	Conditions	min	typ	max	Unit
[FG Amplifier]						
Input offset voltage	$V_{IO\ (FG)}$		–10		+10	mV
Input bias current	$I_{B\ (FG)}$		–1		+1	μA
Output high level voltage	$V_{OH\ (FG)}$		4.8	5.3		V
Output low level voltage	$V_{OL\ (FG)}$			1	1.5	V
FG input sensitivity		Gain: 100 ×	3			mV
Schmitt amplitude for the next stage			100	180	250	mV
Operating frequency range					2	kHz
Open-loop gain		$f_{(FG)}$ = 2 kHz	45	51		dB
[FGS Output]						
Output saturation voltage	$V_{O\ (FGS)}$	$I_{O\ (FGS)}$ = 2 mA		0.1	0.5	V
Output leakage current	$I_{L\ (FGS)}$	$V_O = V_{CC}$			10	μA
[Speed Discriminator]						
Output high level voltage	$V_{OH\ (D)}$		5.3	5.6		V
Output low level voltage	$V_{OL\ (D)}$			0.4	1.1	V
[PLL Output]						
Output high level voltage	$V_{OH\ (P)}$		4.05	4.35	4.65	V
Output low level voltage	$V_{OL\ (P)}$		1.85	2.15	2.45	V
Number of counts				512		
[Lock Detector]						
Output low level voltage	$V_{OL\ (LD)}$	I_{LD} = 10 mA		0.1	0.5	V
Output leakage current	$I_{L\ (LD)}$	$V_O = V_{CC}$			10	μA
Lock range				±6.25		%
[Integrator]						
Input bias current	$I_{B\ (INT)}$		–0.4		+0.4	μA
Output high level voltage	$V_{OH\ (INT)}$		5.0	5.6		V
Output low level voltage	$V_{OL\ (INT)}$			0.8	1.2	V
Open-loop gain			60			dB
Gain bandwidth product				1.6		MHz
Reference voltage			–5%	$V_{CC}/2$	5%	V
[Crystal Oscillator]						
Crystal oscillator frequency	f_{OSC}	Crystal oscillator	1		10	MHz
External input frequency	f_{CLK}	External signal input	1		10.2	MHz
[S/S Pin]						
Input high level voltage	$V_{IH\ (S/S)}$		4.0	3.05		V
Input low level voltage	$V_{IL\ (S/S)}$			2.60	1.5	V
Hysteresis	ΔV_{IN}			0.45		V
Pull-up resistor	$R_{U\ (S/S)}$			63		kΩ
[F/R Pin]						
Input high level voltage	$V_{IH\ (F/R)}$		4.0	3.05		V
Input low level voltage	$V_{IL\ (F/R)}$			2.60	1.5	V
Hysteresis	ΔV_{IN}			0.45		V
Pull-down resistor	$R_{D\ (F/R)}$		30	50	70	kΩ
[BR Pin]						
Input high level voltage	$V_{IH\ (BR)}$		4.0	3.05		V
Input low level voltage	$V_{IL\ (BR)}$			2.60	1.5	V
Hysteresis	ΔV_{IN}			0.45		V
Pull-down resistor	$R_{D\ (BR)}$		30	50	70	kΩ

Pin Assignment

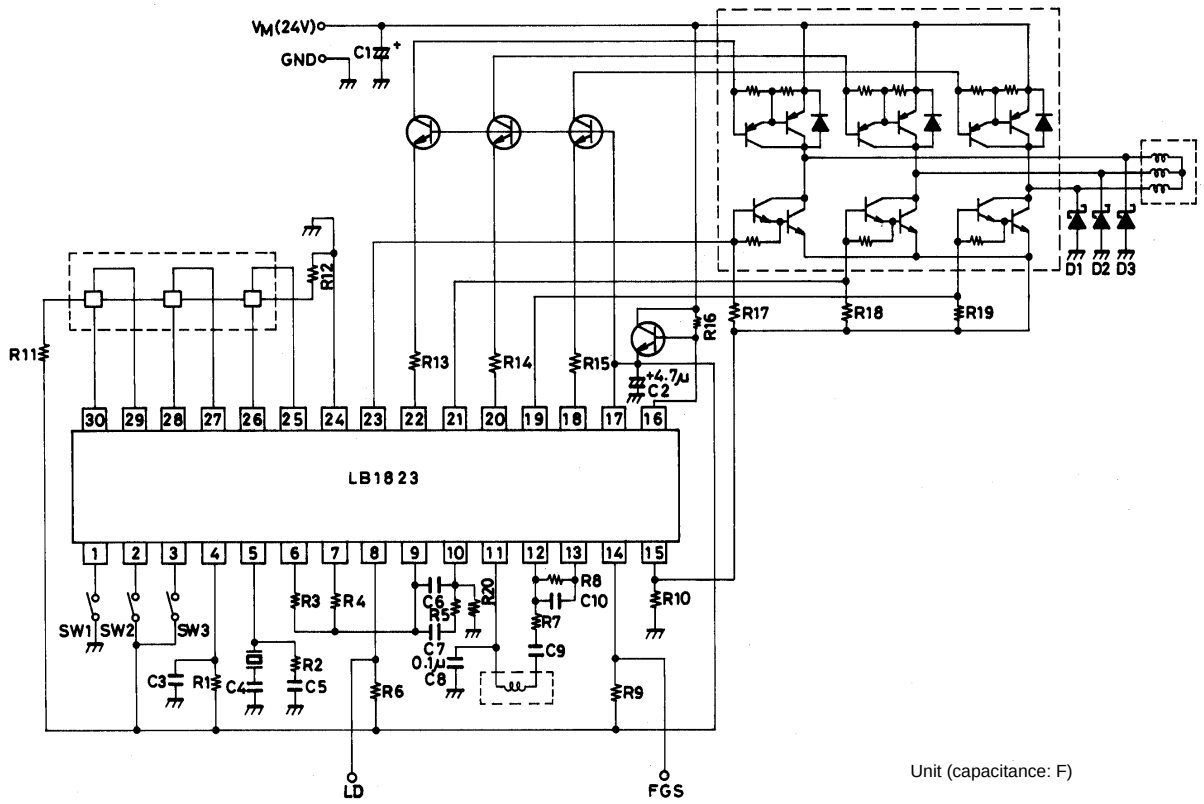


Top view

Block Diagram



Sample Application Circuit



Unit (capacitance: F)

Truth Table

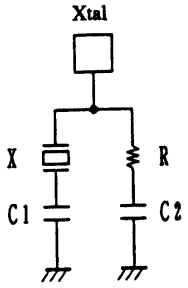
Item	F/R = L			F/R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	Source	Sink
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

Note: High (H) for a given input (IN) specifies the state where $IN^+ > IN^-$.

The formula below gives the relationship between the crystal oscillator frequency (f_{OSC}) and the FG frequency (f_{FG}).

$$f_{FG}\ (\text{servo}) = f_{OSC}/(\text{ECL16 divisor} \times \text{number of counts})$$
$$= f_{OSC}/8192$$

External Crystal Oscillator Circuit



External Constants (reference value, V_{CC} = 6.3 V)

Xtal (MHz)	C1(pF)	C2(pF)	R(Ω)
3 to 4	39	120	390
4 to 5	39	120	560
5 to 7	39	82	820
7 to 10	39	68	2200

External Constants (reference value, V_{CC} = 5 V)

Xtal (MHz)	C1(pF)	C2(pF)	R(Ω)
3 to 4	39	180	330
4 to 5	39	150	390
5 to 7	39	100	560
7 to 10	39	68	1200

Note: However, an oscillator element with crystal fundamental frequency f_O impedance to $3f_O$ impedance ratio = 1:5 or greater must be used.

Pin Functions

Pin No.	Symbol	Function
30, 29 28, 27 26, 25	$IN1^+$, $IN1^-$ $IN2^+$, $IN2^-$ $IN3^+$, $IN3^-$	Hall input pin Hall input pin Hall input pin
19	UH	Output pin, constant current source output
21	VH	Output pin, constant current source output
23	WH	Output pin, constant current source output
18	UL	Output pin, open collector sink output
20	VL	Output pin, open collector sink output
22	WL	Output pin, open collector sink output
17	V_{CC}	Power supply
16	V_{REG}	7 V shunt regulator output
24	GND	Ground
4	CR	PWM oscillator frequency setting
9	INT_{IN}	Integrator input
10	INT_{OUT}	Integrator output (speed control pin)
7	D_{OUT}	Speed discriminator output. High on overspeed.
6	P_{OUT}	PLL output
8	LD	Lock detector Low when the motor speed is in the lock range (±6.25%)
11 12	FG_{IN+} FG_{IN-}	FG pulse input (1/2 of the V_{CC} voltage) FG pulse input
13	FG_{OUT}	FG amplifier output
14	FGS_{OUT}	FG amplifier output (following the Schmitt circuit)
5	X'tal	Crystal oscillator. Connect a crystal oscillator element to this pin.
15	RF	Output current detection
1	S/S	Start/stop control pin Low for start, high or open for stop
2	F/R	Forward/reverse control Low or open for forward, high for reverse
3	BR	Brake, short brake Low or open for start, high for brake. The S/S pin must be set to the stop state when releasing the brake.

External Component Functions

Part	Function	Description
C1	Power supply stabilization	Choose a value such that the voltage fluctuations due to the motor drive currents are stabilized.
C2	IC power supply stabilization	Attach as close as possible to pins 17 and 24.
R1, C3	PWM frequency setting	Use a resistor of 30 kΩ or larger for R1.
C4, C5, R2	External crystal oscillator circuit	See the figure on page 6.
C6, C7, R3, R4, R5	Servo constants	
C8	IC internal power supply stabilization Reset pulse generation	If the capacitance of this capacitor is too small, it will become harder to reset the internal IC logic reliably and incorrect logic operation may occur. Attach as close as possible to pins 11 and 24.
C9, C10, R7, R8	FG amplifier gain and frequency characteristics settings	
R10	Limit current setting	Output current $I_{OUT} = V_{RF}/R10$
R11, R12	Hall element bias current settings	
R13, R14, R15	Sink current settings	These resistors set the sink currents for the UL, VL and WL (open collector) outputs.
R16	Shunt regulator bias current settings	Select a value such that a current of over 1 mA flows in the V_M voltage range for which guaranteed correct operation is desired.
R17, R18, R19	Pull-down resistors	These resistors speed up the motor drive output transistor off times.
R20	Start time assurance	Include R20 in applications in which the start up time is a problem.
D1, D2, D3	Regeneration current absorption	Use Schottky diodes for D1, D2 and D3.

Notes on LB1823 Operation and External Components

1. Speed control circuit
   The LB1823 uses a speed discriminator circuit and a PLL circuit in combination for speed control. The speed discriminator generates an error output once every two FG periods using a charge pump technique. The PLL circuit generates a phase error output once every FG period, also using a charge pump technique. By using a speed discriminator circuit and a PLL circuit together, the LB1823 can suppress speed variations better than earlier systems that only used a speed discriminator for speed control when used with motors faced with large load variations. Since the following formula determines the FG servo frequency, the motor speed is set by the number of FG pulses and the crystal oscillator frequency.
   f_{FG} (servo) = $f_{OSC}/8192$
   f_{OSC}: Crystal oscillator frequency

2. Direct PWM drive
   This IC adopts a direct PWM drive technique to minimize power loss in the outputs. The output transistors are always saturated when on, and the motor drive power is adjusted by changing the duty with which the outputs are on. Since the upper side transistors switch the outputs, Schottky, fast recovery, or similar diodes must be inserted between OUT and ground (diodes D1, D2 and D3). (This is because through currents will flow in the upper side transistors at the instant they turn on if these diodes do not have a short reverse recovery time.) Ordinary rectifying diodes can be used between OUT and V_{CC}. Transistors with no parasitic diodes must be used for the output lower side transistors. If these transistors include parasitic diodes, through currents will flow due to their reverse recovery time, even if Schottky diodes are used for D1, D2 and D3.

3. Current limiter circuit
   The current limiter circuit operates (to limit the peak current) at a current determined by the formula $I = 0.5/R_f$ (where R_f = R10). The limiting operation suppresses the current by reducing the on duty. No phase compensation capacitor is required.

4. Speed lock range
   The speed lock range is ±6.25% of the rated speed, and the LD pin (which is an open collector output) will be low when the motor speed is within the lock range. The LB1823 controls the motor speed to be within the lock range by generating a speed error signal when the motor speed goes out of the lock range and adjusting the motor drive on duty according to that signal.

5. PWM frequency
   The PWM frequency is determined by R1 and C3, which are connected to the CR pin.
   When R1 is connected to a 6.3 V power supply (the application circuit pin 17 voltage):
   $f_{PWM} \approx 1/(0.6 \cdot C \cdot R)$

   R1 must not be any smaller than 30 kΩ. A PWM frequency of 15 kHz is desirable. If the PWM frequency is too low, the motor will resonate at the PWM frequency during motor constraint. This can result in disturbing audible frequency noise. Inversely, the output transistor switching loss can become significant if the PWM frequency is too high.

6. Grounding
   The signal system ground must be separated from the output system ground, and these grounds must be connected to a single ground point at the connector. The output system ground should be kept as short as possible since it carries large current.
   Output system ground – – The R_f (R10) ground side. The D1, D2, and D3 ground side.
   Signal system ground – – The IC pin 24 and the IC peripheral circuit ground.

7. External interface pins
   - LD pin
     Output type: open collector
     Breakdown voltage:8 V
     Manufacturing variation in the saturation voltage (reference value at I_{LD} = 10 mA)
     0.10 to 0.30 V
   - FGS pin
     Output type: open collector
     Breakdown voltage: 8 V
     Manufacturing variation in the saturation voltage (reference value at I_{FGS} = 2 mA)
     0.05 to 0.10 V
     The FGS pin outputs the FG amplifier output converted to a pulse signal by a hysteresis comparator. Thus FGS is a speed monitor output. No pull-up resistor is required when unused.
   - S/S pin
     Input type: PNP transistor base with a 63 kΩ pull-up resistor to V_{CC}
     Threshold level: About 2.6 V (high to low), about 3.05 V (low to high)
     (typical) Hysteresis: about 0.45 V
     In the stop state, power is cut from all but certain circuits (the input, crystal oscillator and divider circuits) and the LB1823 does not operate.
   - F/R pin
     Input type: PNP transistor base with a 50 kΩ pull-down resistor to ground
     Threshold level: About 2.6 V (high to low), about 3.05 V (low to high)
     (typical) Hysteresis: about 0.45 V
     The forward/reverse direction must be switched in the stop state.
   - BR pin
     Input type: PNP transistor base with a 50 kΩ pull-down resistor to ground
     Threshold level: About 2.6 V (high to low), about 3.05 V (low to high)
     (typical) Hysteresis: about 0.45 V
     Braking must be released in the stop mode.

8. FG amplifier
   The FG amplifier gain is determined by R7 and R8, with the DC gain, G, being R8/R7. C9 and C10 determine the FG amplifier frequency characteristics. (R7 and C9 form a high-pass filter and R8 and C10 form a low-pass filter.) Since a Schmitt comparator is connected following the FG amplifier, the components R1, R2, C4 and C5 must be chosen so that the amplitude is at least 250 mVp-p. (It is desirable that the FG output be set up to provide a level of between 1 and 3 Vp-p during steady state motor rotation.)

9. Notes on external capacitors
   - C8
     C8 is required for stabilization of the $FG_{IN}+$ pin constant voltage power supply and to generate the IC internal logic reset pulse. The reset pulse is generated when the $FG_{IN}-$ pin reaches about 1.3 V from 0 V. If the reset does not operate, the LD pin will go on briefly during IC start.
   - C2
     C2 is required for power supply stabilization. Since this IC adopts a PWM technique that switches large output currents, it can generate noise extremely easily. Thus the power supply must be stabilized adequately so that this noise does not cause the IC to operate incorrectly. C2 should be located as close as possible to pins 17 and 24.

10. Notes on external resistors
    - R13, R14 and R15
      These resistors set the external output (source side) transistor drive currents. The drive currents (I_D) can be derived from the following formula.
      $I_D \geq I_{OUT}/h_{FE}$ min
      $I_D = (V_{CC} - 0.7 - V_O \text{ sat})/R$
      I_{OUT}: Maximum output current
      h_{FE} min: Output transistor minimum current amplification factor
      V_O sat: The LB1823 output saturation voltage
    - R16
      R16 sets the shunt regulator bias current. R16 must be selected so that a current of over 1 mA flows in the V_M voltage range for which guaranteed correct operation is desired.
      $R16 \leq (V_M \text{ min} - V_{REG})/1 \text{ mA}$
    - R17, R18 and R19
      R17, R18 and R19 prevent leakage from the lower side output transistors and make the switching time faster.
    - R20
      R20 prevents leakage from the integrator. A value of around 24 kΩ is recommended. If this resistor is not used, the INT OUT pin will go high in stop mode due to leakage currents. Startup is delayed by the integrator external time constant at start time, since the motor is accelerated when the INTOUT pin is low.

11. External transistors
    - Regulator transistor
      Select a transistor with a current capacity of at least 70 mA and a breakdown voltage greater than the largest V_M voltage. Heat generation will be a problem. Use a heat sink or other cooling technique if required.
      $Pd = (V_M \text{ max} - V_{REG}) \times I$
      I: I_{CC} + Hall bias current + output current (source) + α
      When the internal shunt regulator is not used, the power supply must be connected directly to the V_{CC} pin (4.5 to 7 V). The regulator transistor is not required in this case.
      2SC2314 (TO126), 2SD330 (TO220)
      2SC3985 (TO220ML) or similar transistor
    - Output interface transistors
      These transistors are used to assure that high voltages are not applied to the IC. (The total system cost is lower by restricting the IC breakdown voltage.) Select transistors with a current capacity of at least 30 mA and a breakdown voltage greater than the largest V_M voltage. (R13, R14 and R15 determine the currents.)
      2SC4641 (NP), 2SC4640 (SPA)
      2SC4520 (PCP), 2SC4211 (MCP) or similar transistors

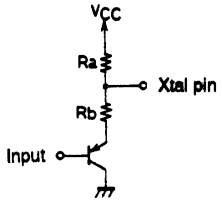
- Output transistors
  The output transistors must be chosen according to the current and breakdown voltage settings determined by the required motor power. Printed circuit board space considerations determine the choice of discrete or driver array components.

Upper side transistors (Darlington)	Lower side transistors	Current	Breakdown voltage
2SA1259	2SD1060	5 A	50 V
2SB881	2SD1061	7 A	50 V
2SB882	2SD1062	10 A	50 V
2SB883	2SD1065	15 A	50 V

The 2SC4070 (SPA) and 2SC4113 (SPA) lower side predriver transistors include an emitter-base resistor. When no resistor is required, the same transistors as used in the output interface can be used.
Driver arrays:
SLA6022 and SLA6023 (Sanken)

12. Through currents due to the direct PWM technique
    In the direct PWM technique through currents flow in the outputs due to the switching, e.g., when used in a discrete structure (including predriver circuits) or in LB1822 applications. These through currents are due to the delays and parasitic capacitances in the output transistors. Although additional capacitors were previously used to deal with this problem, the LB1823 includes circuit modifications to ameliorate through currents. However, even despite these measures, through currents can still occur if the values of R17, R18 and R19 are made too large, since the switching time of the lower side transistors will be increased. Although whiskers of under 10 ns can be seen in the R_f voltage waveform during switching, this will not be a problem. (These occur in the probe and do not correspond to current flows.)

13. Oscillator element
    Normally, a crystal resonator, a resistors, and two capacitors are connected to the LB1823 Xtal pin. A ceramic oscillator could also be used in applications that do not require such precise speed control characteristics. To avoid problems, consult with the manufacturer of the oscillator element when selecting the oscillator element and the values of the external resistor and capacitors used. Use a circuit consisting of resistors and a pnp transistor as shown in the figure to apply an external clock signal (CLK) to the Xtal pin.
    f_{CLK} = 1 to 10.2 MHz
    Input signal levels
    High level voltage: 4.0 V minimum
    Low level voltage: 1.5 V maximum
    Capacitors must be added to this circuit if overshoot and/or undershoot appears in the input waveform. Be sure to check for this condition in that case.



Reference values

V_{CC} = 6.3 V typ (5.8 to 6.8 V)	Ra = 1.5 kΩ	Rb = 2.0 kΩ
V_{CC} = 5.0 V typ (4.5 to 5.5 V)	Ra = 2.0 kΩ	Rb = 1.0 kΩ

14. Servo constants

The servo constant calculation varies significantly with the motor used, and requires specialized know-how. Thus this should be handled by the motor manufacturer. We can provide the IC characteristics data required for the servo constants calculations as well as frequency characteristics simulation data for the filter constants set by the motor manufacturer. If the resistor between D_{OUT} and $INT._{IN}$ (R4) is too small, the values of C6 and C7 will become large. If R4 is too large, speed errors will be likely to occur due to the speed discriminator cutoff current and the integrator input current. Therefore, we think that a value in the range 10 to 100 kΩ is appropriate. If the resistor between P_{OUT} and $INT._{IN}$ (R3) is too small, the influence of the PLL system will be too large and pull-in to lock synchronization will be degraded. Therefore, this resistor should not be too small. (We recommend a value of about 1 MΩ when R4 is 75 kΩ.) First determine the constants for the speed discriminator system only (R4, R5, C6 and C7), and then determine the value of R3 in the PLL system.