



# FAST CMOS BUFFER CLOCK/DRIVER

**IDT49FCT806BT/CT**

## FEATURES:

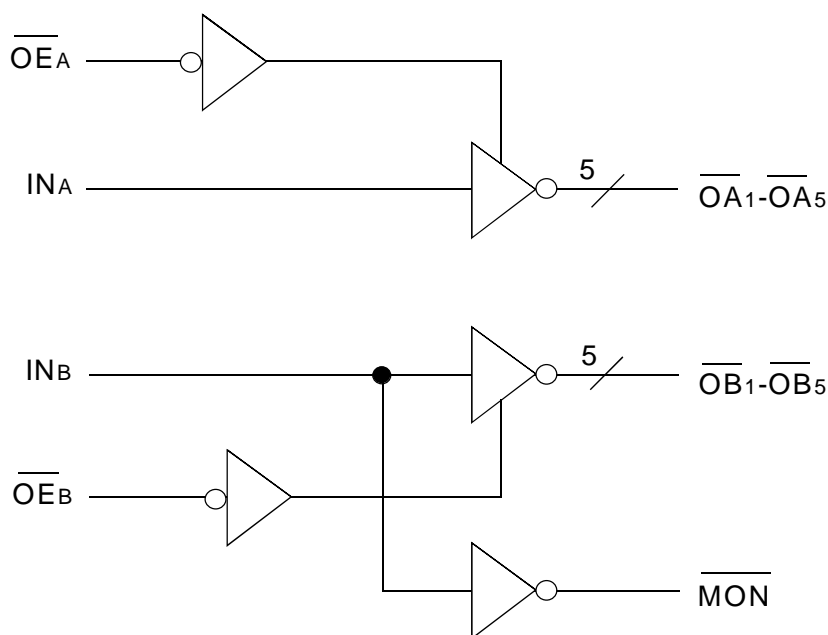
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 600ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: -32mA IOH, +48mA IOL
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in the following packages:
  - Commercial: SOIC, SSOP, QSOP
  - Military: CERDIP, LCC, CERPACK

## DESCRIPTION:

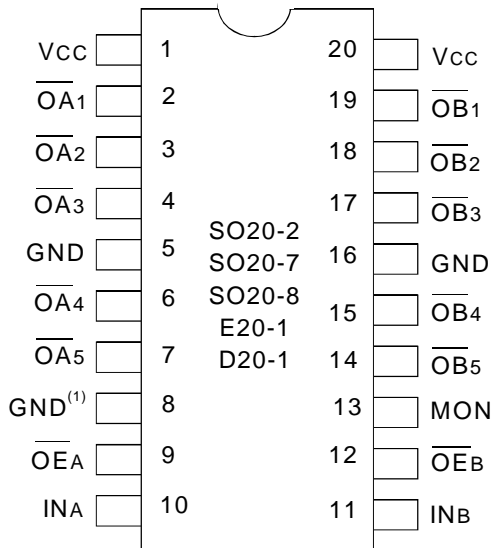
This buffer/clock driver is built using advanced dual metal CMOS technology. The FCT806T is an inverting clock driver consisting of two banks of drivers. Each bank drives five TTL output buffers from a standard TTL compatible input. This part has extremely low output skew, pulse skew, and package skew. The device has a "heart-beat" monitor for diagnostics and PLL driving. The monitor output is identical to all other outputs and complies with the output specifications in this document.

The FCT806T is designed for fast, clean edge rates to provide accurate clock distribution in high speed systems.

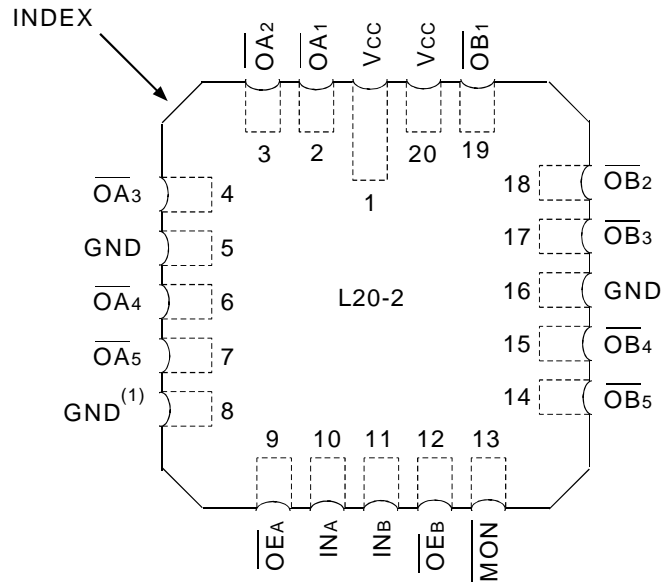
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ CERPACK/ CERDIP  
TOP VIEW



LCC  
TOP VIEW

**NOTE:**

1. Pin 8 is internally connected to GND. To insure compatibility with all products, pin 8 should be connected to GND at board level.

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-65 to +120	mA

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COU	Output Capacitance	VOUT = 0V	5.5	8	pF

**NOTE:**

1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OE}A, \overline{OE}B$	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
$\overline{OA}x, \overline{OB}x$	Clock Outputs
$\overline{MON}$	Monitor Output

## FUNCTION TABLE(1)

Inputs		Outputs	
$\overline{OE}A, \overline{OE}B$	INA, INB	$\overline{OA}x, \overline{OB}x$	$\overline{MON}$
L	L	H	H
L	H	L	L
H	L	Z	H
H	H	Z	L

**NOTE:**

1. H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ :

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current (3-State Output Pins)	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$I_I$	Input HIGH Current	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$		-60	-120	-225	$\text{mA}$
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -12\text{mA MIL}$ $I_{OH} = -15\text{mA COM'L}$	2.4	3.3	—	V
			$I_{OH} = -24\text{mA MIL}$ $I_{OH} = -32\text{mA COM'L}^{(4)}$	2	3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 32\text{mA MIL}$ $I_{OL} = 48\text{mA COM'L}$	—	0.3	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$
$V_H$	Input Hysteresis for all inputs	—		—	150	—	$\text{mV}$
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or $V_{CC}$		—	5	500	$\mu\text{A}$

### NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- Duration of the condition should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/\text{MHz/bit}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_o = 25\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = V_{CC}$ Mon. Output Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.8	4	
		$V_{CC} = \text{Max.}$ Outputs Open $f_o = 50\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Eleven Outputs Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	33	55.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	33.5	57.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH}, \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_o = \text{Output Frequency}$   
 $N_o = \text{Number of Outputs at } f_o$   
 All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (MILITARY)<sup>(1, 2)</sup>

Symbol	Parameter	Condition <sup>(3)</sup>	FCT806BT		FCT806CT		Unit
			Min. <sup>(4)</sup>	Max.	Min. <sup>(4)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay INA to $\overline{OAx}$ , IN <sub>B</sub> to $\overline{OBx}$	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	5.7	1.5	5.2	ns
t <sub>R</sub>	Output Rise Time		—	2	—	2	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(o)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.9	—	0.7	ns
tsk(p)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> –t <sub>PLH</sub>  )		—	0.9	—	0.8	ns
tsk(pp)	Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.2	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\overline{OEa}$ to $\overline{OAx}$ , $\overline{OEb}$ to $\overline{OBx}$		1.5	6.5	1.5	6	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time $\overline{OEa}$ to $\overline{OAx}$ , $\overline{OEb}$ to $\overline{OBx}$		1.5	6.5	1.5	6	ns

### NOTES:

1. t<sub>PLH</sub>, t<sub>PHL</sub>, and tsk(pp) are production tested. All other parameters are guaranteed but not production tested.
2. Propagation delay range indicated by Min. and Max. limit is due to V<sub>cc</sub>, operating temperature, and process parameters. These propagation delay limits do not imply skew.
3. See Test Circuits and Waveforms.
4. Minimum limits are guaranteed but not tested on Propagation Delays.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (COMMERCIAL)<sup>(1, 2)</sup>

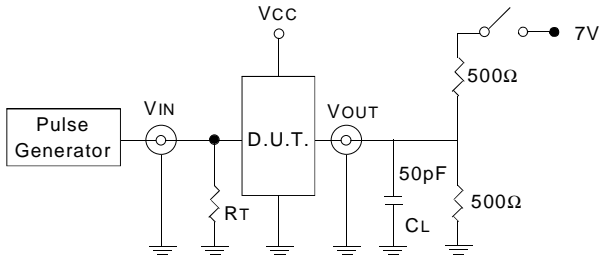
Symbol	Parameter	Condition <sup>(3)</sup>	FCT806BT		FCT806CT		Unit
			Min. <sup>(4)</sup>	Max.	Min. <sup>(4)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay INA to $\overline{OAx}$ , IN <sub>B</sub> to $\overline{OBx}$	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	5	1.5	4.5	ns
t <sub>R</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(o)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.5	ns
tsk(p)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> –t <sub>PLH</sub>  )		—	0.7	—	0.6	ns
tsk(pp)	Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.2	—	1	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\overline{OEa}$ to $\overline{OAx}$ , $\overline{OEb}$ to $\overline{OBx}$		1.5	6	1.5	5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time $\overline{OEa}$ to $\overline{OAx}$ , $\overline{OEb}$ to $\overline{OBx}$		1.5	6	1.5	5	ns

### NOTES:

1. t<sub>PLH</sub>, t<sub>PHL</sub>, and tsk(pp) are production tested. All other parameters are guaranteed but not production tested.
2. Propagation delay range indicated by Min. and Max. limit is due to V<sub>cc</sub>, operating temperature, and process parameters. These propagation delay limits do not imply skew.
3. See Test Circuits and Waveforms.
4. Minimum limits are guaranteed but not tested on Propagation Delays.

## TEST CIRCUITS AND WAVEFORMS

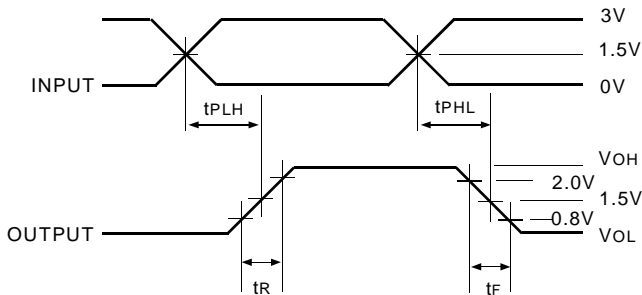
### TEST CIRCUITS FOR ALL OUTPUTS



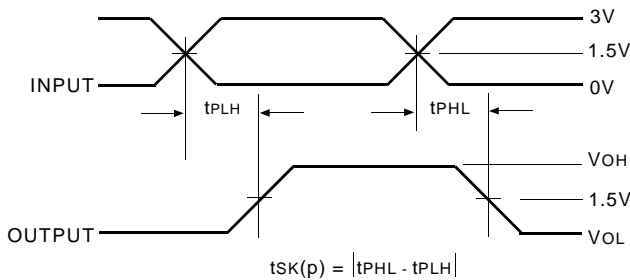
**DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

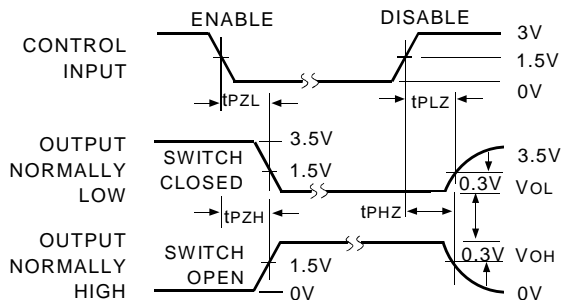
### PACKAGE DELAY



### PULSE SKEW - tsk(p)



### ENABLE AND DISABLE TIMES



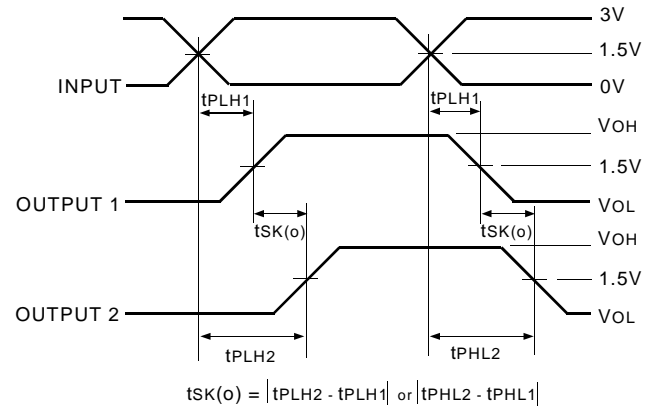
**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tR ≤ 2.5ns; tF ≤ 2.5ns

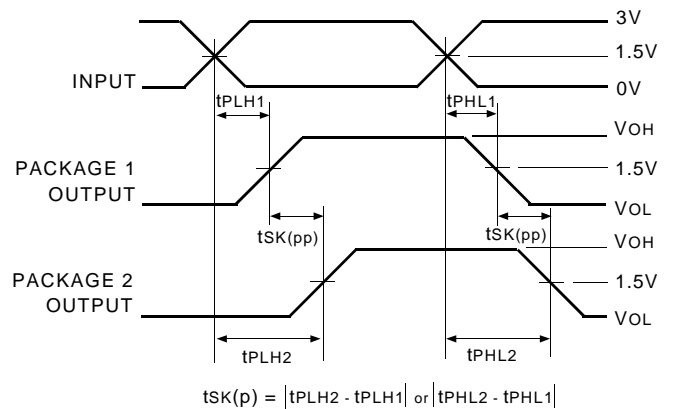
### ENABLE AND DISABLE TIMES SWITCH POSITION

TEST	SWITCH
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

### OUTPUT SKEW



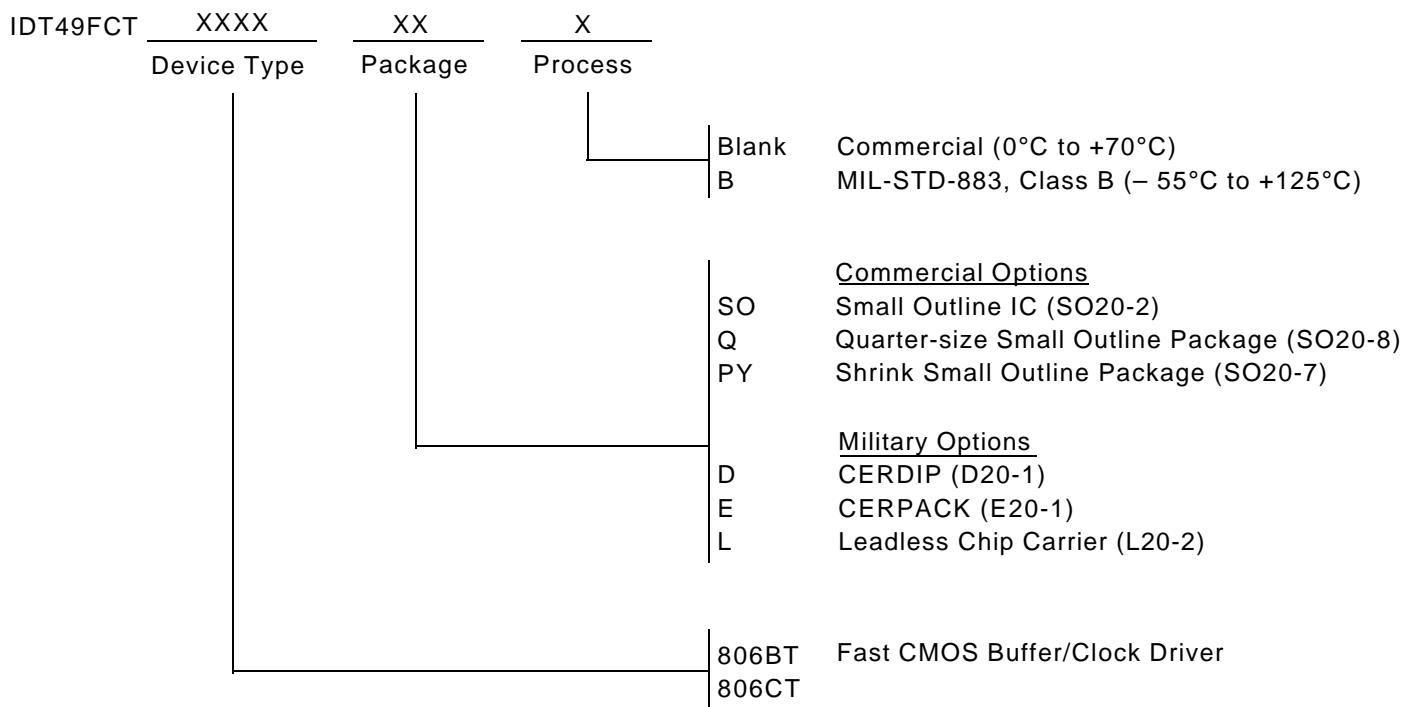
### PART-TO-PART SKEW - tsk(pp)



**NOTE:**

1. Package 1 and Package 2 are same device type and speed grade.

**ORDERING INFORMATION**



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
 www.idt.com\*

\*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.  
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.