TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

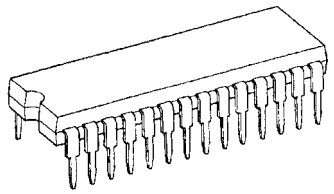
TC90A80N,TC90A80F

3-Line Digital Comb Filter for VCR, YNR/CNR, and Skew Correctors (NTSC)

The TC90A80N/F is a 3-line digital Y/C (luminance/ chrominance) separation IC for VCR.

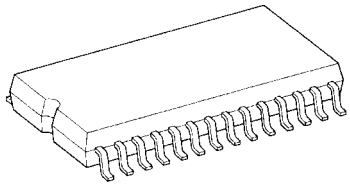
In addition to YNR and CNR used for noise reduction in the playback signal, the IC incorporates skew correctors for special playback. The IC is then suitable for processing S-VHS recorded playback signals.

TC90A80N



SDIP28-P-400-1.78

TC90A80F



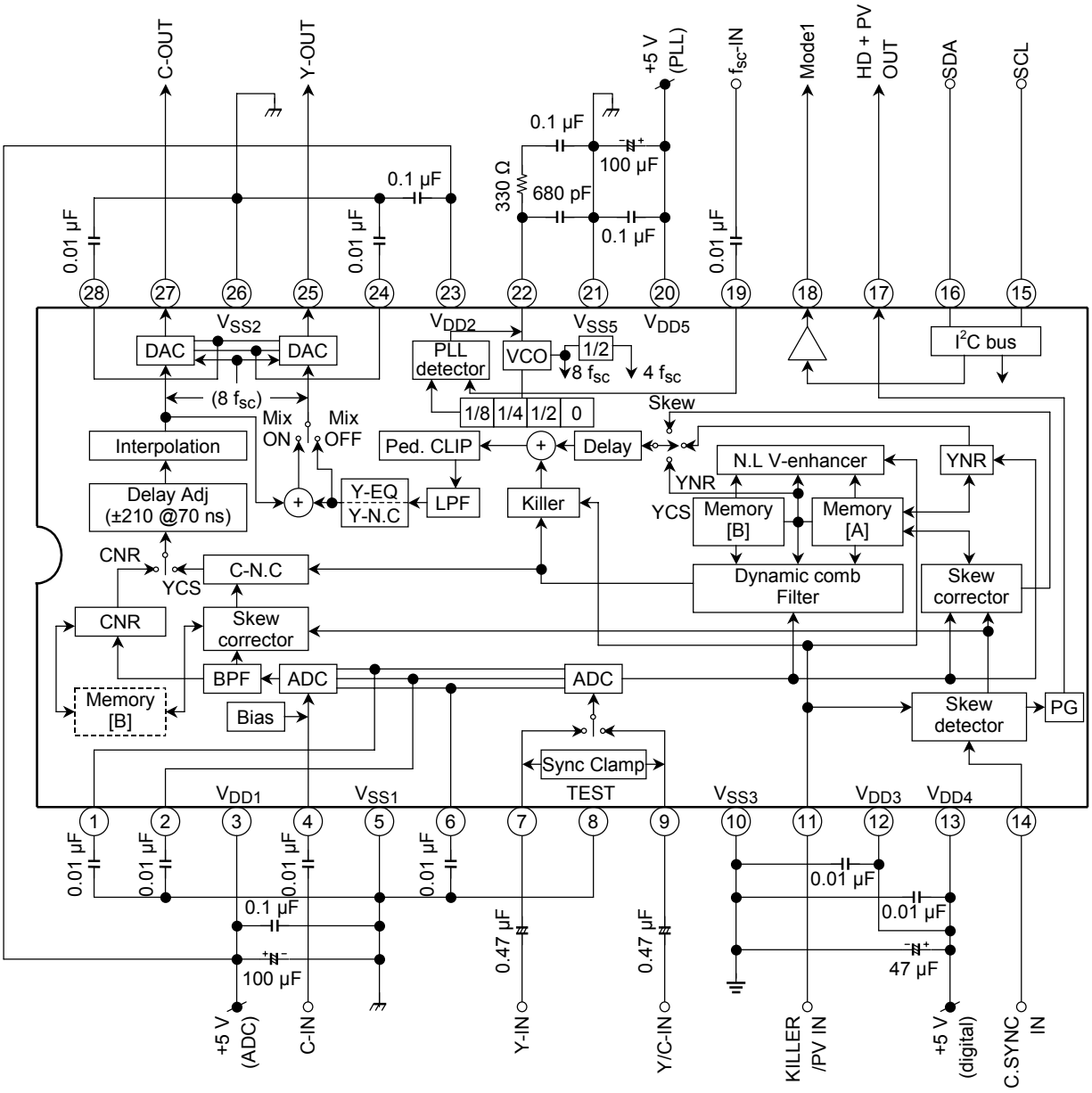
SOP28-P-450-1.27

Weight
SDIP28-P-400-1.78 : 1.7 g (typ.)
SOP28-P-450-1.27 : 0.8 g (typ.)

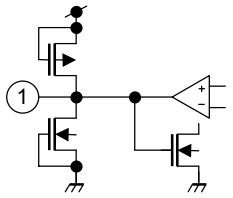
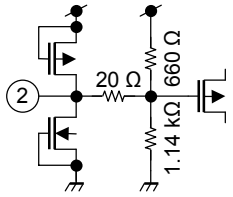
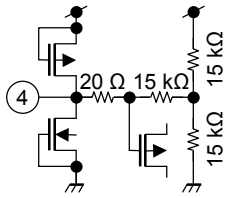
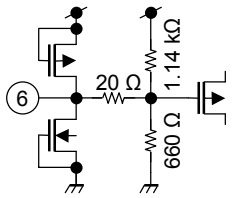
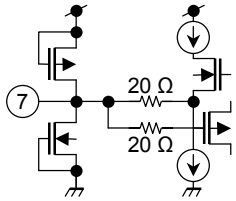
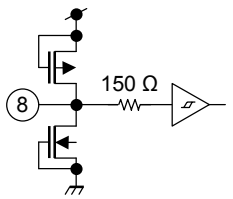
Features

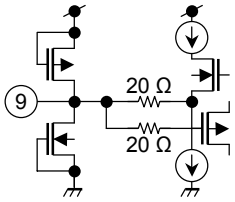
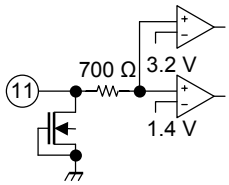
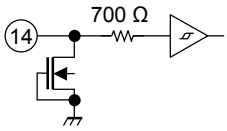
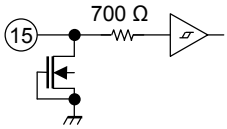
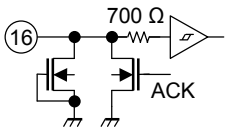
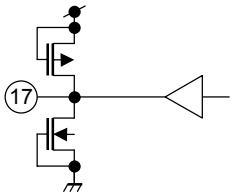
- TV format: NTSC (3.58)
- Dynamic comb filter
- YNR circuit
- CNR circuit
- Luminance signal non-linear vertical edge corrector (with coring function)
- Luminance signal horizontal frequency characteristic corrector (with coring function)
- Luminance signal line noise canceller
- Record/playback input switch circuit (switches between Y/C and Y inputs)
- Y and C input pins, independently one another (Y: sync tip clamp; C: center bias)
- Re-mixer circuit after Y/C sharpness processing
- Skew detector and correctors (NTSC ×5 Mode: in units of 0.2 H)
- PLL detector for switching frequencies (f_{sc}, 2 f_{sc}, 4 f_{sc} and 8 f_{sc} clock inputs)
- 8-bit 4 f_{sc} AD converter (2 channels)
- 10-bit 8 f_{sc} DA converter (2 channels)
- 1-H delay line (2 channels)
- I^2C bus control
- I^2C bus decode output pin (High/Low)
- 5-V single power operation

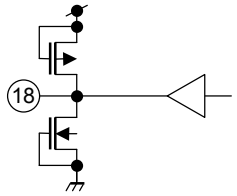
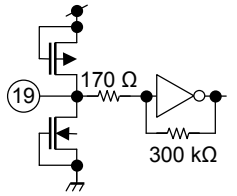
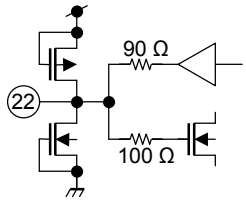
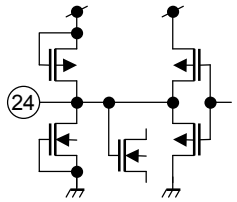
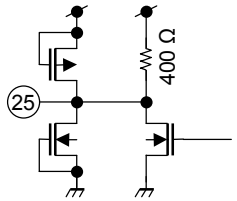
Block Diagram

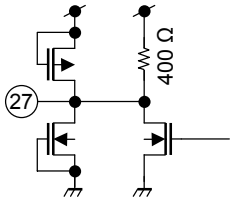
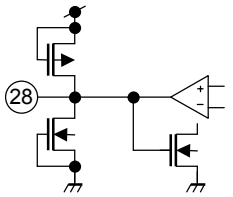


Pin Functions

Pin No.	Pin Name	Function	DC Level (V)	Interface Circuit
1	BIAS	ADC bias pin Connect a 0.01-μF capacitor between this pin and pin 5 (V_{SS1}).	1.3	
2	VRT	ADC bias pin Sets upper limit of range D for ADC. Connect a 0.01-μF capacitor between this pin and pin 5 (V_{SS1}). The output voltage is held at internal level.	3.16	
3	V_{DD1}	ADC power supply pin (analog) Apply the same voltage as that of pin 23 (V_{DD2}).	5.0	Internally connected to pin 23 (V_{DD2}).
4	CIN	Chrominance signal input pin (I^2C Bus function: NR) Because the signal is internally center-biased, it should be applied after cutting the DC component using a capacitor of around 0.01 μF.	2.5	
5	V_{SS1}	ADC GND pin (analog) Set the same voltage as that of pin 26 (V_{SS2}).	0.0	Internally connected to pin 26 (V_{DD2}).
6	VRB	ADC bias pin Sets lower limit of range D for ADC. Connect a 0.01-μF capacitor between this pin and pin 5 (V_{SS1}). The output voltage is held at internal level.	1.83	
7	YIN	Luminance signal input pin (I^2C Bus function: NR) Because sync tip clamp is internally used, the signal should be applied after cutting the DC component using a capacitor of around 0.47 μF.	Sync Tip NR Mode : 1.86 YCS Mode : 1.83	
8	TEST	Pin for reset control and test control when shipping. Reset control: Applying pulse of 10 μs or longer while the pin is at High with power on resets all the I^2C bus settings to 0. For normal use, set the pin to Low.	0.0	

Pin No.	Pin Name	Function	DC Level (V)	Interface Circuit
9	YCIN	Composite video signal input pin (I^2C Bus function: YCS) Because sync tip clamp is internally used, the signal should be applied after cutting the DC component using a capacitor of around 0.47 µF.	Sync Tip YCS Mode : 1.86 NR Mode : 1.83	
10	V_{SS3}	Logic and DRAM GND pin (digital) Separate digital V_{SS} from analog V_{SS}.	0.0	—
11	KIPVIN	Killer control and pseudo vertical pulse (PV) input pin (M or H polarity can be selected using I^2C Bus.) In Killer mode, Y/C separation, vertical enhancer, CNR, and YNR are halted. PV input: Vertical mask signal for detecting skew. Apply PV which is synchronous with input video signal. For normal use, or not in use, set the pin to Low.	3-level input	
12	V_{DD3}	Logic power supply pin (digital) Separate digital V_{DD} from analog V_{DD}.	5.0	—
13	V_{DD4}	DRAM power supply (digital) Separate digital V_{DD} from analog V_{DD}.	5.0	—
14	CSYNCIN	Composite sync pulse input pin for detecting skew Apply sync separation pulse (positive polarity pulse) of the input video signal. When not in use, set to Low.	—	
15	SCL	I^2C bus clock input pin	—	
16	SDA	I^2C bus data input/output pin	—	
17	HDPVOUT	Sync output pin In Skew Correction Mode: Output can be selected as either HD pulse which is synchronous with output video signal or signal mixed with input PV. In modes other than Skew Correction, drives out C Composite sync pulse. Use for later-stage circuit such as 3DNR.	—	

Pin No.	Pin Name	Function	DC Level (V)	Interface Circuit
18	MODE1	MODE1 output pin High or Low output voltage signal can be selected using I^2C bus. Use for controlling peripheral circuits.	—	
19	FSC	Clock input pin Apply sine wave locked to the frequency of the input video burst signal. One of the four frequencies (f_{sc}, $2f_{sc}$, $4f_{sc}$, and $8f_{sc}$) can be selected using I^2C bus.	2.45	
20	V_{DD5}	PLL power supply pin (analog)	5.0	—
21	V_{SS5}	PLL GND pin (analog)	0.0	—
22	FIL	VCO control pin Connect lag-lead filter between this pin and pin 21 (V_{SS5}).	3.0	
23	V_{DD2}	DAC power supply pin (analog) Apply the same voltage as that of pin 3 (V_{DD1}).	5.0	Internally connected to pin 3 (V_{DD1}).
24	V_{B2}	DAC bias 2 pin Connect a 0.01-μF capacitor between this pin and pin 26 (V_{SS2}).	3.4	
25	YOUT	Luminance signal output pin When Y/C Re-Mix Mode is selected using I^2C bus, this pin drives out a composite video signal.	Sync Tip : 2.46	
26	V_{SS2}	DAC GND pin (analog) Set the same voltage as that of pin 5 (V_{SS1}).	0.0	Internally connected to pin 5 (V_{SS1}).

Pin No.	Pin Name	Function	DC Level (V)	Interface Circuit
27	COUT	Chrominance signal output pin When Y/C Re-Mix Mode is selected using I^2C bus, this pin drives out no signal.	3.7	
28	V_{B1}	DAC bias pin 1 Connect a 0.01-μF capacitor between this pin and pin 26 (V_{SS2}).	1.6	

Note 1: Caution regarding external circuits (component allocation) for improving S/N and stabilizing operation:
Power supply pins are paired with GND pins. Read the section on Pin Functions and connect a ceramic capacitor and an electrolytic capacitor directly between power supply and GND pins.
Toshiba recommend using a capacitor of 0.1 μF or more between analog power supply and GND pins. (For digital pins, use a 0.01-μF capacitor.)

IC Control Specifications

- Functions and characteristics of this IC are set using the I²C bus.
- The data transfer format conforms to the Philips I²C bus format.
- When reset signal is applied, the following DATA bits are all cleared to 0.
- Data transfer format

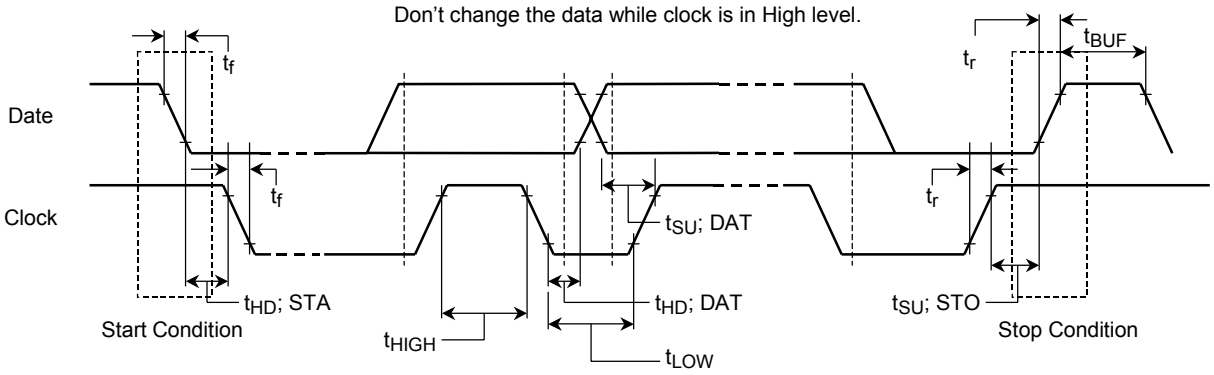
S	Slave address (8 bits)	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	P

Slave address: B4H S: Start condition, A: Acknowledgement, P: Stop condition

- Outline of I²C bus format

  I²C bus transfers data between ICs using two lines: data (SDA) and clock (SCL).
  The I²C bus starts according to the start condition and ends according to the stop condition.
  The start condition is satisfied if SDA changes from High to Low when SCL is High.
  The stop condition is satisfied if SDA changes from Low to High when SCL is High.
  The length of data to be transferred is 8 bits. Data are transferred via the SDA line. An acknowledge (ACK) bit is required after a data byte. The bus line must be pulled up to the power supply level using a resistor. When SCL is High, data must not be changed.

- I²C bus control signal timing



Characteristics	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	100	kHz
Hold time to satisfy start condition	t_{HD}; STA	4.0	—	μs
SCL clock Low period	t_{LOW}	4.7	—	μs
SCL clock High period	t_{HIGH}	4.0	—	μs
Data hold time	t_{HD}; DAT	0	3.45	μs
Data setup time	t_{SU}; DAT	250	—	ns
SDA/SCL signal rise time	t_r	—	1000	ns
SDA/SCL signal fall time	t_f	—	300	ns
Stop condition setup time	t_{SU}; STO	4.0	—	μs
Bus free time between stop and start conditions	t_{BUF}	4.7	—	μs

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

I²C Bus Control Data List

I²C Bus Control List

Slave address: 1011010x

	D7	D6	D5	D4	D3	D2	D1	D0
DATA1	Function	Skew	C-Delay			D-Range	Input Clock	
	0: YCS 1: NR	0: OFF 1: ON	000: ±0 ns 001: −70 010: −140	011: −210 100: ±0 ns 101: +70	110: +140 111: +210	0: 2 V_{p-p} 1: 1 V_{p-p}	00: f_{sc} 01: 2 f_{sc}	10: 4 f_{sc} 11: 8 f_{sc}
DATA2	CNR Gain		CNR Lim.			CNR Corr.	Mode1	Y-EQ/N.C f_o
	00: OFF 01: 0.5	10: 0.625 11: 0.75	000: 1 001: 3 010: 5	011: 7 100: 9 101: 11	110: 13 111: 15	0: ON 1: OFF	0: Low 1: High	0: High 1: Low
DATA3	Y-EQ Gain		Y-EQ/N.C Lim		YNR Corr.	Pulse M/H	Sync Out	Y/C Mix
	00: OFF 01: 0.125	10: 0.25 11: 0.5	00: OFF 01: H2 (L4)	10: H4 (L8) 11: H8 (L14)	0: ON 1: OFF	0: PV 1: Killer	0: HD 1: HD + PV	0: OFF 1: ON
DATA4	V-Emph Gain (YCS)			V-Emph N.L (YCS)			V-Emph Core (YCS)	
	000: OFF 001: +0.25 010: +0.25	011: +0.50 100: +0.75 101: +1.00	110: +1.25 111: +1.50	000: 4 001: 8 010: 12	011: 16 100: 20 101: 24	110: 28 111: 32	00: OFF 01: 1	10: 2 11: 3
	YNR Gain (NR)			YNR Lim (NR)			YNR Mode (NR)	
	000: OFF 001: 0.125 010: 0.25	011: 0.375 100: 0.5 101: 0.625	110: 0.75 111: 0.875	000: 1 001: 3 010: 5	011: 7 100: 9 101: 11	110: 13 111: 15	00: YNR-W 01: YNR-N	10: YCOMB-W 11: YCOMB-N

Description of I^2C Bus Control

(1) Function : Controls input signal and IC functions. (YCS: Y/C-IN → 3 line Y/C separation, NR: Y and C input independently → YNR, CNR)
(2) Skew : Controls skew correction. (OFF: normal mode, ON: Corrects skew every 0.2 H.)
(3) C-Delay : Controls Y/C time. (Switches chroma signal delay time. −: Advances chroma signal. +: Delays chroma signal.)
(4) D-Range : Controls input/output gain. (2 Vp-p: 1 V input 2 V output, Gain = 6dB, 1 Vp-p: 1 V input 1 V output, Gain = 0dB)
(5) Input Clock : Controls clock PLL. (Select input clock.)
(6) CNR Gain : Controls CNR cyclic coefficient/subtraction gain. (OFF: Stops CNR. 0.75: Maximum effect)
(7) CNR Lim. : Controls the CNR limiter. (Limiter level when converting 100 IRE input.: 4 ≈ −31dB to 18 ≈ −18dB)
(8) CNR Corr. : Controls CNR correlation/non-correlation
ON: Controls CNR correlation/non-correlation. → Low vertical color misalignment
OFF: Maximum → effect with vertical color misalignment
(9) Mode1 : Controls parallel output. (Low: Drives out voltage approx. V_{SS}. High: Drives out voltage approx. V_{DD}.)
(10) Y-EQ f_o : Corrects Y frequency characteristic and controls Y-NC bottom frequency. (high: 4/3 f_{sc}, low: f_{sc})
(11) Y-EQ Gain : Controls Y frequency characteristic correction addition gain. (OFF: Stops frequency characteristic correction. 0.5: Corrects by +3dB at 3 MHz.)
(12) Y-EQ/N.C Lim : Controls Y frequency characteristic correction coring level and Y-NC limiter. (OFF: N.C OFF, H*: Limiter level when Y-EQ f_o = high, L*: Limiter level when Y-EQ f_o = low, When converting 100 IRE input, limiter levels are as follows.2: −37dB, 4: −31dB, 8: −25dB, 14: −20dB)
(13) YNR Corr. : Controls YNR correlation/non-correlation
ON: Controls YNR correlation/non-correlation → Low Y vertical color misalignment
OFF: Maximum effect → with Y vertical color misalignment
(14) Pulse Middle/High : Controls High pulse input polarity. (PV: PV with M/H and Killer with Middle/Low, Killer: Killer with M/H and PV with M/L)
PV: Used for vertical-masking PLL for detecting skew and driving out HD + PV when compensating skew.
Killer: Used for controlling separation Off, V-Emph Off in YCS Mode, and YNR/CNR Off in NR Mode.
(15) Sync Out : Controls pulse output in Skew Correction Mode. (HD: Drives out HD which is synchronous with output signal. HD + PV: Mixes PV in HD which is synchronous with to output signal.) HD lock phase is not held (varies from 500 ns to 600 ns).
In modes other than Skew Correction, drives out input C.SYN after delaying approx. 560 ns.
(16) Y/C Mix : Controls Y/C mix output. (OFF: Drives out separated Y and C. ON: Drives out mixed Y and C from the Y output pin. The C output pin is mute.)
(17) V-Emph Gain (YCS): Controls vertical enhancer gain. (OFF: Enhancer Off. +1.5: Maximum effect)
(18) V-Emph N.L (YCS) : Controls vertical enhancer non-linear point. (4: Low effect, 32: Maximum effect)
(19) V-Emph Core (YCS): Controls vertical enhancer coring. (OFF: Coring Off. 3: Emphasizes non correlation of approx. 15 mV or more.)
(20) YNR Gain (NR) : Controls YNR cyclic coefficient/subtraction gain. (OFF: Stops YNR. 0.875: Maximum effect)
(21) YNR Lim (NR) : Controls the YNR limiter. (Limiter level when converting 100 IRE input.: 1 ≈ −43dB~15 ≈ −19dB)
(22) YNR Mode (NR) : Controls YNR and Y-COMB bandwidths. (*-W: Wideband, *-N: Narrowband)
(Note that the controls of DATA4 D7 to DATA4 D0 vary according to the setting of DATA1 D7 (function).)

Functions

Bus Setting		Function														
Function	Skew	Y/C Sep	C-Delay	Drang	CK Select	CNR	YNR	Y-EQ/NC	V-Emph	Skew	Killer	P-M/H	Sync output	Y/C MIX	Y-OUT	C-OUT
YCS (composite video signal input)	OFF	3 Line Comb Sep	O	O	O	△ C-N.C	×	O	O	×	O	O	C.Sync	OFF	Y	C
														ON	Y/C	Mute
	ON	BPF Sep	O	O	O	△ C-N.C	×	O	O	O	O	O	HD·PV	OFF	Y	C
														ON	Y/C	Mute
NR (Y and C input independently)	OFF	×	O	O	O	O	O	O	×	×	O	O	C.Sync	OFF	Y	C
														ON	Y/C	Mute
	ON	×	O	O	O	△ C-N.C	×	O	×	O	O	O	HD·PV	OFF	Y	C
														ON	Y/C	Mute

O: Specified, ×: Not specified

Description of Functions

(1) 3-line Y/C separation circuit (VTR Record Mode)
Provides clear Y and C separation using a dynamic comb filter, which logically extracts the chrominance signal, based on the result of detecting vertical 3-line non correlation using two 1-H delay lines.
Also incorporates a vertical edge enhancer with coring function, which produces a clearer record signal with suppressed noise.

(2) YNR and CNR circuits (VTR Playback Mode)
Independently incorporates cyclic noise reduction using 1-H delay lines for Y and C, effectively reducing vertical non-correlation noise in the playback signal.

(3) Skew corrector (Special Playback Mode for VHS VTR ×5 speed videotape)
From composite sync pulse signal (sync separation output) detects horizontal skew in units of 0.2 H (×2 = 0.4 H before and after Cue/Rev noise bar) generated at special playback of VHS VTR ×5 speed videotape. Using the detection result, automatically corrects horizontal skew included in the input playback video signal by switching the delay time for line memory.
This function can be used for both composite video signals and independently-applied Y and C signals.

1) Pseudo vertical (PV) signal and composite signal necessary for detecting skew
Based on the reference signal of the horizontal frequency generated from the input composite sync signal, detects the position of input sync signal in units of 0.2 H. Because skew is detected due to the noise included in the input composite signal, apply the composite sync signal from which noise is reduced to some extent at sync separation (no filter in the IC).
Note that erroneous skew detection around the period where vertical sync signal is included can be prevented by halting skew detection and by setting PLL to the f_h as reference during the PV pulse period. So, apply pseudo vertical signal.

2) Supplementary function: pin 17 (HDPVOUT)
In Skew Correction Mode, pin 17 drives out the HD pulse (width: approx. 4 μs) which synchronizes with the video signal after skew correction; in modes other than Skew Correction, pin 17 drives out the input composite sync signal. Pin 17 can also be used for output with the input PV mixed using the I^2C bus (in Skew Correction Mode only). Use pin 17 for later-stage circuit such as 3DNR. Note, however, that since the HD lock position and jitter performance are not designed for high precision, do not use pin 17 directly for circuits requiring high precision.

3) Recommended use conditions (eg, search speed)
Since the skew amount is not the same for Cue/Rev with ×5 speed tape, depending on the search speed, after skew correction, horizontal synchronization may become inconsistent at junctions between fields. As a result, the time for each field differs and vertical synchronization degrades.
To avoid this phenomenon, it is necessary to select a search speed where four types of skew comprise a cycle during a 1-V pulse period (excluding PV pulse period). Consider a search speed with no or not much degradation of vertical synchronization, paying attention to the position of the noise bar.
(Example): In ×11 Cue Mode, skew for the 1-V pulse period consists of Skew 0 H → noise → skew 0.4 H → noise → skew 0.8 H → noise → skew 0.2 H → noise → skew 0.6 H → noise → skew 0 H. Where, consistency of horizontal synchronization is maintained. Degradation of vertical synchronization can also be made less conspicuous visually by increasing the search speed.

Maximum Rating (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}	V_{SS} + 6.0	V
Input voltage		V_{IN}	V_{SS} − 0.3 to V_{DD} + 0.3	V
Potential difference between power supply pins (Note 2)		V_{DG}	0.4	V
Power dissipation (Note 3)	TC90A80N	P_D	900	mW
	TC90A80F		600	
Storage temperature		T_{stg}	-55 to +125	°C

Note 2: Connect pin 3 to pin 23. The potential difference among all power supply pins, 3 (23), 12, 13, and 20, must not exceed 0.4 V.
The potential difference among V_{SS} pins 5, 10, 21, and 26 must not exceed 0.01 V.

Note 3: Ta = 75°C for TC90A80F mounted on a PCB (70 mm × 70 mm × 1.6 mm)

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Potential difference between pins 3 and 23 (Note 4)	V_{DG1}	—	0	0.04	V
Potential difference among power supply pins 3,12, 13, and 20	V_{DG2}	—	0	0.15	V
Potential difference among V_{SS} pins 5, 10, 21, and 26	V_{SG}	—	0	0.01	V
Input voltage	V_{IN}	0	—	V_{DD}	V
Operating temperature	T_{opr}	−10	—	75	°C

Note 4: Since power supply pins 3 and 23 are connected in the IC, supply power to them at the same voltage. If there is a large potential difference between the pins, a large current flows through the IC causing degradation or damage due to heat stress.

Maximum ratings: A set of specified parameter values which must not be exceeded during operation, even for an instant. If any of these limit values is exceeded during operation, it causes permanent damage to the TC90A80N/F. Therefore, care must be exercised that the TC90A80N/F operates within the specified ranges.

Recommended operating conditions: Minimum, typical and maximum values for key operating parameters such as supply voltage, DC voltage and operating temperature. Ensuring that the parameter values remain within these specified ranges during operation will help to ensure that the integrity of the TC90A80N/F is not compromised. When designing video equipment, be aware that the TC90A80N/F can function within the recommended operating ranges.

Electrical Characteristics

DC Characteristics

(Ta = 25°C, V_{DD} = 5.00 V, clock input: 3.579545 MHz, 0.5 V_{p-p}, I^2C BUS: according to test conditions)

Characteristics	Pin No.	Pin Name	Symbol	Min	Typ.	Max	Unit	Test Conditions (Remarks)				
								I^2C bus setup	DATA1	DATA2	DATA3	DATA4
Power supply	3, 12, 13, 20, 23	V_{DD}	I_{DD}	60	85	105	mA	I^2C bus setup	0 0	0 0	0 0	0 0
								• Input signal : Apply NTSC color bar at 1-Vp-p to pin 9. • Test content : Measure the total current of power supply pins 3, 12, 13, 20, and 23.				
Pin voltage	1	BIAS	V_1	0.9	1.3	1.7	V	I^2C bus setup	0 0	0 0	0 0	0 0
	2	VRT	V_2	3.02	3.16	3.30	V	• Input signal : Not apply to pins 4, 7, and 9. • Test content : Measure the DC voltage of those pins.				
	4	CIN	V_4	2.4	2.5	2.6	V					
	6	VRB	V_6	1.69	1.83	1.97	V					
	7	YIN	V_7	1.69	1.83	1.97	V					
	9	YCIN	V_9	1.72	1.86	2.00	V					
	19	FSC	V_{19}	2.00	2.45	2.90	V					
	22	FIL	V_{22}	1.8	3.0	4.2	V					
	24	V_{B2}	V_{24}	3.0	3.4	3.8	V					
	25	YOUT	V_{25}	2.37	2.5	2.63	V					
	27	COUT	V_{27}	3.52	3.7	3.88	V					
	28	V_{B1}	V_{28}	1.2	1.6	2.0	V					
3-level input voltage	11: KIPVIN		V_{IML}	V_{SS}	—	1.0	V	I^2C bus setup	4 0	0 0	0 2	0 0
								• Input signal : Apply NTSC color bar at 1-Vp-p to pin 9. • Test content : Apply DC voltage to pin 11 and measure the DC voltage change at the following points. V_{IML} : Normal operation V_{IMM} : Stops Y/C separation (drives out composite video signal to pin 25). V_{IMH} : Receives PV (drives out High (V_{OH}) to pin 17). Operations of V_{IMM} and V_{IMH} are inverted by DATA3 D2 = 1 of the I^2C bus settings. To support high-speed pulse input, the circuit must have no hysteresis				
			V_{IMM}	1.8	—	2.8	V					
			V_{IMH}	3.6	—	V_{DD}	V					
2-level input voltage	8 : TEST 14: CSYNCIN 15: SCL 16: SDA		V_{IH}	4	—	V_{DD}	V	I^2C bus setup	0 0	0 2	0 0	0 0
								• Test content : Apply DC voltage to pins 8, 14, 15, and 16. Change the DC voltage and check the point where High/Low level is applied to those pins by monitoring the DC change on pins 17 and 18. Measure the input bottom voltage of the pins 8, 14, 15 and 16. V_{IH} : Apply reset signal, composite sync signal, I^2C bus High level. V_{IL} : Apply reset signal, composite sync signal, I^2C bus Low level.				
			V_{IL}	V_{SS}	—	1	V					

Output voltage	17: HDPVOUT 18: MODE1		V_{OH}	4.6	—	V_{DD}	V	I^2C bus setup	0 0	0 0	0 0	0 0
								I^2C bus setup	0 0	0 2	0 0	0 0
			V_{OL}	V_{SS}	—	0.4	V	• Test content : Measure the output voltage on pins 17 and 18 when DC is applied with a 4.7-kΩ resistor. V_{OH} : Connects a 4.7-kΩ resistor between pin 17/18 and GND. V_{OL} : Connects a 4.7-kΩ resistor between pin 17/18 and V_{DD}.				
	16	SDA	V_{ACK}	V_{SS}	—	0.4	V	I^2C bus setup	0 0	0 0	0 0	0 0
								• Test content : Measure the ACK output voltage when DC is applied with a 4.7-kΩ resistor. Connect a 4.7-kΩ resistor between pin 16 and V_{DD}.				

AC Characteristics

Luminance signal input/output characteristics

(Ta = 25°C, V_{DD} = 5.00 V, clock input: 3.579545 MHz, 0.5 V_{p-p}, I^2C bus: according to test conditions)

Characteristics	Symbol	Min	Typ.	Max	Unit	Test Conditions (Remarks)				
						I^2C bus setup	DATA1	DATA2	DATA3	DATA4
Recommended input level	V_{YIN}	—	1.0	1.3	V	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : Apply white 100% signal to pins 7 and 9.				
Low-frequency gain	GY	5.5	6.0	6.5	dB	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : Apply white 100% signal at 1-Vp-p to pin 9.				
						• Test content : Compare pin 25 output level with pin 9 input level.				
Comb characteristic	Ycom	40	45	—	dB	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : Apply 1-Vp-p, 2.5-V DC offset sine wave to pin 9.				
						• Test content : Monitor pin 25. Change input frequency. Measure gain difference between 3.51678 MHz and 3.579545 MHz.				
Frequency characteristic	FY	−2	−1	0	dB	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : Apply 1-Vp-p, 2.5-V DC offset sine wave to pin 9.				
						• Test content : Monitor pin 25 in Killer Mode. Change input frequency. Measure gain difference between 0.5 MHz and 3 MHz.				
Differential error	L	−1	0	+1	LSB	(reference value)				
Integral error	B	−3	0	+3	LSB	(reference value)				
Output impedance	Zy	250	400	700	Ω	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : Input 1-Vp-p, 15-kHz square wave to pin 9.				
						• Test content : Calculate output impedance, AC applied with/without 300-Ω resistor connected between pin 25 and GND.				
Fundamental clock leakage	L_{1fy}	—	0.3	1.0	mVrms	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : No input to pin 9.				
						• Test content : Measure f_{SC} (3.579545 MHz) component of pin 25.				
Clock leakage 1	L_{4fy}	—	4	—	mVrms	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : No input to pin 9.				
						• Test content : Measure 4 f_{SC} (14.31818 MHz) component of pin 25.				
Clock leakage 2	L_{8fy}	—	20	—	mVrms	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : No input to pin 9.				
						• Test content : Measure 8 f_{SC} (28.63636 MHz) component of pin 25.				

Chrominance signal input/output characteristics
(Ta = 25°C, V_{DD} = 5.00 V, clock input: 3.579545 MHz, 0.5 V_{p-p}, I^2C bus: according to test conditions)

Characteristics	Symbol	Min	Typ.	Max	Unit	Test Conditions (Remarks)				
						I^2C bus setup	DATA1	DATA2	DATA3	DATA4
Recommended input level	V_{CIN}	—	1.0	1.3	V	I^2C bus setup	8 0	0 0	0 0	0 0
						• Input signal : Apply chroma 100% signal to pin 4. (To pin 4, chrominance signal only; to pin 9, composite video signal)				
Chrominance signal gain	GC	4.5	5.2	5.8	dB	I^2C bus setup	0 0	0 0	0 0	0 0
						I^2C bus setup	8 0	0 0	0 0	0 0
						• Input signal : Apply chroma 100%, 0.714-Vp-p signal to pins 4 and 9. (To pin 4, chrominance signal only; to pin 9, composite video signal)				
						• Test content : Compare pin 27 output level with input level.				
Comb characteristic	Ccom	35	40	—	dB	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : Apply 0.714-Vp-p, 2.5-V DC offset sine wave to pin 9.				
						• Test content : Monitor pin 27. Change input frequency. Measure gain difference between 3.57168 MHz and 3.579545 MHz.				
BPF frequency characteristic	BWC	−0.5	−0.2	0	dB	I^2C bus setup	8 0	0 0	0 0	0 0
						• Input signal : Apply 0.714-Vp-p sine wave to pin 4.				
						• Test content : Monitor pin 27. Change input frequency. Measure gain difference between 3.579545 MHz and 3.079545 MHz.				
Differential gain	DG	0	2	5	%	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : Apply 1-Vp-p, 5-step staircase (0 = 40 IRE) to pin 9.				
Differential phase	DP	0	2	5	°	• Test content : Monitor pin 27 using vector scope (p-p value).				
Output impedance	Zc	250	400	700	Ω	I^2C bus setup	8 0	0 0	0 0	0 0
						• Input signal : Apply 1-Vp-p chroma 100% signal to pin 4.				
						• Test content : Calculate output impedance, AC applied with/without 300-Ω resistor connected between pin 27 and GND.				
Fundamental wave clock leakage	L_{1fc}	—	0.3	1.0	mVrms	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : No input to pin 9.				
						• Test content : Measure f_{SC} (3.579545 MHz) component of pin 27.				
Clock leakage 1	L_{4fc}	—	4	—	mVrms	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : No input to pin 9.				
						• Test content : Measure $4f_{SC}$ (14.31818 MHz) component of pin 27.				
Clock leakage 2	L_{8fc}	—	20	—	mVrms	I^2C bus setup	0 0	0 0	0 0	0 0
						• Input signal : No input to pin 9.				
						• Test content : Measure $8f_{SC}$ (28.63636 MHz) component of pin 27.				

YNR Characteristics

(Ta = 25°C, V_{DD} = 5.00 V, clock input: 3.579545 MHz, 0.5 V_{p-p}, I^2C bus: according to test conditions)

Characteristics	Symbol	Min	Typ.	Max	Unit	Test Conditions (Remarks)				
						I^2C bus setup	DATA1	DATA2	DATA3	DATA4
Y comb characteristic 1	YNRW1	—	−23	−20	dB	I^2C bus setup	8 0	0 0	0 8	F C
						• Input signal : Apply 71.3 mVp-p, 2.5-V DC offset sine wave to pin 7. • Test content : Monitor pin 25. Change input frequency. Measure gain difference between 629.36 kHz and 621.493 kHz.				
Y comb characteristic 2	YNRN1	—	−20	−17	dB	I^2C bus setup	8 0	0 0	0 8	F D
						• Input signal : Apply 71.4 mVp-p, 2.5-V DC offset sine wave to pin 7. • Test content : Monitor pin 25. Change input frequency. Measure gain difference between 629.36 kHz and 621.493 kHz.				
Y comb characteristic 3	YCOBW1	—	−9	−7	dB	I^2C bus setup	8 0	0 0	0 8	F E
						• Input signal : Apply 71.4 mVp-p, 2.5-V DC offset sine wave to pin 7. • Test content : Monitor pin 25. Change input frequency. Measure gain difference between 629.36 kHz and 621.493 kHz.				
Y comb characteristic 4	YCOBN1	—	−12	−10	dB	I^2C bus setup	8 0	0 0	0 8	F F
						• Input signal : Input 71.4 mVp-p, 2.5-V DC offset sine wave to pin 7. • Test content : Monitor pin 25. Change input frequency. Measure gain difference between 629.36 kHz and 621.493 kHz.				

CNR Characteristic

(Ta = 25°C, V_{DD} = 5.00 V, clock input: 3.579545 MHz, 0.5 Vp-p, I^2C bus: according to test conditions)

Characteristics	Symbol	Min	Typ.	Max	Unit	Test Conditions (Remarks)				
						I^2C bus setup	DATA1	DATA2	DATA3	DATA4
C comb characteristic	CNR	—	−14	−12	dB	I^2C bus setup	8 0	F C	0 0	0 0
						• Input signal : Apply 71.4 mVp-p, 2.5-V DC offset sine wave to pin 4. • Test content : Monitor pin 27. Change input frequency. Measure gain difference between 3.579545 MHz and 3.571678 MHz.				

PLL characteristic

(Ta = 25°C, V_{DD} = 5.00 V, clock input: according to test conditions, I^2C bus: according to test conditions)

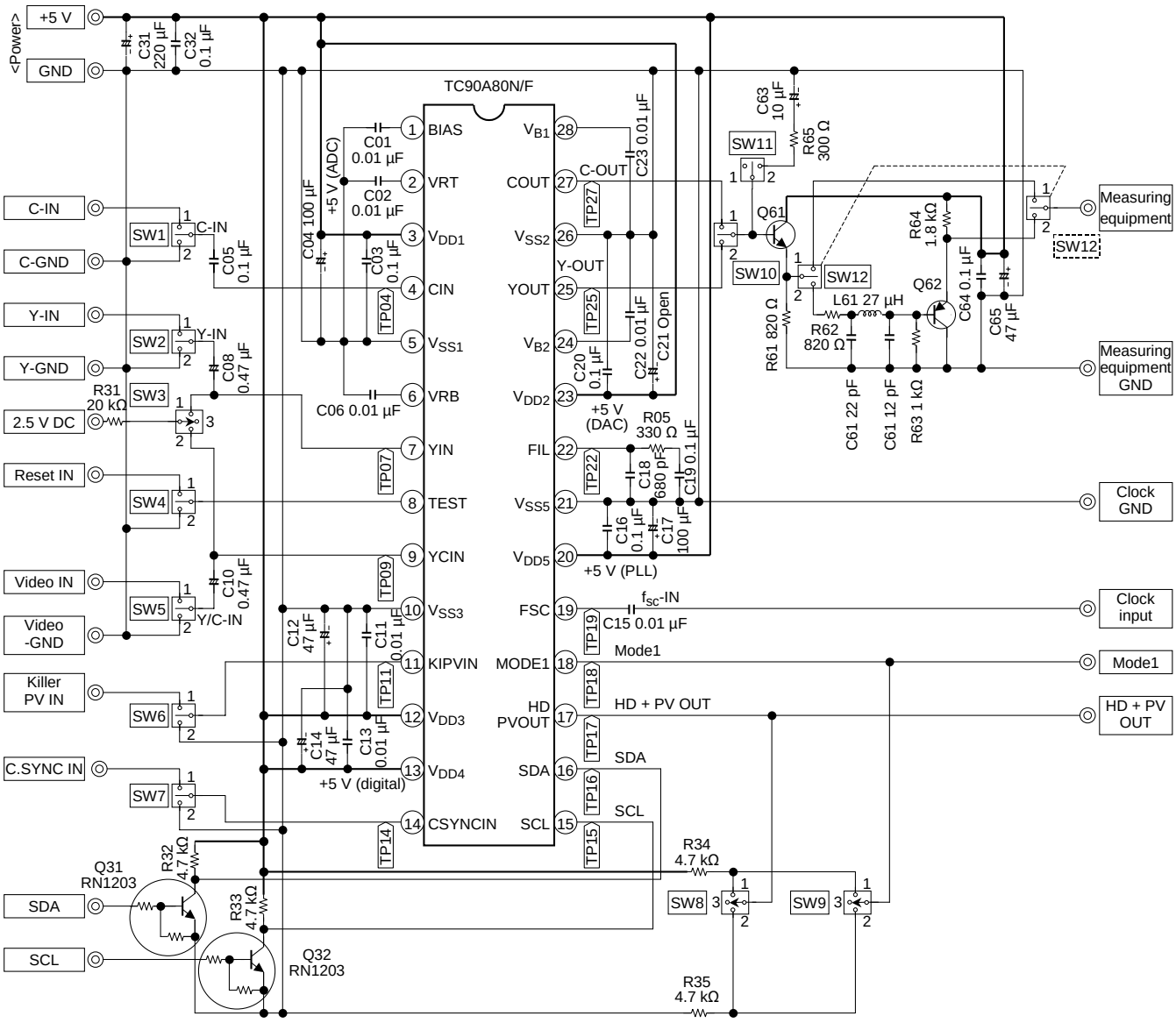
Characteristics	Symbol	Min	Typ.	Max	Unit	Test Conditions (Remarks)				
						I^2C bus setup	DATA1	DATA2	DATA3	DATA4
Pull-in frequency range	Δf_{ckN}	±100	—	—	kHz	I^2C bus setup	0 0	0 0	0 0	0 0
						• Clock input : Change input frequency at 0.5 Vp-p. • Test content : Change input frequency with f_{sc} (3.579545 MHz) as reference and measure pull-in range for PLL.				
Operating input amplitude 1	V_{ck}	0.3	0.5	2.0	V_{p-p}	I^2C bus setup	0 0	0 0	0 0	0 0
						• Clock input : Change input amplitude at f_{sc} (3.579545 MHz). • Test content : Increase input clock amplitude from 0 Vp-p and measure input amplitude for PLL.				
						I^2C bus setup	0 1	0 0	0 0	0 0
						• Clock input : Change input amplitude at 2 f_{sc} (7.15909 MHz). • Test content : Increase input clock amplitude from 0 Vp-p and measure input amplitude for PLL.				
						I^2C bus setup	0 2	0 0	0 0	0 0
						• Clock input : Change input amplitude at 4 f_{sc} (14.31818 MHz). • Test content : Increase input clock amplitude from 0 Vp-p and measure input amplitude for PLL.				
Operating input amplitude 2	V_{ck8}	0.5	1.0	2.0	V_{p-p}	I^2C bus setup	0 3	0 0	0 0	0 0
						• Input signal : Apply 10-kHz, 1-Vp-p triangular wave to pin 9. • Clock input : Change input amplitude at 8 f_{sc} (28.63636 MHz). • Test content : Increase input clock amplitude from 0 Vp-p and measure input amplitude where pin 25 output stabilizes.				

HD Reference Characteristics

(Ta = 25°C, V_{DD} = 5.00 V, clock input: 3.579545 MHz, 0.5 V_{p-p}, I^2C bus: according to test conditions)

Characteristics	Symbol	Min	Typ.	Max	Unit	Test Conditions (Remarks)				
						I^2C bus setup	DATA1	DATA2	DATA3	DATA4
HD output pulse width	HDW	—	4.4	—	µs	I^2C bus setup	4 0	0 0	0 0	0 0
						• Input setting : pin 11 = 0 V, pin 14 = 0 V • Test content : Measure HD pulse width of pin 17.				
HD free-running frequency	HDF	—	15.734	—	kHz	I^2C bus setup	4 0	0 0	0 0	0 0
						• Input setting : pin 11 = 5 V, pin 14 = 0 V • Test content : Measure HD frequency of pin 17.				
HD pull-in frequency range	HDPU	—	±280	—	Hz	I^2C bus setup	4 0	0 0	0 0	0 0
						• Input setting : Set pin 11 to 0 V, and apply pulse signal whose High period is 4 µs and amplitude is 5 V (increase from 0 V to 5 V) to pin 14. Change input frequency. • Test content : Change input frequency with f_h (15.734 kHz) as reference and measure pull-in range where HD frequency of pin 17 locks to the input frequency.				
Minimum input sync pulse width	HD	—	300	—	ns	I^2C bus setup	4 0	0 0	0 0	0 0
						• Input setting : Set pin 11 to 0 V, and apply f_h (15.734 kHz) pulse signal whose amplitude is 5 V (increase from 0 V to 5 V) to pin 14. Change High period of input pulse. • Test content : Increase input pulse width from 50 ns and measure input pulse width where HD frequency of pin 17 locks to f_h.				

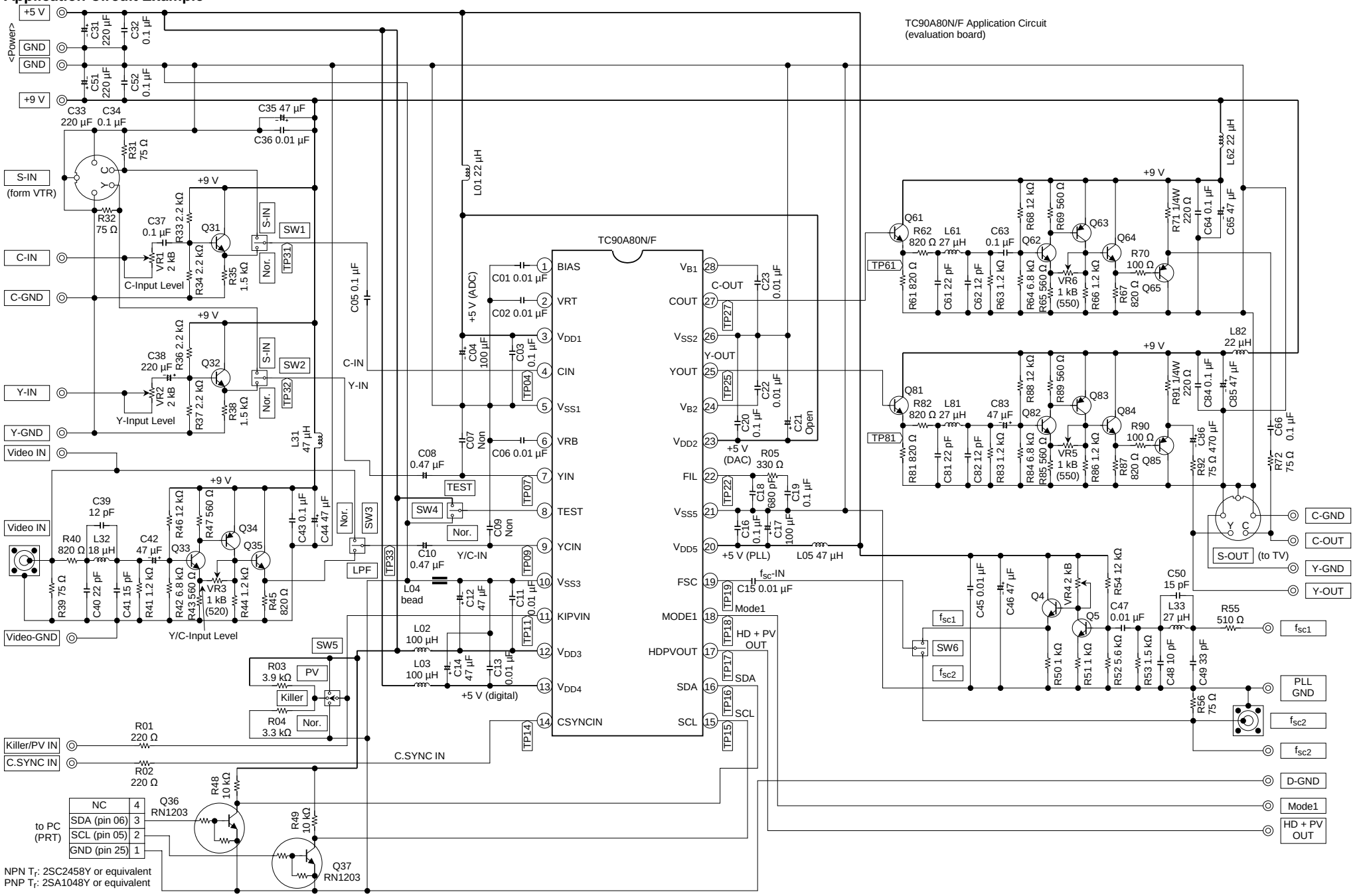
Test Circuit



SW Control Table

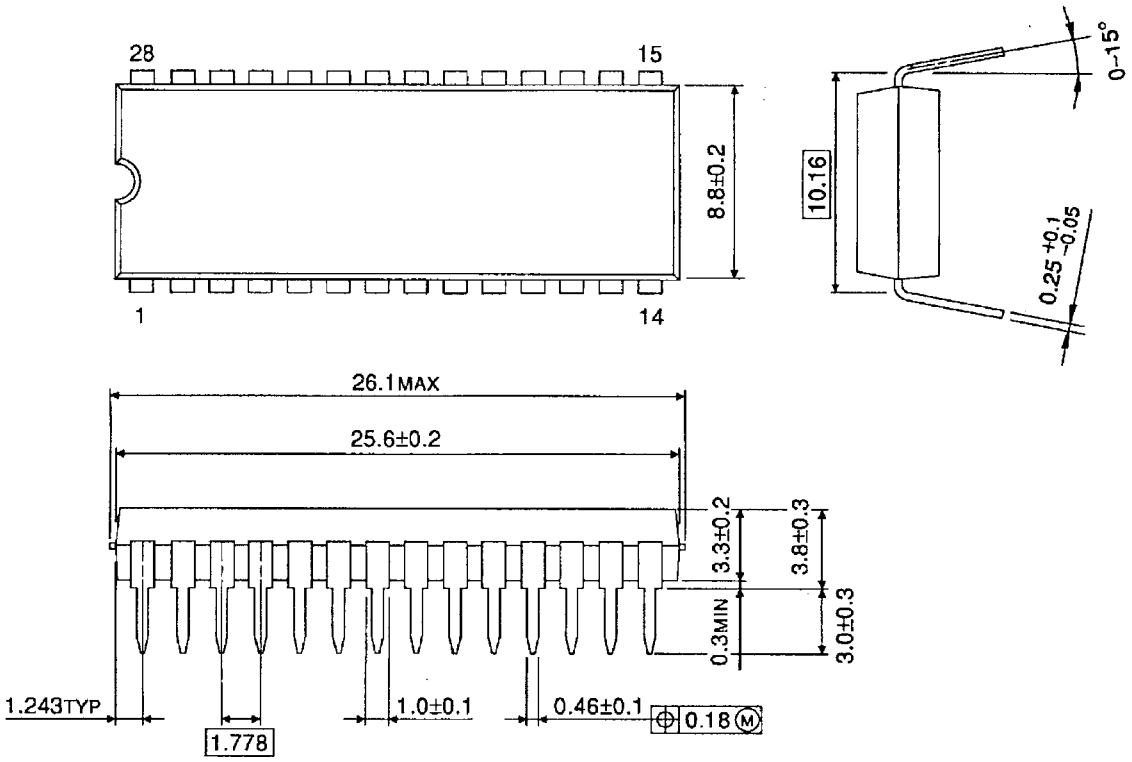
Measuring characteristic (symbol)	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply current	1	1	3	2	1	2	2	3	3	2	1	1
Pin voltage	2	2	3	2	2	2	2	3	3	2	1	1
3-level input voltage	1	1	3	2	1	1	2	3	3	2	1	1
2-level input voltage	1	1	3	1	1	2	1	3	3	2	1	1
Output voltage	1	1	3	2	1	2	1	1, 2	1, 2	2	1	1
Low-frequency gain	1	1	3	2	1	2	2	3	3	2	1	1
Comb characteristic (Ycom)	1	1	2	2	1	2	2	3	3	2	1	1
Frequency characteristic	1	1	2	2	1	1	2	3	3	2	1	1
Output impedance (Zy)	1	1	3	2	1	2	2	3	3	2	1, 2	2
Fundamental wave clock leakage (L_{1fy})	2	2	3	2	2	2	2	3	3	2	1	1
Chrominance signal gain	1	1	3	2	1	2	2	3	3	1	1	1
Comb characteristic (Ccom)	1	1	2	2	1	2	2	3	3	1	1	1
BPF frequency characteristic	1	1	3	2	1	2	2	3	3	1	1	1
Output impedance (Zc)	1	1	3	2	1	2	2	3	3	1	1, 2	2
Fundamental wave clock leakage (L_{1fc})	2	2	3	2	2	2	2	3	3	1	1	1
Y comb frequency characteristic 1, 2, 3, 4	1	1	1	2	1	2	2	3	3	2	1	1
CNR characteristic	1	1	3	2	1	2	2	3	3	1	1	1
PLL characteristic (3 items)	1	1	3	2	1	2	2	3	3	2	1	1
HD reference characteristic (4 items)	1	1	3	2	1	1	1	3	3	2	1	1
I^2C bus control characteristic	1	1	3	2	1	2	2	3	3	2	1	1

Application Circuit Example



Package Dimensions

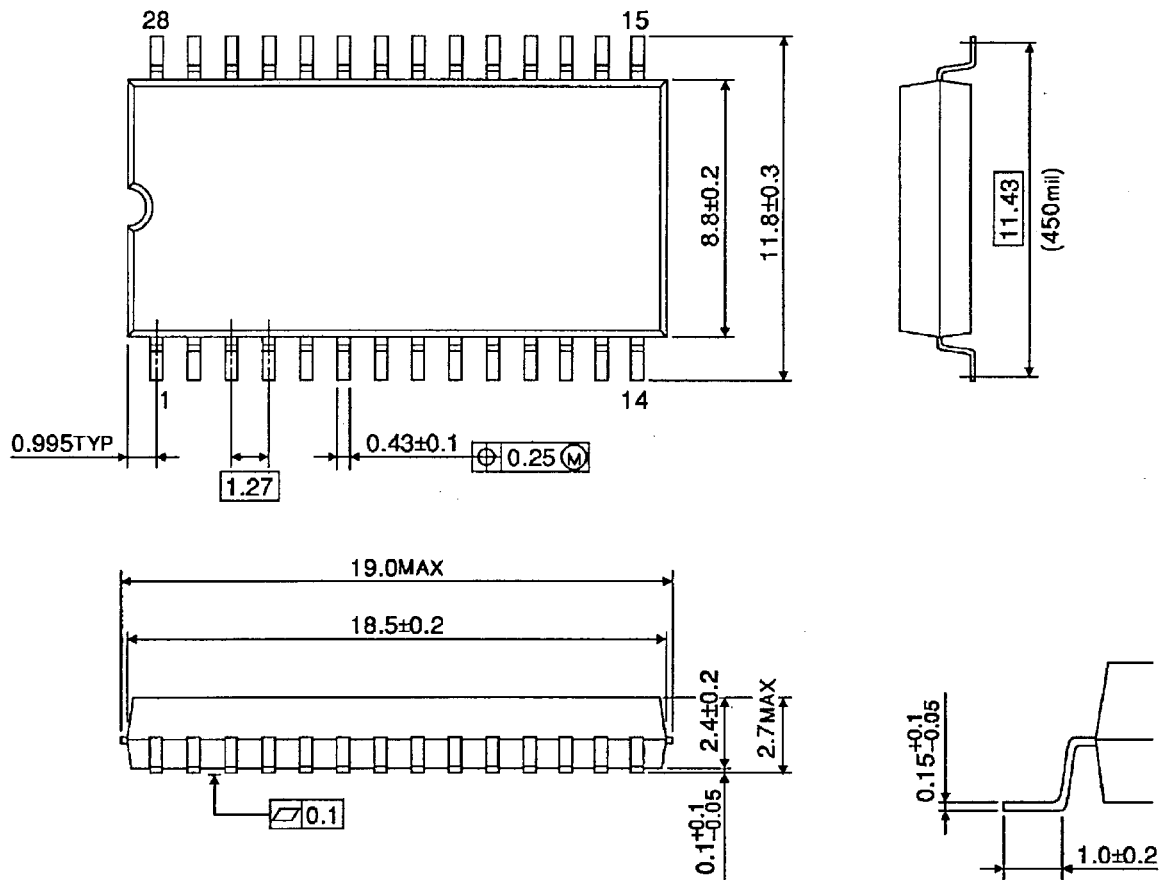
SDIP28-P-400-1.78 Unit : mm



Weight: 1.7 g (typ.)

Package Dimensions

SOP28-P-450-1.27 Unit : mm



Weight: 0.8 g (typ.)

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000707EBA

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