

Feb. 1985

**Features**

- Provides DTMF high and low group filtering
- Hard-limiting on filter outputs
- 6 pole bandpass high and low group filters
- 40 dB (typ) Intergroup attenuation
- Dial tone suppression
- +5 to +12V single supply operation
- Logical powerdown
- Uses inexpensive 3.58 MHz crystal
- Wide dynamic range 30dB

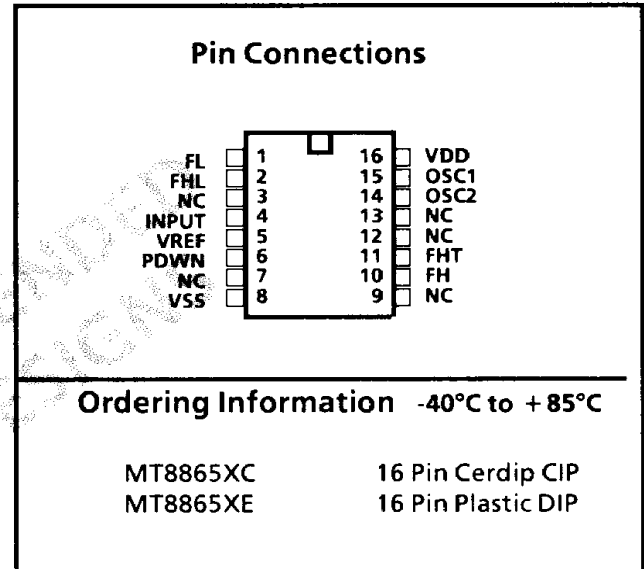
**Applications**

In DTMF Receivers For

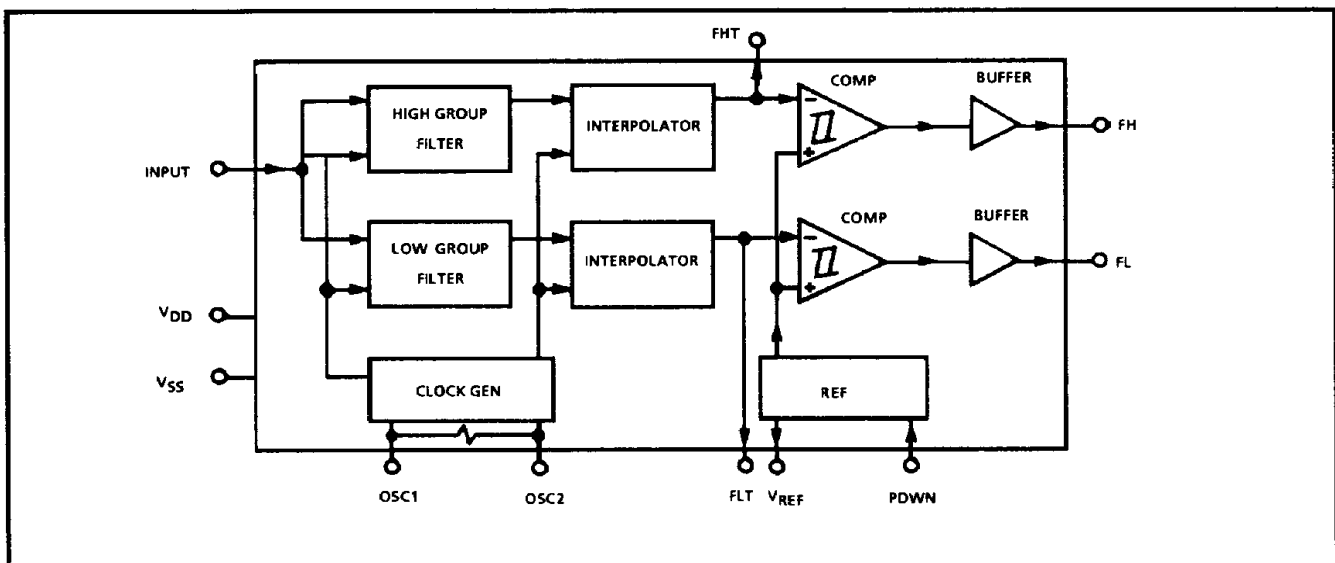
- End-to-end signalling
- Control systems
- PABX
- Central Office
- Mobile Radio
- Key systems
- Tone to pulse converters

**Description**

The Mitel MT8865 contains both the high group and low group filtering and comparator functions required to implement a Dual Tone Multi Frequency tone receiver using a Mitel DTMF Digital Detector (i.e., Mitel MT8860). Switched capacitor techniques are used to implement the filters and the device is fabricated using Mitel's double poly ISO<sup>2</sup>-CMOS high density technology. The filter clocks are


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derived from an on-chip oscillator requiring only a low cost TV crystal as external components. The MT8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.


**Fig. 1 Functional Block Diagram**

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## Absolute Maximum Ratings\*

	Parameter	Symbol	Min	Max	Units	
1	$V_{DD} - V_{SS}$			15	V	
2	Voltage on any pin except OS1, OSC2		$V_{EE} - 0.3$	$V_{DD} + 0.3$	V	
3	Max. Current at any pin	$I_I$		10	mA	
4	Storage Temperature	C Package	$T_{STG}$	-65	+150	°C
		E Package	$T_{STG}$	-65	+125	°C
5	Power Dissipation	C Package <sup>①</sup>	$P_D$		850	mW
		E Package <sup>②</sup>	$P_D$		400	mW

\*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

① Derate above 75°C at 16 mW / °C. All leads soldered to board.

② Derate above 25°C at 6.3 mW / °C. All leads soldered to board.

## Recommended Operating Conditions - Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated.

	Parameter	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	DC Power Supply Voltage	$V_{DD}$	4.75		13	V	
2	Operating Temperature	$T_O$	-40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

## DC Electrical Characteristics - Voltages are with respect to ground ( $V_{SS}$ ), $T_A = 25^\circ\text{C}$ , $f_c = 3.579545$ MHz unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	Operating Supply Voltage	$V_{DD}$	4.75		13	V	$V_{DD} = 5V$
		$V_{DD}$					$V_{DD} = 12V$
2	Operating Supply Current	$I_{DD}$		1.2	3	mA	$V_{DD} = 5V, PDWN = V_{SS}$
		$I_{DD}$		5	10	mA	$V_{DD} = 12V, PDWN = V_{SS}$
3	Standby Supply Current	$I_{DDs}$		70	100	μA	$V_{DD} = 5V, PDWN = V_{DD}$
		$I_{DDs}$		300	500	μA	$V_{DD} = 12V, PDWN = V_{DD}$
4	Operating Power Consumption Fig. 5(c)	$P_O$		6		mW	$V_{DD} = 5V, PDWN = V_{SS}$
		$P_O$		60		mW	$V_{DD} = 12V, PDWN = V_{SS}$
5	Standby Power Consumption C = 15 pF	$P_S$		0.5		mW	$V_{DD} = 5V, PDWN = V_{DD}$
		$P_S$		1.5		mW	$V_{DD} = 12V, PDWN = V_{DD}$
6	Low Level Input Voltage PDWN & OSC1	$V_{IL}$			1.5	V	$V_{DD} = 5V$
		$V_{IL}$			3.5	V	$V_{DD} = 12V$
7	High Level Input Voltage PDWN & OSC1	$V_{IH}$	3.5			V	$V_{DD} = 5V$
		$V_{IH}$	8.5			V	$V_{DD} = 12V$
8	Pull Down Sink Current PDWN	$I_{IH}$		3	6	μA	$V_{DD} = 5V$
		$I_{IH}$		12	24	μA	$V_{DD} = 12V$
9	Input Current OSC1	$I_I$		±2.5		μA	$V_{DD} = 5V$
		$I_I$		±6		μA	$V_{DD} = 12V$
10	Low Level Output Voltage FL, FH, OSC2	$V_{OL}$			0.1	V	$V_{DD} = 5V, \text{No Load}$
		$V_{OL}$			0.1	V	$V_{DD} = 12V, \text{No Load}$
11	High Level Output Voltage FL, FH, OSC2	$V_{OH}$	4.9			V	$V_{DD} = 5V, \text{No Load}$
		$V_{OH}$	11.9			V	$V_{DD} = 12V, \text{No Load}$
12	Output Drive Current, FL, FH N Channel Sink	$I_{OL}$	0.2			mA	$V_{DD} = 5V, V_{OL} = 0.4V$
		$I_{OL}$	0.5			mA	$V_{DD} = 12V, V_{OL} = 1.2V$

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

**DC Electrical Characteristics (Cont'd)** - Voltages are with respect to ground ( $V_{SS}$ ),  $T_A = 25^\circ\text{C}$ ,  $f_c = 3.579545$  MHz unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>†</sup>	Max	Units	Test Conditions
13	Output Drive Current OSC2, N Channel Sink	$I_{OL}$	0.1			mA	$V_{DD} = 5V, V_{OL} = .4V$
			0.25			mA	$V_{DD} = 12V, V_{OL} = 1.2V$
14	Output Drive Current, FL, FH P Channel Source	$I_{OH}$	0.2			mA	$V_{DD} = 5V, V_{OH} = 4.6V$
			0.5			mA	$V_{DD} = 12V, V_{OH} = 10.8V$
15	Output Drive Current, OSC2, P Channel Source	$I_{OH}$	0.1			mA	$V_{DD} = 5V, V_{OH} = 4.6V$
			0.25			mA	$V_{DD} = 12V, V_{OH} = 10.8V$
16	Output Voltage, $V_{Ref}$	$V_{Ref}$	2.3		2.6	V	$V_{DD} = 5V, \text{No Load}$
			5.4		6.2	V	$V_{DD} = 12V, \text{No Load}$
17	Output Resistance, $V_{Ref}$	$R_{OR}$			16	k $\Omega$	$V_{DD} = 5V$
					8	k $\Omega$	$V_{DD} = 12V$

<sup>†</sup> Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

**AC Electrical Characteristics** - Voltages are with respect to ground ( $V_{SS}$ ),  $T_A = 25^\circ\text{C}$ ,  $f_c = 3.579545$ ,  $V_{DD} = 4.75 - 13V$ .

	Characteristics	Sym	Min	Typ <sup>†</sup>	Max	Units	Test Conditions
1	Dynamic Range		30		36	dB	
2	Valid Input Signal Levels (Each tone of composite signal)		27.9		$V_{DD}/2$	$V_{pp}$	$V_{DD} = 5V$ $V_{DD} = 12V$
			67.0		883	mVrms	
3	Input Impedance	$Z_i$	10			M $\Omega$	
4	Passband Ripple	$A_v$		$\pm 0.3$	$\pm 1.0$	dB	See Note 1
5	Low Group 1dB Bandwidth	Lower Limit	$f_{LL}$	670	684	Hz	
			Upper Limit	$f_{LU}$	958	990	Hz
6	High Group 1dB Bandwidth	Lower Limit	$f_{HL}$	1162	1188	Hz	
			Upper Limit	$f_{HU}$	1660	1740	Hz
7	Intergroup Rejection Low Group with High Tone	$IR_{L1209}$	34	45		dB	1209Hz - w.r.t. 770Hz
			$IR_{L1477}$	36	40		dB
8	Intergroup Rejection High Group with Low Tone	$IR_{H941}$	38	50		dB	941Hz - w.r.t. 1336Hz
			$IR_{H770}$	36	40		dB
9	Dial Tone Rejection Low Group	$DR_{L440}$	40	60		dB	440Hz - w.r.t. 770Hz
			$DR_{L350}$	28	30		dB
10	Dial Tone Rejection High Group	$DR_{H440}$	52	60		dB	440Hz - w.r.t. 1336Hz
			$DR_{H350}$	50	55		dB
11	FHT FLT Maximum Permissible Load	$R_{LFT}$	250			k $\Omega$	
			$C_{LFT}$			1000	pF
12	Output Rise Time FL, FH	$t_{TLHO}$		90	150	ns	10% to 90% $V_{DD}$
	Output Fall Time FL, FH	$t_{THLO}$		60	100	ns	
13	Crystal/Clock Freq. OSC1, OSC 2	$f_c$	3.5759	3.5795	3.5831	MHz	
14	Clock Input (OSC 1)	Rise Time	$t_{LHCI}$		110	ns	See Note 2
		Fall Time	$t_{HLCI}$		110	ns	
		Duty Cycle	$DC_{CI}$	40	50	60	
15	Clock Output OSC 2 Capacitive Load	$C_{LOC}$			30	pF	Unbalanced load see Fig. 5
16	Capacitance Any Input	$C_i$		5	7.5	pF	

Note 1. Passband ripple measured with respect to a passband gain of 0 dB  $\pm$  1dB.

Note 2. 10% to 90%  $V_{DD}$ . Externally Applied Clock.

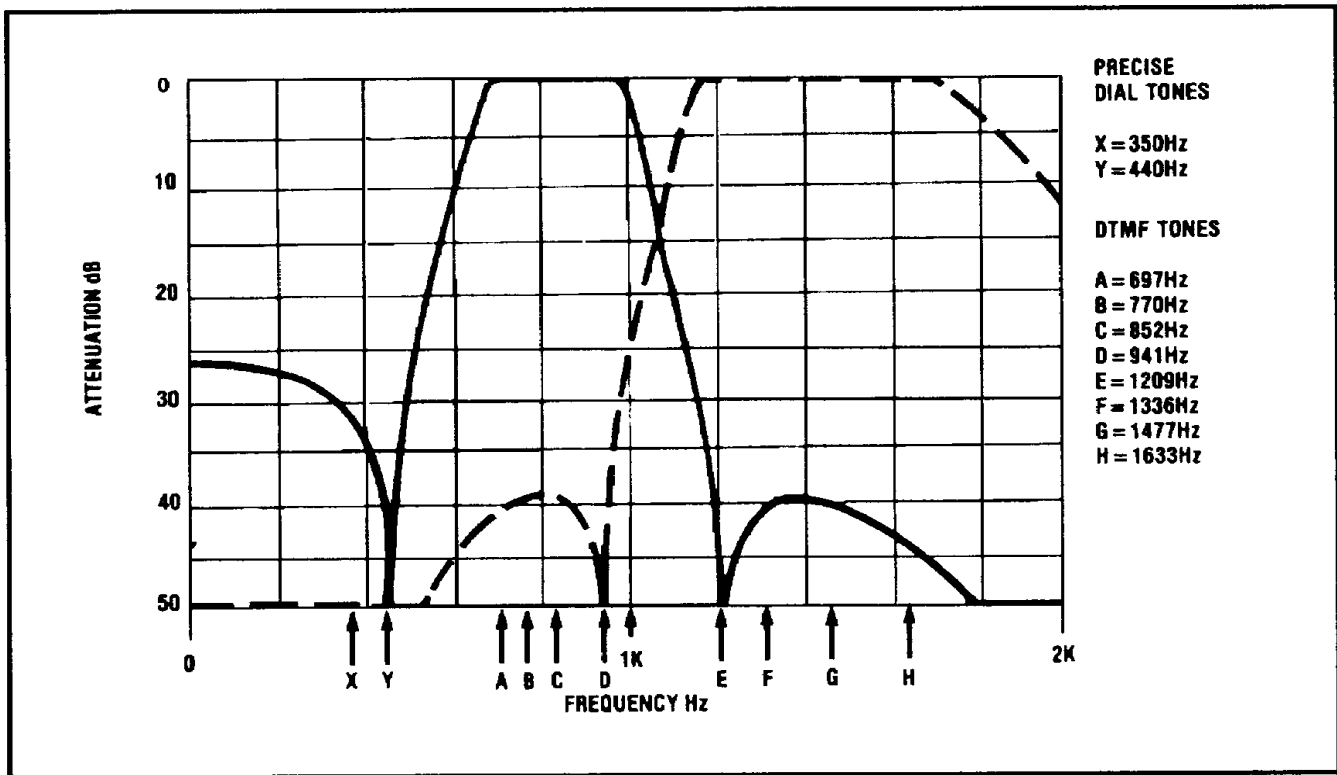


Fig. 2 - Typical Filter Characteristics

Pin Description

Pin #	Name	Description
1	FL	Low Group Limiter Output.
2	FLT	Test Output. Monitors low group filter output. Decouple to V <sub>SS</sub> with 680pF capacitor.
3	NC	Not Connected.
4	INPUT	Tone Signal Input (single ended).
5	V <sub>Ref</sub>	Internal Reference. Can be used to bias input via 2MΩ resistor.
6	PDWN	Power Down Active High. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.
7	NC	Not Connected.
8	V <sub>SS</sub>	Negative (OV) Power Supply.
9	NC	Not Connected.
10	FH	High Group Limiter Output.
11	FHT	Test Output. Monitors high group filter output. Decouple to V <sub>SS</sub> with 680pF capacitor.
12	NC	Not Connected.
13	NC	Not Connected.
14	OSC2	Clock Output.
15	OSC1	Clock Input. 3.579545 MHz crystal connected between this pin and OS2 completes the internal oscillator circuit.
16	VDD	Positive Power Supply.

**Functional Description**

The MT8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves, to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of the DTMF Digital Decoder (MT8860). See Fig. 3.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths

of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig. 2) also incorporates a notch at 440Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting. The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MT8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig. 3) or via a differential buffer to a telephone line (Fig. 4). The signal input (Pin 4) should be biased at  $V_{DD}/2$ . With the input

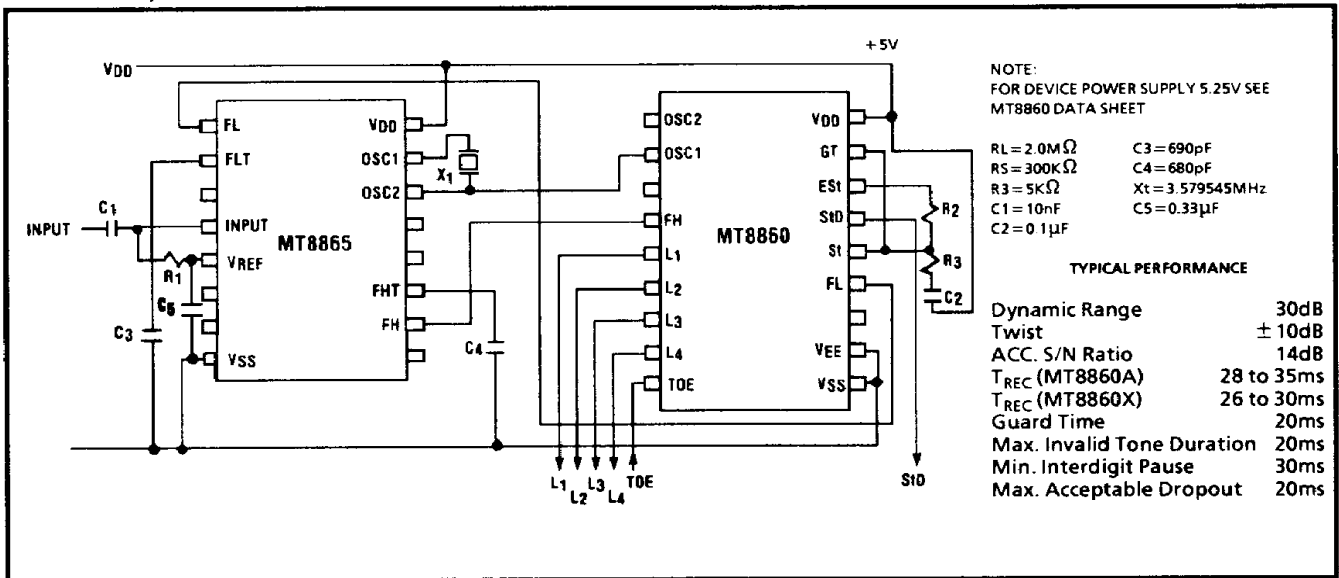


Fig. 3 - Connection Diagram for Single-Ended Input Receiver Using the MT8860 (5V Operation)

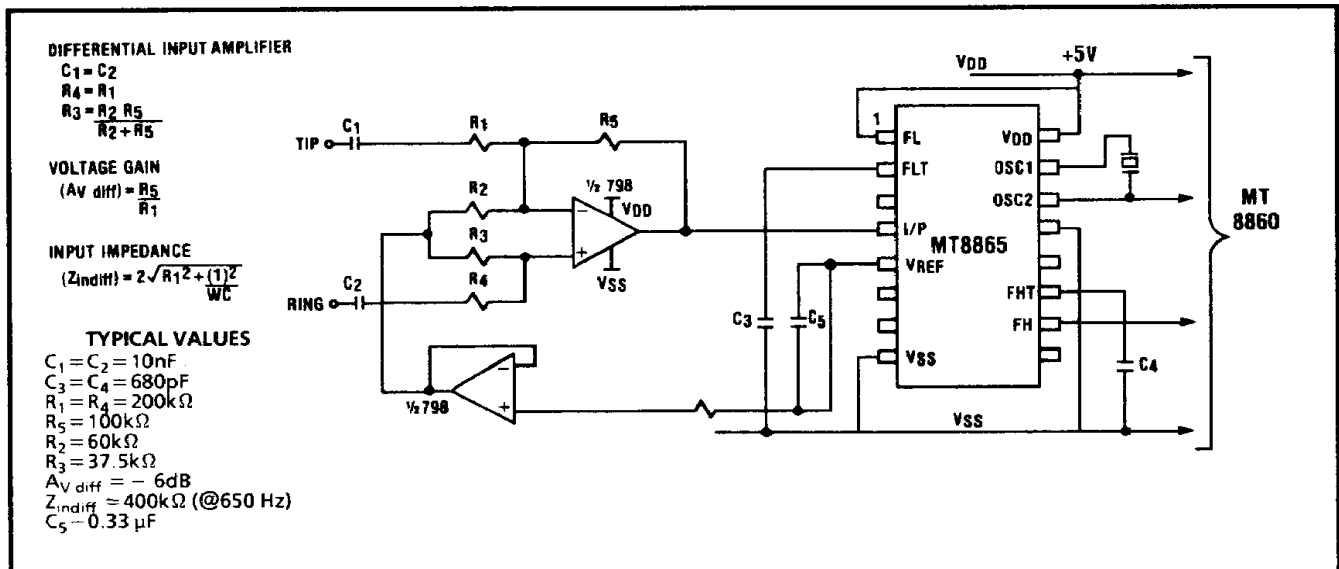
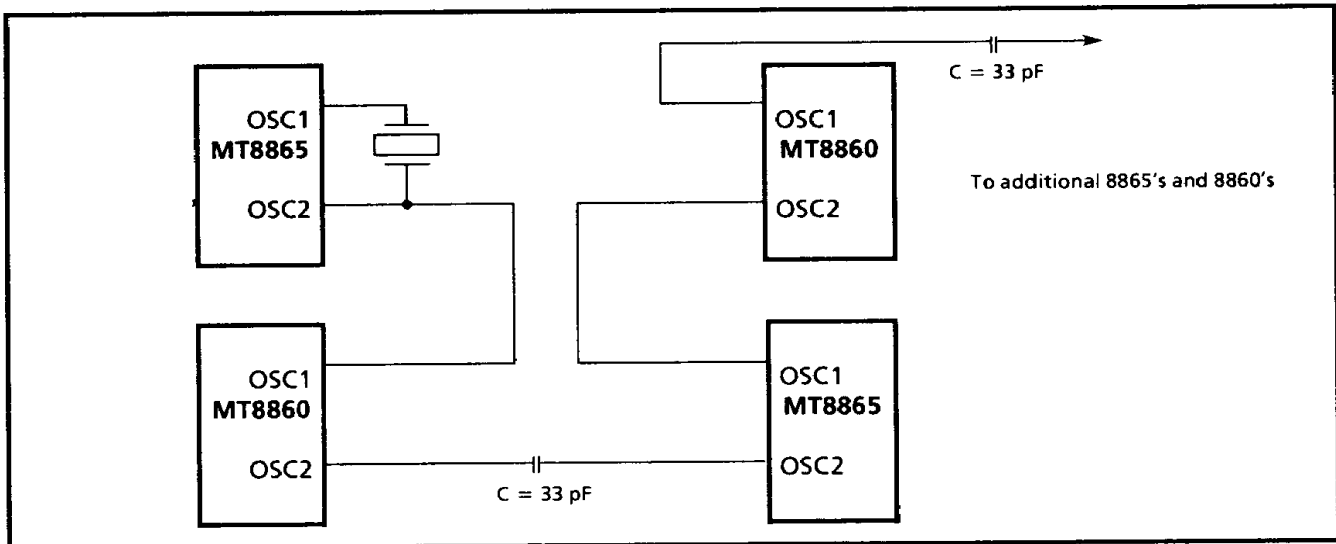


Fig. 4 - Circuit for Connection to a Telephone Line

capacitively coupled, this is achieved by connecting the signal input to  $V_{Ref}$  (Pin 5) via a  $2M\Omega$  resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to  $V_{SS}$  by 680pF capacitors.

The MT8865 and its companion, the MT8860 DTMF decoder, can share a crystal by cascading the oscillator output (OSC2) to the adjacent device oscillator input (OSC1). The recommended circuit is shown in Figure 5.



**Fig. 5 - Cascaded Oscillator Configuration**