Data Sheet

41KD Interrupt Holding Register

Features

- Up to four interrupt inputs per interrupt holding register
- Cascadable inputs and outputs for expansion
- Convenient interface signals: A0, $\overline{E}$, R/$\overline{W}$
- Individually maskable interrupt inputs
- Masking and interrupt registers may be read or written to verify operational integrity
- TTL/CMOS-compatible
- Low-power Schottky LSTTL-technology

Description

The 41KD Interrupt Holding Register (IHR) is designed to capture, mask, store, and retrieve interrupt signals in systems that contain integrated read and write control signals.* The system must supply read and write timing via the 41KD device's enable signal. Control logic is provided that permits processor interfacing on a memory-mapped basis to all microprocessors or microcomputers. When queried by the processor for interrupts, the IHR returns a linear indication of pending interrupts on a one-to-one basis rather than a binary weighted priority indication. Various processor subroutines can be used to prioritize and stack pending interrupts. A single IHR can accommodate up to four interrupt inputs; however, cascadable inputs and outputs are provided for expansion. The IHR is an LSTTL-technology device and is packaged in a 16-pin plastic DIP (41KD), 16-pin plastic SOJ package (41KD-J), or in a 16-pin plastic SOIC package (41KD-W).

User Information

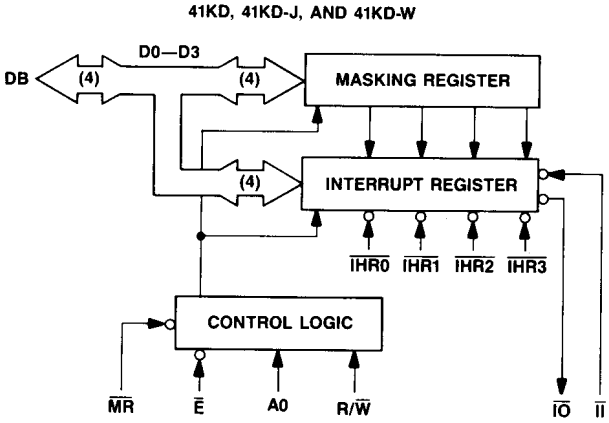


Figure 1. Block Diagram

* Systems that have separate read and write control signals should use the 146R Interrupt Holding Register (DS87-315DBIP).

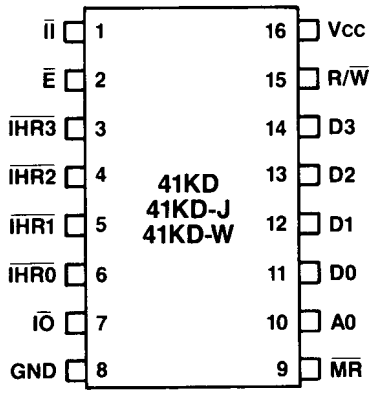


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name
1	$\overline{II}$	I	Interrupt Input
2	$\overline{E}$	I	Chip Enable
3—6	$\overline{IHR3}$—$\overline{IHR0}$	I	Interrupt Holding Register
7	$\overline{IO}$	O	Interrupt Output
8	GND	—	Ground
9	$\overline{MR}$	I	Master Reset
10	A0	I	Address Input
11—14	D0—D3	I/O	Data Input and Output
15	R/$\overline{W}$	I	Read or Write Signal
16	Vcc	—	5.0 ±0.5 V

Overview

The internal architecture of the IHR is based on one section of control logic and two 4-bit-wide registers (masking and interrupt).

Control Logic. The control logic interfaces the masking and interrupt registers with the processor bus. The system software can read or write either the masking or interrupt register by accepting Addresses (A0), Chip Enable ($\overline{E}$), and Read/Write (R/$\overline{W}$) signals, and can initialize the IHR with a Master Reset ($\overline{MR}$) signal.

The Address line input (A0) addresses the desired register for a read or write operation. When A0 is a logic low, the input addresses the interrupt register. When A0 is a logic high, the input addresses the masking register.

The Chip Enable input ($\overline{E}$) enables all IHR read and write operations via the data bus. A read or write operation may be performed only when $\overline{E}$ is a logic low.

The Read/Write input (R/$\overline{W}$) selects either a read or write operation for the register. A write operation occurs when R/$\overline{W}$ is a logic low and a read occurs when it is a logic high.

The Master Reset input ($\overline{MR}$) is an overriding clear input that initializes the IHR. As long as $\overline{MR}$ is a logic low, all internal flip-flops are reset (low state). When the $\overline{MR}$ low is removed, the masking register is in the "non-mask" condition and the interrupt register is in the "no-interrupt" condition. The state of the Chip Enable will not affect the operation of the Master Reset.

Masking Register. The 4-bit masking register inhibits one or more of the corresponding interrupt holding inputs ($\overline{IHR0}$—$\overline{IHR3}$). A logic high written to the masking register (via the data bus) inhibits an interrupt from setting the corresponding interrupt holding latch.

Interrupt Register. The 4-bit interrupt register contains the status of the four interrupt flip-flops. This register normally contains all zeros, indicating that no interrupt requests have occurred. The individual register flip-flops are set (made a logic high) by the presence of an external active low level at any one or all of the interrupt holding inputs ($\overline{IHR0}$—$\overline{IHR3}$), providing the corresponding masking register bit is a logic low. There is a one-to-one correspondence between the Interrupt Masking Register and the Interrupt Input Signals. The Interrupt Output ($\overline{IO}$) and the Interrupt Input ($\overline{II}$) lines are used for IHR cascading.

The Interrupt Output ($\overline{IO}$) goes low if any of the four flip-flops of the interrupt register are set (high) or if the Interrupt Input ($\overline{II}$) is set low. Chip Enable has no effect on the Interrupt Output, which is always enabled.

The Interrupt Input ($\overline{II}$) is used to cascade IHRs. When $\overline{II}$ is a logic high, the $\overline{IO}$ line functions as previously described. When $\overline{II}$ is a logic low, the $\overline{IO}$ line goes low and stays low until $\overline{II}$ is returned to a logic high.

Table 2. Truth Table

$\overline{E}$	$\overline{MR}$	R/$\overline{W}$	A0	Device Function
1	X	X	X	Device Inactive
0	0	X	X	Reset IHR
0	1	1	0	Read Interrupt Register
0	1	1	1	Read Masking Register
0	1	0	0	Write Interrupt Register
0	1	0	1	Write Masking Register

Note: X indicates a "don't care" condition (logic 1 or 0)

Characteristics

Electrical Characteristics

T_A = −40 to +85 °C, V_{CC} = 5.0 ± 0.5 V

Parameter	Symbol	Min	Max	Unit
Input Voltages				
Low Level	V_{IL}	0.0	0.7	V
High Level	V_{IH}	2.0	—	V
Input Clamp Diode Voltage (V_{CC} = 4.5 V, I_I = −5 mA)	V_{IK}	—	−1.5	V
Output Voltages (Data Input/Output, D0—D3) (V_{CC} = 4.5 V)				
Low Level (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Low Level (I_{OL} = 16 mA)	V_{OL}	—	0.5	V
High Level (I_{OH} = −800 μA)	V_{OH}	2.5	—	V
Output Voltages (Interrupt Output, $\overline{IO}$) (V_{CC} = 4.5 V)				
Low Level (I_{OL} = 4 mA)	V_{OL}	—	0.4	V
Low Level (I_{OL} = 8 mA)	V_{OL}	—	0.5	V
High Level (I_{OH} = −400 μA)	V_{OH}	2.5	—	V
Input Currents (V_{CC} = 5.5 V)				
Low Level (V_I = 0.4 V)	I_{IL}	—	0.36	mA
High Level (V_I = 2.7 V)	I_{IH}	—	0.02	mA
High Level (V_I = 5.5 V)	I_{IH}	—	0.1	mA
Short-Circuit Output Current (V_{CC} = 5.5 V)				
Data Input/Output (D0—D3)	I_{OS}	−40	−200	mA
Interrupt Output ($\overline{IO}$)	I_{OS}	−20	−100	mA
Power Supply Current Drain (V_{CC} = 5.5 V)	I_{CC}	—	100	mA

Maximum Ratings

Power Supply Voltage (V_{CC}) . . . . . 7.0 Vdc
Input Voltage (V_{IH}) . . . . . 5.5 Vdc
Operating Temperature Range (T_J) . . . . . −25 to +125 °C
Storage Temperature Range (T_{stg}) . . . . . −40 to +125 °C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of the devices can be performed safely at temperatures up to 300 °C.

Timing Characteristics

T_A = 25 °C, C_L = 15 pF, V_{CC} = 5.0 V

Parameters	Description	Min	Typ	Max	Unit	Notes
t_{AVEL}	Address Set-Up Time	30	—	—	ns	Figure 3
t_{RWHEL}	Read/Write Set-Up Time	30	—	—	ns	Figure 3
t_{ELOV}	Data Bus On Time	—	—	60	ns	Figures 3 & 5
t_{AVDV}	Register Access Time	40	—	—	ns	Figure 3
t_{EHDZ}	Data Bus Off Time	—	—	60	ns	Figures 3 & 5
t_{AVEH}	Address Set-Up Time	30	—	—	ns	Figure 4
t_{RWLEH}	Read/Write Set-Up Time	30	—	—	ns	Figure 4
t_{ELEH}	Write Pulse Width Time	100	—	—	ns	Figure 4
t_{DVEH}	Data Set-Up Time	75	—	—	ns	Figure 4
t_{EHDX}	Data Hold Time	0	—	—	ns	Figure 4
t_{EHRWH}	Read/Write Hold Time	15	—	—	ns	Figure 4
t_{EHAX}	Address Hold Time	30	—	—	ns	Figure 4
t_{AVRWH}	Address Set-Up Time	30	—	—	ns	Figure 5
t_{ELRWH}	Enable Set-Up Time	30	—	—	ns	Figure 5
t_{RWLWRH}	Write Pulse Width Time	100	—	—	ns	Figure 5
t_{RWLDZ}	Data Bus Off Time	—	—	60	ns	Figure 5
t_{DVRWH}	Data Set-Up Time	75	—	—	ns	Figure 5
t_{RWHDX}	Data Hold Time	0	—	—	ns	Figure 5
t_{RWHDV}	Data Bus On Time	—	—	60	ns	Figure 5
t_{RWHEH}	Enable Hold Time	30	—	—	ns	Figure 5
t_{RWHAX}	Address Hold Time	30	—	—	ns	Figure 5
t_{IPW}	Interrupt Pulse Width Time	60	—	—	ns	$\overline{IHR}$ to Latch
t_{IIO}	Interrupt Response Time	75	—	—	ns	$\overline{IHR}$ to $\overline{IO}$
t_{IIO}	Interrupt Cascade Time	40	—	—	ns	$\overline{II}$ to $\overline{IO}$

Timing Diagrams

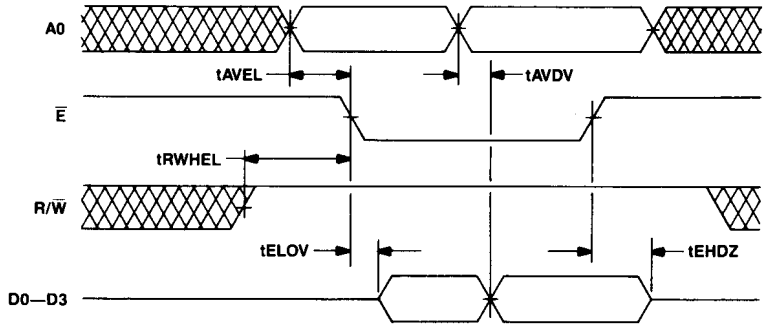


Figure 3. Read Cycle (R/W Used to Access Data)

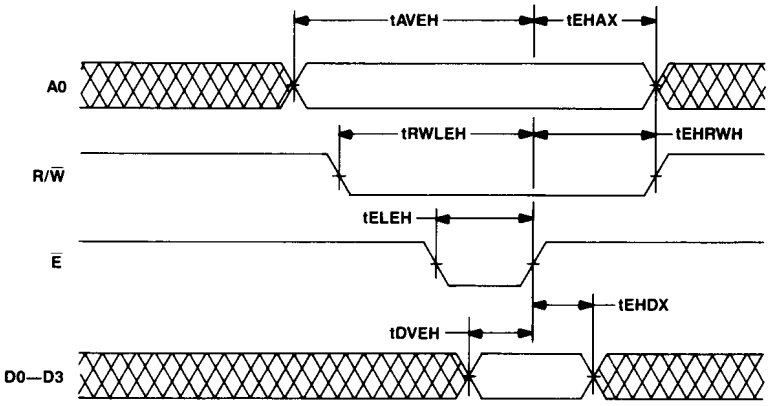
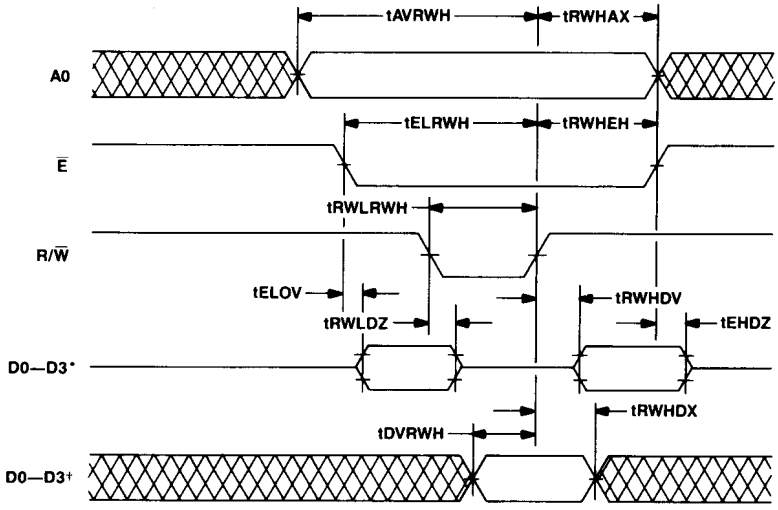


Figure 4. Write Cycle (E Used to Write Data)



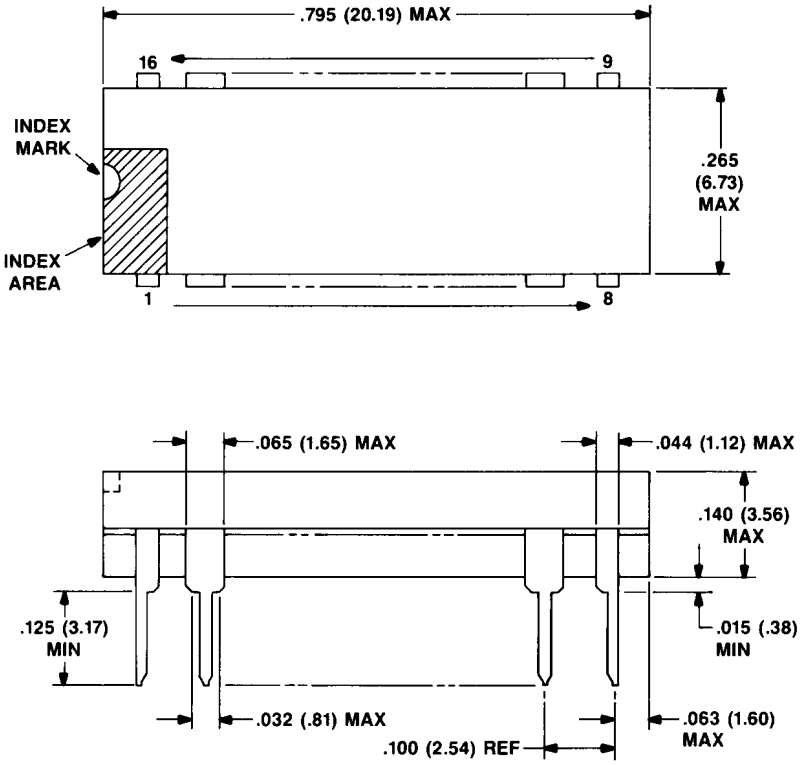
* D0—D3 IN OUTPUT CONDITION
† D0—D3 IN INPUT CONDITION

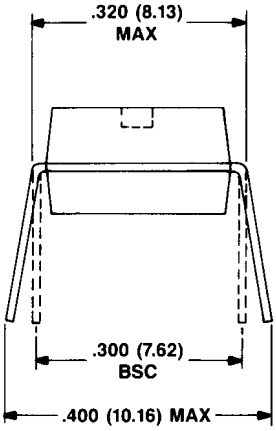
Figure 5. Write Cycle (R/W Used to Write Data)

Outline Diagrams

Dimensions in inches and (millimeters)

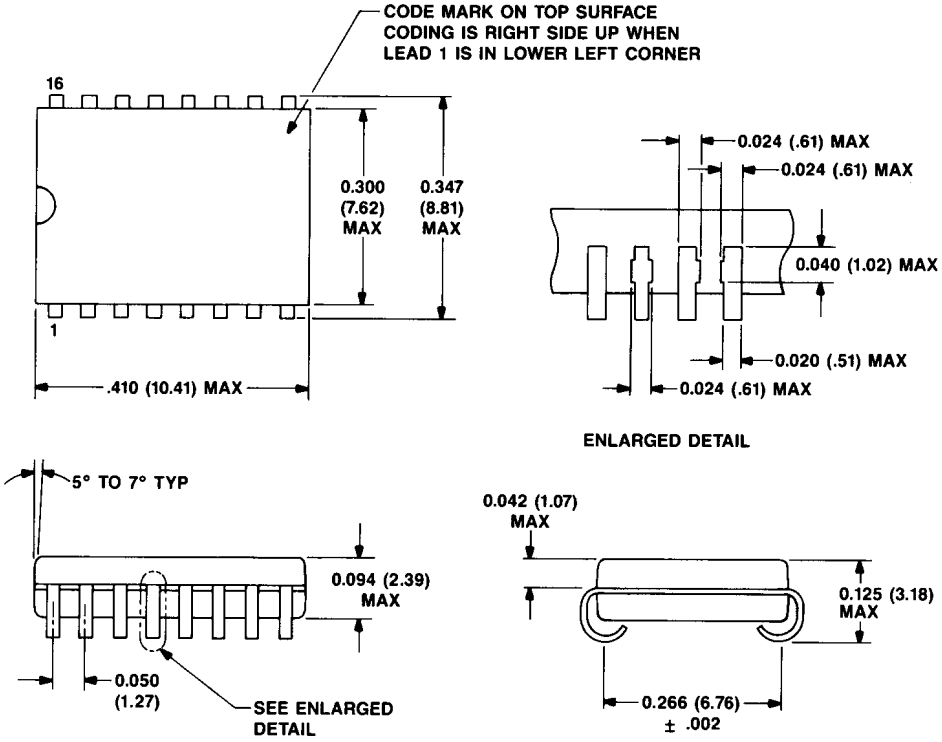
16-Pin Plastic DIP



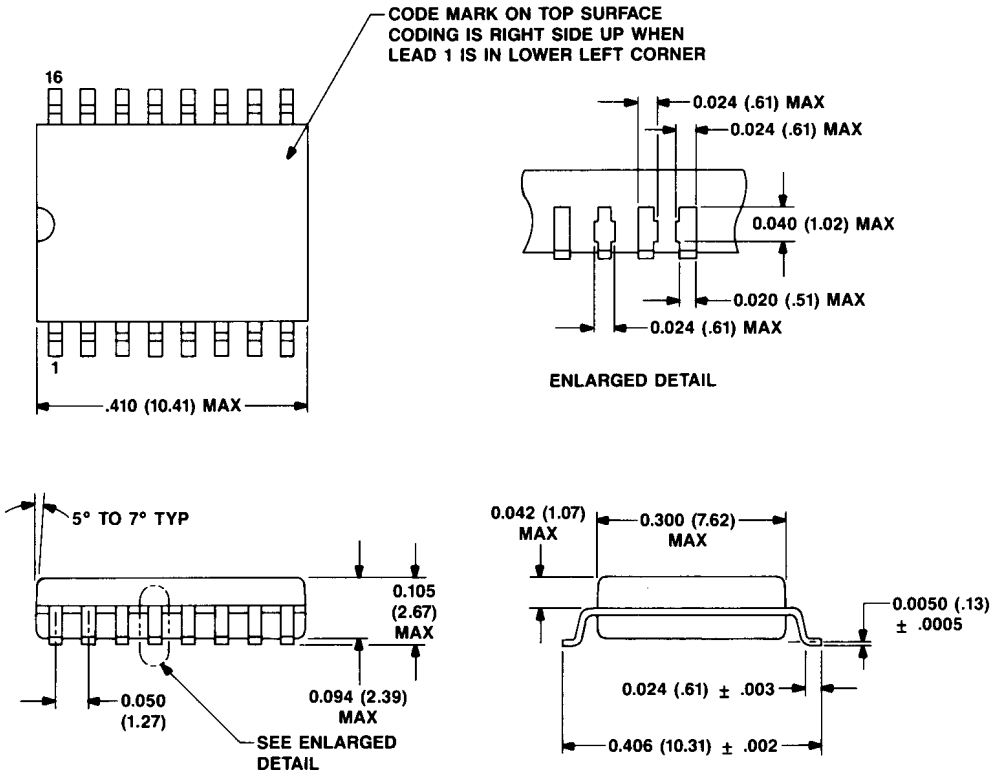


16-Pin Plastic SOJ

Dimensions in inches and (millimeters)



16-Pin Plastic SOIC



Ordering Information

Device Code	Package	Comcode
41KD	16-Pin Plastic DIP	103257903
41KD-J	16-Pin Plastic SOJ	104450929
41KD-W	16-Pin Plastic SOIC	104450937

For additional information, contact your AT&T Account Manager, or call:

☐ AT&T Microelectronics
Dept. 51AL230230
555 Union Boulevard
Allentown, PA 18103
1-800-372-2447

In Canada, call:
1-800-553-2448

☐ AT&T Microelectronics GmbH
Freischützstrasse 92
D-8000 Munich 81
West Germany
Tel. 0 89/95 97 0
Telex 5 216 884

☐ AT&T Microelectronics Pte. Ltd.
745 Lorong 5 Toa Payoh
Singapore 1231
Tel. 259-6622
Telex RS42898
FAX 259-2244

☐ AT&T Japan
7F, Fukoku Seimei Bldg.,
2-2-2, Uchisaiwai-cho,
Chiyoda-ku, Tokyo 100 Japan
Tel. (03) 502-3055
Telex J32562 ATTIJ
FAX (03) 593-3307

June 1988

DS87-316DBIP

AT&T
The right choice.

008185