DATA SHEET

TDA4885
150 MHz video controller with I²C-bus

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Philips Semiconductors

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150 MHz video controller with I²C-bus TDA4885

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2 GENERAL DESCRIPTION

The TDA4885 is a monolithic integrated RGB pre-amplifier for colour monitor systems (e.g. 15" and 17") with I²C-bus control and OSD. In addition to bus control beam current limiting and gain modulation are possible. The signals are amplified in order to drive commonly used video modules or discrete solutions. Individual black level control with negative feedback from the cathode (DC coupling) or fixed black level control with positive feedback and 3 DAC outputs for external cut-off control (AC coupling) is possible.

With special advantages the circuit can be used in conjunction with the TDA485x monitor deflection IC family.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4885	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)		7.6	8.0	8.8	V
I_P	supply current (pin 7)		–	20	25	mA
$V_{P1, 2, 3}$	channel supply voltage (pins 29, 24 and 19)		7.6	8.0	8.8	V
$I_{P1, 2, 3}$	channel supply current (pins 29, 24 and 19)		–	40	–	mA
$V_{i(b-w)}$	input voltage (black-to-white value; pins 6, 8 and 10)		–	0.7	1.0	V
$V_{o(b-w)}$	nominal output voltage swing (black-to-white value; pins 30, 25 and 20)	nominal contrast; maximum gain; pins 12, 13 and 14 grounded	2.5	2.8	–	V
$V_{o(b-w)(max)}$	maximum output voltage swing (black-to-white value; pins 30, 25 and 20)	maximum contrast; maximum gain; pins 12, 13 and 14 grounded	–	4.5	–	V
V_o	output voltage level (pins 30, 25 and 20)		0.1	–	6.0	V
V_{bl}	typical reference black level (pins 30, 25 and 20)		0.5	–	2.5	V
$I_{o(sink)}$	peak output sink current	during fast signal transients	–	–	20	mA
$I_{o(source)}$	peak output source current	during fast signal transients	–40	–	–	mA
B	bandwidth	–3 dB (small signal)	–	150	–	MHz
$t_{r(O)}$	video rise time at signal outputs (pins 30, 25 and 20)		–	2.7	–	ns
dV_O	over/undershoot at signal outputs (pins 30, 25 and 20)	minimum rise/fall time	–	5	–	%
α_{ct}	crosstalk at signal outputs (pins 30, 25 and 20)	f = 80 MHz	–	–30	–	dB
C_C	contrast control related to nominal contrast		–28	–	+4	dB
G_C	gain control related to maximum gain		–7	–	0	dB
BC	brightness control (typical black level voltage change related to output signal amplitude)		–10	–	+30	%
$V_{o(OSD)(max)}$	maximum OSD output voltage swing related to nominal output voltage swing (pins 30, 25 and 20)	maximum OSD contrast; maximum gain; pins 12, 13 and 14 grounded	–	125	–	%
C_{OSD}	OSD contrast control related to maximum OSD contrast		–12	–	0	dB

5 BLOCK DIAGRAM

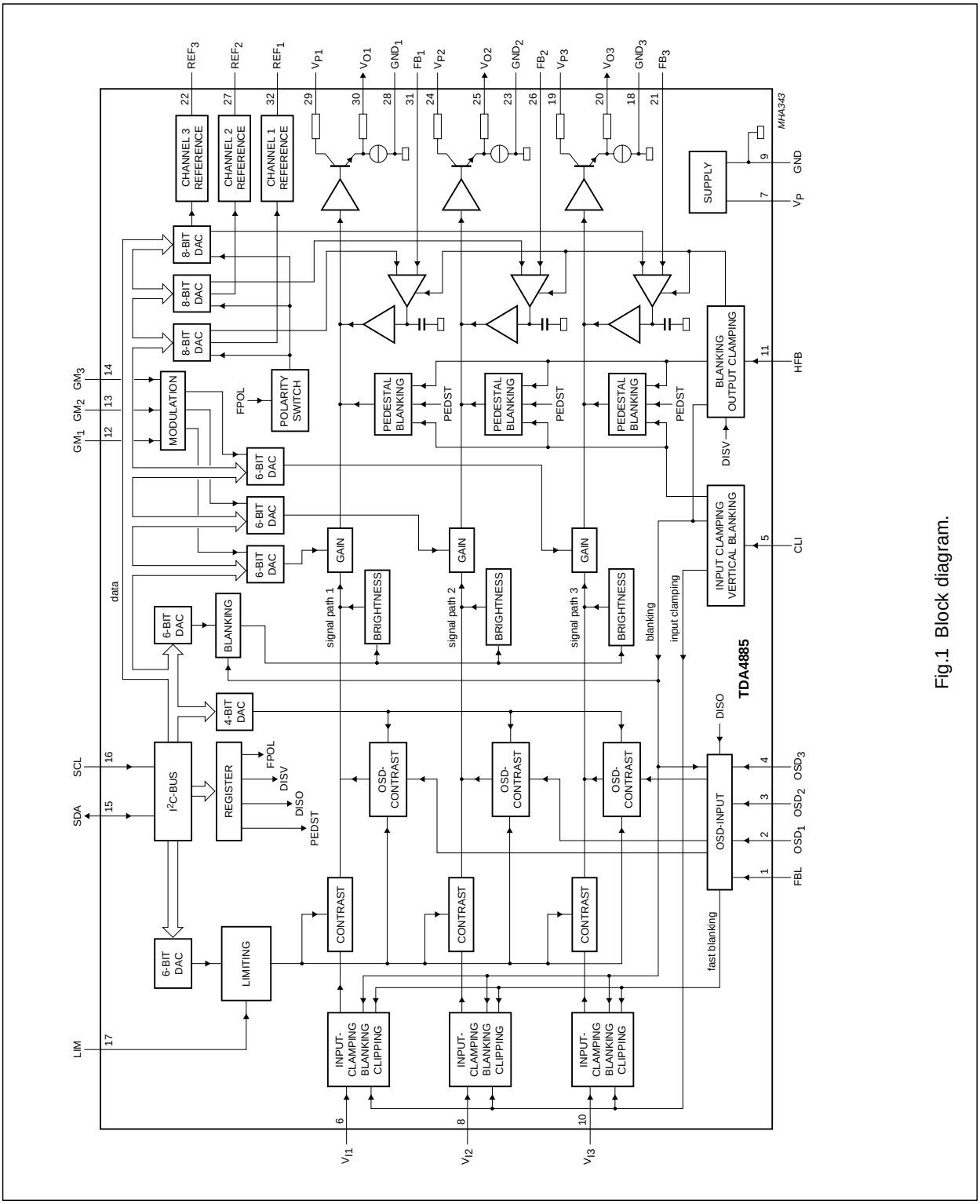


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
FBL	1	fast blanking input for OSD insertion
OSD_1	2	OSD input channel 1
OSD_2	3	OSD input channel 2
OSD_3	4	OSD input channel 3
CLI	5	vertical blanking input (input clamping)
V_{I1}	6	signal input channel 1
V_P	7	supply voltage
V_{I2}	8	signal input channel 2
GND	9	ground
V_{I3}	10	signal input channel 3
HFB	11	horizontal flyback input (output clamping, blanking)
GM_1	12	gain modulation input channel 1
GM_2	13	gain modulation input channel 2
GM_3	14	gain modulation input channel 3
SDA	15	I²C-bus serial data input/output
SCL	16	I²C-bus clock input
LIM	17	beam current limiting input, subcontrast setting
GND_3	18	ground channel 3
V_{P3}	19	supply voltage channel 3
V_{O3}	20	signal output channel 3
FB_3	21	feedback input channel 3
REF_3	22	reference voltage channel 3
GND_2	23	ground channel 2
V_{P2}	24	supply voltage channel 2
V_{O2}	25	signal output channel 2
FB_2	26	feedback input channel 2
REF_2	27	reference voltage channel 2
GND_1	28	ground channel 1
V_{P1}	29	supply voltage channel 1
V_{O1}	30	signal output channel 1
FB_1	31	feedback input channel 1
REF_1	32	reference voltage channel 1

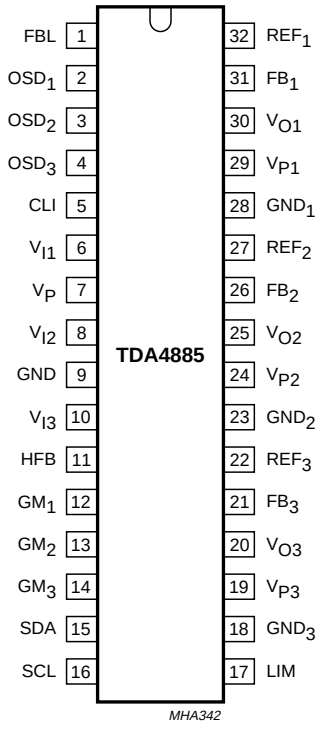


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

See block diagram (Fig.1) and definition of levels and output signals (Chapter “Characteristics” notes 1 to 3; Figs 3 to 6).

7.1 Signal input stage (input clamping, blanking and clipping)

The RGB input signals with nominal signal amplitude of $0.7V_{b\text{-}w}$ are capacitively coupled into the TDA4885 from a low-ohmic source (75 Ω recommended) and actively clamped to an internal DC voltage during signal black level. Because of the high-ohmic input impedance of the TDA4885 the coupling capacitor (which also functions as storage capacitor during clamping pulses) can be relatively small (10 nF recommended). The internal leakage currents will discharge the coupling capacitor resulting in black output signals for missing **input clamping pulses**.

Composite signals will not disturb normal operations because a **clipping circuit** cuts all signal parts below black level.

A fast **signal blanking** stage belongs to the input stage which is driven by several **blanking pulses** (see Section “Clamping and blanking pulses”) and control bit DISV = 1. During the off condition the internal reference black level will be inserted instead of the input signals.

7.2 Electronic potentiometer stages

7.2.1 Contrast control (driven by I²C-bus, 6-bit DAC)

The input signals related to the internal reference black level can be simultaneously adjusted by contrast control with a control range of typically 32 dB. The nominal contrast setting is defined for 26H (4 dB below maximum).

7.2.2 Brightness control (driven by I²C-bus, 6-bit DAC)

With brightness control the video black level will be shifted in relation to the reference black level simultaneously for all three channels. With a negative setting (maximum 10% of nominal signal amplitude) dark signal parts will be lost in ultra black while for positive settings (maximum 30% of nominal signal amplitude) the background will alter from black to grey. The nominal brightness setting (10H) is no shift. The brightness setting is also valid for OSD signals. During blanking and output clamping the video black level will be blanked to reference black level (**brightness blanking**).

7.2.3 Gain control (driven by I²C-bus, 6-bit DAC) and grey scale tracking

Gain control is used for white point adjustment (correction for different voltage to light amplification of the three colour channels) and therefore individual for the three channels. The video signals related to the reference black level can be gain controlled within a range of typical 7 dB.
The nominal setting is maximum gain. The video signal is the addition of the contrast controlled input signal and the brightness shift. The gain setting is also valid for OSD signals, thus the complete ‘grey scale’ is effected by gain control.

7.3 Output stage

In the output stage the nominal input signal will be amplified to $2.8V_{b\text{-}w}$ output colour signal at nominal contrast and maximum gain. The maximum input-output amplification at maximum contrast and gain settings is 16 dB. By **output clamping** the reference black level can be adjusted. In order to achieve very fast rise and fall times of the output signals with minimum crosstalk between the channels, each output stage has its own supply voltage and ground pin.

7.4 Pedestal blanking

For the video portion the reference black level should correspond to the ‘extended cut-off voltage’ at the cathode. During vertical flyback nevertheless retrace lines may be visible, though blanking to spot cut-off is useful. With control bit PEDST = 1 the pedestal black level will be adjusted by output clamping instead of the reference black level (see Fig.5). The pedestal black level is more negative than the video black level at minimum brightness setting and the voltage difference to reference black level is independent of any user control.

7.5 Output clamping, feedback references and DAC outputs

Aim of the output clamping (pins FB_1, FB_2 and FB_3) is to set the reference black level of the signal outputs to a value which corresponds to the ‘extended cut-off voltage’ of the CRT cathodes. At lack of output clamping pulses the integrated storage capacitors will discharge resulting in output signals going to switch-off voltage. Feedback references are driven by the I²C-bus.

1. **Control bit FPOL = 0**

   The cathode voltage (DC-coupled) is divided by a voltage divider and fed back to the IC. During the **output clamping pulse** it is compared with an adjustable feedback reference voltage with a range of 5.8 to 4.0 V. Any difference will lead to a reference black level correction (control bit PEDST = 0) or pedestal black level correction (control bit PEDST = 1) by charging or discharging the integrated capacitor which stores the black level information between the output clamping pulses. The DC voltages of the output stages should be designed in such a way that the reference black level/pedestal black level is within the range of 0.5 to 2.5 V. The reference voltages are also fed to the DAC output pins (REF_1, REF_2 and REF_3).

   For correct operation it is necessary that there is enough room for ultra black signals (negative brightness setting, pedestal black level if control bit PEDST = 1). Any clipping with the video supply voltage can disturb signal rise/fall times or the black level stabilization.

2. **Control bit FPOL = 1**

   For applications with AC-coupled cathodes positive feedback can be taken directly or divided by a voltage divider from the signal outputs or the emitter of an external emitter follower. During the output clamping pulse it is compared with a fixed reference voltage of 0.7 V.

   For black level restoration the DAC outputs (REF_1, REF_2 and REF_3) with a range of 5.8 to 4.0 V can be used.

   The use of **pedestal blanking** allows a very simple black level restoration with a DC diode clamp instead of a complicated pulse restoration circuit because the pedestal black level is the most negative output signal.

7.6 Clamping and blanking pulses

The pin CLI of TDA4885 can be directly connected to pin CLBL of e.g. TDA4855 sync processor for input clamping pulses and vertical blanking pulses.
The threshold for the input clamping pulse (typical 3 V) is higher than the threshold for the vertical blanking pulse (typical 1.4 V) but there must be no blanking during input clamping. Thus vertical blanking only is enabled if no input clamping is detected. For this reason the input clamping pulse must have rise/fall times faster than 75 ns/V during the transition from 1.2 to 3.5 V and opposite. The internal vertical blanking pulse will be delayed by typical 290 ns.

During the vertical blanking pulse at pin CLI **signal blanking**, **brightness blanking** and with control bit PEDST = 1 **pedestal blanking** will be activated. Input clamping pulses during vertical blanking will not switch off blanking.

For proper **input clamping** the input signals have to be at black level during the input clamping pulse.

An input pulse at pin HFB (e.g. horizontal flyback pulse) will be scanned with two thresholds. If the input pulse exceeds the first one (typical 1.4 V) **signal blanking**, **brightness blanking** and if control bit PEDST = 1 **pedestal blanking** will be activated. If the input pulse exceeds the second one (typical 3 V) additionally **output clamping** will be activated. The vertical blanking pulse can also be mixed with the horizontal flyback pulse at pin HFB.

7.7 On Screen Display (OSD)

If the fast blanking input signal at pin FBL exceeds the threshold (typical 1.4 V) the input signals are blanked (**signal blanking**) and OSD signals are enabled. Then any signal at pins OSD_1, OSD_2 or OSD_3 exceeding the same threshold will create an insertion signal with an amplitude of 125% of the nominal colour signal (approximately 80% of the maximum colour signal). The amplitude can be controlled by OSD contrast (driven by I²C-bus) with a range of 12 dB. The OSD signals are inserted at the same point as the contrast controlled input signals and will be treated with brightness and gain control like normal input signals.

With control bit DISO = 1 OSD, signal insertion and fast blanking (pin FBL) are disabled.

7.8 Limiting by contrast reduction

Beam current limiting is possible with an external voltage at pin LIM. The maximum overall voltage gain of contrast (and OSD contrast) control can be reduced by a voltage between 4.5 V (start of reduction) and 2.0 V (−26 dB) without effecting the contrast bit resolution. By setting the maximum voltage at pin LIM to less than 4.5 V the maximum gain is reduced for all channels (subcontrast setting). The open-circuit pin will have a voltage of approximately 5.0 V but is very high-ohmic and should be tied to a voltage source of 5.0 V or higher or should be connected to a capacitance of some nF if not used.

7.9 Gain modulation

To achieve brightness uniformity over the screen scan dependent gain modulation is possible. With open-circuit pins the gain will be reduced by 20% giving the possibility of symmetrical gain modulations (±18%) with ±1 V related to the open-circuit voltage of about 2.0 V at any gain setting.

If the gain modulation feature will not be used pins GM_1, GM_2 and GM_3 should be grounded to profit by maximum voltage gain.

7.10 I²C-bus control

The TDA4885 contains an I²C-bus receiver for several control functions:

1. Contrast control with 6-bit DAC
2. Brightness control with 6-bit DAC
3. OSD contrast control with 4-bit DAC
4. Gain control for each channel with 6-bit DAC
5. Internal feedback reference and external reference voltage control for each channel with 8-bit DAC
6. Control register with control bits FPOL, DISV, DISO and PEDST
7. Test register for production tests only.

All registers are set to logic 0 (minimum value for control registers) after power-up and after internal power-on reset of the I²C-bus.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
$V_{P1, 2, 3}$	supply voltage channel 1, 2 and 3 (pins 29, 24 and 19)	0	8.8	V
V_i	input voltage (pins 6, 8 and 10)	–0.1	V_P	V
V_{ext}	external DC voltage applied to the following pins:			
	pins 1 to 4	–0.1	V_P	V
	pins 12, 13, 14 and 17	–0.1	V_P	V
	pins 11 and 5	–0.1	V_P + 0.7	V
	pins 15 and 16	–0.1	V_P	V
	pins 31, 26 and 21	–0.1	V_P + 0.7	V
	pins 30, 25 and 20	note 1	note 1	
	pins 32, 27 and 22	–0.1	V_P	V
$I_{o(av)}$	average output current (pins 30, 25 and 20)	–	20	mA
I_{OM}	peak output current (pins 30, 25 and 20)	–	50	mA
P_{tot}	total power dissipation	–	1300	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
T_j	junction temperature	–25	+150	°C
V_{ESD}	electrostatic handling for all pins			
	machine model 0.75 μH (note 2)	–250	+250	V
	human body model (note 3)	–3000	+3000	V

Notes

1. No external voltages.
2. Equivalent to discharging a 200 pF capacitor via a 10 Ω series resistor (*"UZW-B0/FQ-B302"*).
3. Equivalent to discharging a 100 pF capacitor via a 1500 Ω series resistor (*"UZW-B0/FQ-A302"*).

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

10 CHARACTERISTICS

All voltages and currents are measured in test circuit of Fig.19; all voltages are measured with respect to GND (pins 9, 28, 23 and 18); $V_P = V_{P1, 2, 3} = 8$ V (pins 7, 29, 24 and 19); $T_{amb} = 25$ °C; nominal input signals [0.7 V (peak-to-peak value) at pins 6, 8 and 10]; nominal colour signals at signal outputs (pins 30, 25 and 20); reference black level (V_{rbl}) approximately 0.7 V; nominal settings for brightness and contrast; maximum settings for OSD contrast and gain; no limiting of contrast ($V_{17} = 5$ V); no OSD fast blanking (pin 1 connected to ground); no gain modulation (pins 12, 13 and 14 connected to ground); notes 1 to 3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 7)		7.6	8.0	8.8	V
I_P	supply current (pin 7)	note 4	–	20	25	mA
$V_{P1, 2, 3}$	channel supply voltage (pins 29, 24 and 19)		7.6	8.0	8.8	V
$I_{P1, 2, 3}$	channel supply current (pins 29, 24 and 19)	signal outputs (pins 30, 25 and 20) open-circuit; $V_{rbl} = 0.7$ V; note 5	–	40	45	mA
V_{PSO}	supply voltage for signal switch off (threshold at pin 7)	signal outputs switched to switch-off voltage; note 1	–	–	7.2	V
Clamping and blanking pulses (pins 5 and 11)						
V_5	input clamping and vertical blanking input signal	note 6				
		no blanking, no input clamping	–0.1	–	+1.2	V
		blanking, no input clamping	1.6	–	2.6	V
		input clamping, no blanking	3.5	–	V_P	V
I_5	input current	$V_5 = 1$ V; note 7	–1.5	–0.2	–0.05	µA
		pin 5 grounded; note 7	–80	–60	–30	µA
		$V_5 = -0.1$ V; note 7	–250	–200	–100	µA
$t_{r/f5}$	rise/fall time for input clamping pulse, disable for blanking	note 6; see Fig.7	–	–	75	ns/V
t_{W5}	width of input clamping pulse		0.6	–	–	µs
t_{dl5}	delay between leading edges of vertical blanking input pulse and internal blanking pulse	$V_{11} < 0.8$ V; input pulse with 50 ns/V; threshold for rising input pulse $V_5 = 1.4$ V; threshold after input clamping pulse $V_5 = 3$ V; see Fig.7	–	270	–	ns
t_{dt5}	delay between trailing edges of vertical blanking input pulse and internal blanking pulse	$V_{11} < 0.8$ V; input pulse with 50 ns/V; threshold $V_5 = 1.4$ V; see Fig.7	–	115	–	ns
V_{11}	output clamping and blanking input signal	note 8				
		no blanking, no output clamping	–0.1	–	+0.8	V
		blanking, no output clamping	2.0	–	2.6	V
		blanking, output clamping	3.5	–	V_P	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{11}	input current	V_{11} = 0.8 V; note 7	–3	–0.4	–0.1	µA
		pin 5 grounded; note 7	–80	–60	–30	µA
		V_5 = –0.1 V; note 7	–250	–200	–100	µA
Video signal inputs (channel 1: pin 6; channel 2: pin 8; channel 3: pin 10)						
$V_{i(b-w)6, 8, 10}$	positive input signal referred to black		–	0.7	1.0	V
$V_{I(clamp)6, 8, 10}$	DC voltage during input clamping	note 9	–	4	–	V
$I_{I6, 8, 10}$	DC input current	no input clamping; $V_{I6, 8, 10} = V_{I(clamp)6, 8, 10}$; T_{amb} = –20 to +70 °C	0.02	0.20	0.35	µA
		during input clamping; $V_{I6, 8, 10} = V_{I(clamp)6, 8, 10}$ ±0.7 V	±110	±150	±190	µA
$\lvert Z_{i6, 8, 10} \rvert$	magnitude of signal input impedance	f = 100 MHz; $V_{I(DC)6, 8, 10} = V_{I(clamp)6, 8, 10}$	500	–	–	Ω
$C_{i6, 8, 10}$	input capacitance against ground		–	–	3	pF
Signal blanking						
$\alpha_{ct(bl)}$	crosstalk suppression from input to output during blanking	control bit DISV = 1; f = 80 MHz	20	30	–	dB
		control bit DISV = 1; f = 135 MHz	10	15	–	dB
$t_{d11(sig)l}$	delay between blanking input (leading edge) and output signal blanking	see Fig.8	–	55	–	ns
$t_{d11(sig)t}$	delay between blanking input (trailing edge) and output signal blanking	see Fig.8	–	25	–	ns
Clipping (measured at signal outputs)						
ΔV_{clipp}	offset during sync clipping related to nominal colour signal	$V_{I6, 8, 10} = V_{I(clamp)6, 8, 10}$; note 10; see Fig.3	–	1	2	%
Contrast control; see Fig.9 and note 11						
d_C	colour signal related to nominal colour signal	3FH (maximum)	–	4	–	dB
		26H (nominal)	–	0	–	dB
		00H (minimum)	–	–28	–	dB
ΔG_{track}	tracking of output colour signals of channels 1, 2 and 3	3FH to 00H; note 12	–	0.0	0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast blanking (pin 1) and OSD signal insertion (channel 1: pin 2; channel 2: pin 3; channel 3: pin 4); note 13						
V_1	fast blanking input signal	no video signal blanking, OSD signal insertion disabled	0	–	1.1	V
		video signal blanking, OSD signal insertion enabled	1.7	–	$V_P - 1$	V
$V_{2, 3, 4}$	OSD input signal	$V_1 > 1.7$ V				
		no internal OSD signal insertion	0	–	1.1	V
		internal OSD signal insertion	1.7	–	$V_P - 1$	V
$t_{f(FBL)}$	fall time of colour signals (pins 30, 25 and 20)	90 to 10% amplitude; start of fast blanking pulse at pin 1 with 1.2 ns/V; note 14; see Fig.10	–	–	10	ns
$t_{r(FBL)}$	rise time of colour signals (pins 30, 25 and 20)	10 to 90% amplitude; end of fast blanking pulse at pin 1 with 1.2 ns/V; note 14; see Fig.10	–	–	10	ns
$t_{r(OSD)}$	rise time of OSD colour signals	10 to 90% amplitude; input pulse with 1.2 ns/V; see Fig.10	–	–	4	ns
$t_{f(OSD)}$	fall time of OSD colour signals	90 to 10% amplitude; input pulse with 1.2 ns/V; see Fig.10	–	–	7	ns
$t_{g(CO)}$	width of (negative going) OSD signal insertion glitch, leading edge	identical pulses with 1.2 ns/V at fast blanking input (pin 1) and OSD signal inputs (pins 2, 3 and 4); note 15; see Fig.10	–	–	6	ns
$t_{g(OC)}$	width of (negative going) OSD signal insertion glitch, trailing edge	identical pulses with 1.2 ns/V at fast blanking input (pin 1) and OSD signal inputs (pins 2, 3 and 4); note 15; see Fig.10	–	–	6	ns
dV_{OSD}	overshoot/undershoot of OSD colour signal related to actual OSD output pulse amplitude	OSD input pulse (pins 2, 3 and 4) with 1.2 ns/V; $V_1 > 1.7$ V	–	13	20	%
t_{over}	time of OSD signal overshoot exceeding 10%	OSD input pulse (pins 2, 3 and 4) with 1.2 ns/V; $V_1 > 1.7$ V	–	–	2	ns
$V_{OSD(max)}$	maximum OSD colour signal related to nominal colour signal	maximum OSD contrast; maximum gain; pins 12, 13 and 14 connected to ground	100	125	150	%
OSD contrast control; see Fig.11 and note 16						
d_{OC}	OSD colour signal related to maximum OSD colour signal	00H (minimum)	–14	–12	–10	dB
		0FH (maximum)	–	0	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting (pin 17); see Fig.9 and note 17						
$V_{17(nom)}$	input voltage	pin 17 open-circuit	4.7	5.0	5.3	V
$V_{17(start)}$	starting voltage for contrast and OSD contrast reduction		4.2	4.5	4.8	V
$V_{17(stop)}$	stop voltage for contrast and OSD contrast reduction	–32 dB below maximum colour signal (contrast setting 3FH)	1.5	2.0	2.5	V
I_{17}	maximum input current	V_{17} = 0 V	–1.0	–0.5	–0.1	μA
Brightness control; see Fig.12 and notes 18 and 19						
ΔV_{bl}	difference between black level and reference black level at signal outputs related to nominal colour signal	3FH (maximum)	+25	+30	+35	%
		10H (nominal)	–2	0	+2	%
		00H (minimum)	–12	–10	–8	%
ΔV_{BT}	difference of ΔV_{bl} between any two channels related to nominal colour signal		–1.2	0	+1.2	%
Brightness blanking						
$t_{d11(br)l}$	delay between blanking input at pin 11 (leading edge) and brightness blanking at signal outputs	see Fig.8	–	–	60	ns
$t_{d11(br)t}$	delay between blanking input at pin 11 (trailing edge) and brightness blanking at signal outputs	see Fig.8	–	–	60	ns
Gain control; see Fig.13 and note 20						
d_G	video signal related to video signal at maximum gain	00H (minimum)	–8	–7	–6	dB
		3FH (maximum)	–	0	–	dB
Gain modulation (channel 1: pin 12; channel 2: pin 13; channel 3: pin 14)						
$V_{12, 13, 14}$	input voltage	symmetrical modulation	1.0	–	3.0	V
		modulation feature not in use	–	–	0	V
		nominal: pins 12, 13 and 14 open-circuit	1.8	2.0	2.2	V
$G_{mod1, 2, 3}$	gain modulation channels 1, 2 and 3	note 21; see Fig.14				
		pins 12, 13 and 14 grounded (modulation feature not in use)	112	120	130	%
		$V_{12, 13, 14}$ = 1 V (maximum)	112	118	124	%
		$V_{12, 13, 14}$ = 2 V	–	100	–	%
		$V_{12, 13, 14}$ = 3 V (minimum)	76	82	88	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pedestal blanking						
$\Delta V_{30, 25, 20PED}$	difference of pedestal black level to video black level at nominal brightness at signal output pins related to nominal colour signal	note 22; see Fig.5	–18	–16	–14	%
$\Delta V_{30, 25, 20PED(T)}$	variation of $\Delta V_{30, 25, 20PED}$ with temperature related to nominal colour signal	T_{amb} = –20 to +70 °C	–0.8	0	+0.8	%
Signal outputs (channel 1: pin 30; channel 2: pin 25; channel 3: pin 20)						
$V_{30, 25, 20(b-w)}$	nominal colour signal	nominal contrast; maximum gain; pins 12, 13 and 14 grounded; $V_{I(b-w)}$ = 0.7 V; without load	2.5	2.8	3.1	V
$V_{30, 25, 20(max)}$	maximum colour signal	maximum contrast; maximum gain; pins 12, 13 and 14 grounded; $V_{I(b-w)}$ = 0.7 V; without load	4.0	4.5	5	V
$V_{30, 25, 20(min)}$	switch-off voltage (minimum output voltage level)		–	0.05	0.1	V
$V_{30, 25, 20(max)}$	maximum output voltage level	at arbitrary input signals, contrast, brightness and gain adjustments; without load	V_P – 2	–	V_P – 1	V
$R_{30, 25, 20}$	output resistance		–	80	–	Ω
$I_{30, 25, 20}$	maximum source current		–15	–	–	mA
$I_{30, 25, 20M(source)}$	peak source current	during fast positive signal transients	–40	–	–	mA
$I_{30, 25, 20M(sink)}$	peak sink current	during fast negative signal transients	–	–	20	mA
S/N	signal-to-noise ratio	note 23	44	50	–	dB
$D_{30, 25, 20(th)}$	output thermal distortion	note 24	–	–	0.6	%
Frequency response at signal outputs (channel 1: pin 30; channel 2: pin 25; channel 3: pin 20)						
$\Delta G_{30, 25, 20(f)}$	amplification decrease by frequency response	f = 135 MHz (small signal)	–	1.2	3.0	dB
$t_{r(30, 25, 20)}$	rise time of fast transients	10 to 90% amplitude; nominal colour signal; note 25	–	2.7	3	ns
$t_{f(30, 25, 20)}$	fall time of fast transients	90 to 10% amplitude; nominal colour signal; note 25	–	3.9	4.3	ns
$dV_{30, 25, 20}$	over/undershoot of output signal pulse related to actual output pulse amplitude	input rise/fall time = 1 ns; nominal colour signal	–	5	10	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crosstalk at signal outputs (channel 1: pin 30; channel 2: pin 25; channel 3: pin 20)						
$\alpha_{ct(tr)}$	transient crosstalk suppression	input rise/fall time = 1 ns; note 26	10	25	–	dB
$\alpha_{ct(f)}$	crosstalk suppression by frequency	f = 50 MHz	25	30	–	dB
		f = 100 MHz	10	20	–	dB
Internal feedback reference voltage; see Fig.15 and note 27						
$V_{ref(n)}$	internal reference voltage for negative feedback polarity	FFH; FPOL = 0	3.8	4.0	4.2	V
		00H; FPOL = 0	5.6	5.8	6.1	V
$V_{ref(p)}$	fixed internal reference voltage for positive feedback polarity	FPOL = 1	0.6	0.7	0.8	V
$\Delta V_{ref}/\Delta T$	variation of $V_{ref(n)}$ and $V_{ref(p)}$ in the temperature range	T_{amb} = –20 to +70 °C	0	–	±1.0	%
$\Delta V_{ref}/\Delta V_P$	variation of $V_{ref(n)}$ and $V_{ref(p)}$ with supply voltage V_P	7.6 V ≤ V_P ≤ 8.8 V	0	–	±1.0	%
External reference voltages (REF_1: pin 32; REF_2: pin 27; REF_3: pin 22); see Fig.16 and note 28						
$V_{32, 27, 22}$	external reference voltage (equal to internal reference voltage with control bit FPOL = 0)	FFH	3.8	4.0	4.2	V
		00H	5.6	5.8	6.1	V
$\Delta V_{32, 27, 22}/\Delta T$	variation of $V_{32, 27, 22}$ in the temperature range	T_{amb} = –20 to +70 °C	0	–	±1.0	%
$\Delta V_{32, 27, 22}/\Delta V_P$	variation of $V_{32, 27, 22}$ with supply voltage V_P	7.6 V ≤ V_P ≤ 8.8 V	0	–	±1.0	%
$R_{32, 27, 22}$	output resistance		–	90	–	Ω
$I_{32, 27, 22}$	maximum sink current		–	–	400	µA
$I_{32, 27, 22}$	maximum source current		–	–330	–280	µA
Output clamping, feedback inputs (channel 1: pin 31; channel 2: pin 26; channel 3: pin 21)						
$I_{31, 26, 21(max)}$	maximum input current	during output clamping; V_{11} > 3.5 V; $V_{31, 26, 21}$ = 0.5 V	–500	–100	–60	nA
$V_{30, 25, 20rbl(min)}$	minimum reference black level	PEDST = 0; V_{11} > 3.5 V	0.01	0.1	0.5	V
	minimum pedestal black level	PEDST = 1; V_{11} > 3.5 V	0.01	0.1	0.5	V
$V_{30, 25, 20rbl(max)}$	maximum reference black level	PEDST = 0; V_{11} > 3.5 V	2.4	2.8	4	V
	maximum pedestal black level	PEDST = 1; V_{11} > 3.5 V	2.4	2.8	4	V
$\Delta V_{bl(CRT)}$	black level variation at CRT	note 29	0	40	200	mV
$\Delta V_{bl(lf)}$	black level variation between clamping pulses related to nominal colour signal	line frequency 60 kHz; 10% duty cycle	–	0.1	0.5	%
t_{W11}	width of clamping pulse	measured at V_{11} = 3 V; see Fig.8	1	–	–	µs
$t_{d11(clamp)l}$	delay between clamping input at pin 11 (leading edge) and start of internal output clamping pulse	see Fig.8	–	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d11(clamp)t}$	delay between clamping input at pin 11 (trailing edge) and end of internal output clamping pulse	see Fig.8	–	–	60	ns
I²C-bus inputs (pins 15 and 16)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
V_{IL}	LOW-level input voltage		0.0	–	1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	5.0	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–10	μA
I_{IH}	HIGH-level input current	V_{IH} = 5 V	–	–	–10	μA
V_{OL}	LOW-level output voltage	during acknowledge	0.0	–	0.4	V
I_{ack}	output current at pin 15 during acknowledge	V_{OL} = 0.4 V	3.0	–	5.0	mA
$V_{th(POR)(r)}$	threshold for power-on reset on	rising supply voltage	–	1.5	2.0	V
		falling supply voltage	–	3.5	–	V
$V_{th(POR)(f)}$	threshold for power-on reset off	rising supply voltage	–	–	7.0	V
		falling supply voltage	–	1.5	–	V

Notes to the characteristics

1. Definition of levels (see Figs 3 to 5):

   Reference black level: this is the level to which the input level is clamped during the input clamping pulse (V_5 > 3.5 V). It is used internally as a reference for the gain settings. It can be observed on the outputs:

   a) when the input is at black and the brightness setting is nominal (subaddress 01H = 10H)

   b) during output blanking/clamping (V_{11} > 3.5 V) if control bit PEDST = 0.

   Video black level: this is the black level of the actual video. On the input it is still equal to the reference black level. On the output it may deviate from it according to the brightness setting. Contrast setting leaves the video black level unaltered.

   Pedestal black level: this is an ultra black level which deviates from reference black level by a fixed amount. It can be observed on the output during output blanking/clamping (V_{11} > 3.5 V) if control bit PEDST = 1.

   Switch-off voltage: this is the lowest signal voltage at outputs. The signals will be switched off by discharging the internal black level storage capacitors if the supply voltage is less than V_{PSO}.

   Blanking level: this level equals reference black (control bit PEDST = 0) or pedestal black (control bit PEDST = 1).

2. Explanation to black level adjustment:

   The actual blanking level on the output depends on the external feedback application. The loop will only function correctly if it is within the control range of $V_{30,\ 25,\ 20rbl(min)}$ to $V_{30,\ 25,\ 20rbl(max)}$. Note: changing control bit PEDST in a given application will not affect the blanking level, but instead shifts the video (and needs re-alignment of the three black levels).

   The three reference black levels are aligned correctly when they are made equal to the ‘extended cut-off levels’ of the three cathodes. Full raster and spot cut-off can only be achieved by enabling the pedestal blanking or by applying a negative pulse to grid 1.

3. Definition of output signals (see Fig.6):

   Colour signal: all positive voltages referred to black level at signal outputs.

   Nominal colour signal: colour signal with nominal input signal ($0.7V_{b\text{-}w}$), nominal contrast setting and maximum gain setting.

   Video signal: all positive voltages referred to reference black level at signal outputs. The video signal is the superposing of the brightness information (ΔV_{bl}) and the colour signal.

4. The total supply current $I_P = I_7 + I_{29} + I_{24} + I_{19}$ depends on the supply voltage with a factor of approximately 10 mA/V and varies in the temperature range of –20 to +70 °C by approximately ±10% ($V_{30, 25, 20} = 0.7$ V).

5. The channel supply current depends on the signal output current, the channel supply voltage and the signal output voltage. With $I_{px} = I_{29, 24, 19}$ at $V_{P1, 2, 3} = 8$ V and $V_{30, 25, 20} = 0.7$ V:

$$I_{29, 24, 19} \approx I_{px} + I_{30, 25, 20} + 3.1\ \frac{mA}{V} \times (V_{P1, 2, 3} - 8\ V) - 2.5\ \frac{mA}{V} \times (V_{30, 25, 20} - 0.7\ V)$$

6. Pin 5 should be used for input clamping and blanking during vertical retrace (signal blanking, brightness blanking and if control bit PEDST = 1 pedestal blanking). With a fast clamping pulse (transition between $V_5 = 1.2$ to 3.5 V and vice versa in less than 75 ns/V) no blanking will occur during input clamping.

   For 75 ns/V < $t_{r/f5} \leq$ 280 ns/V the generation of the internal vertical blanking pulse is uncertain, for $t_{r/f5}$ > 280 ns/V the internal blanking pulse will be generated.

   Pin 5 open-circuited will activate permanent input clamping and undefined blanking.

7. Input voltages less than –0.1 V can produce internal substrate currents which disturb the leakage currents at the signal inputs. An internal protection circuit creates a current for pin voltages of approximately 0 V or less. Feeding clamping/blanking pulses via a resistor of some kΩ protects the pin from negative voltages.

8. Pin 11 should be used for output clamping and/or blanking. Pin 11 open-circuited will activate permanent blanking and output clamping.

9. The DC voltage during input clamping is temperature dependent with a factor of approximately 0.5 V/100 °C ($3V_{BE}$).

10. Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below input reference black level (see Fig.3).

11. Contrast control acts on internal colour signals under I²C-bus control; subaddress 02H (bit resolution 1.6% of contrast range).

12. $$\Delta G_{track} = 20 \times \text{maximum of } \left\{ \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{20}}{A_2} \right) \right| ; \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{30}}{A_3} \right) \right| ; \left| \log\left(\frac{A_2}{A_{20}} \times \frac{A_{30}}{A_3} \right) \right| \right\} \text{ dB}$$

    A_x: colour signal output amplitude in channel x at any contrast setting.

    A_{x0}: colour signal output amplitude in channel x at nominal contrast and same gain setting.

13. When OSD fast blanking is active and $V_{2, 3, 4}$ are HIGH ($V_1 > 1.7$ V, $V_{2, 3, 4} > 1.7$ V) the OSD colour signals will be inserted in front of the gain potentiometers. This assures a correct grey scale of all video signals. The amplitudes of the inserted OSD signals can be controlled simultaneously by OSD contrast via I²C-bus.

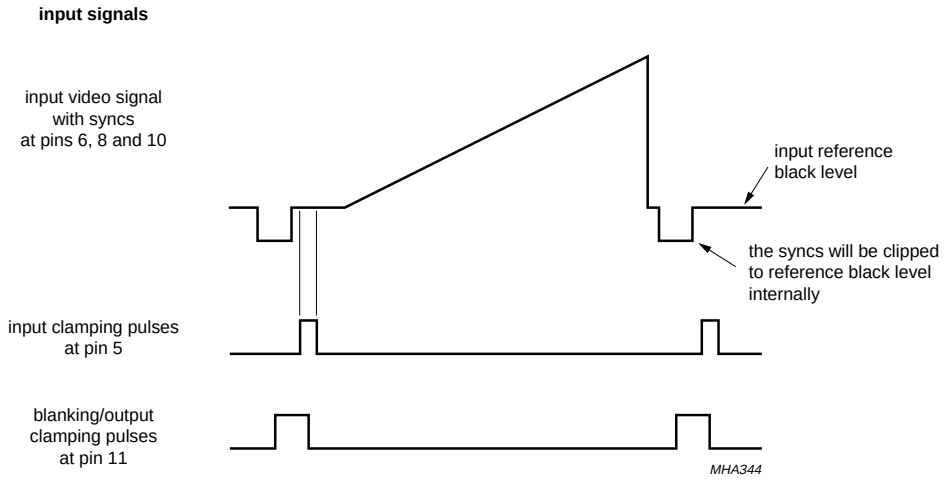
14. Typical pulse at fast blanking input (pin 1) and response at signal outputs (pins 30, 25 and 20) with nominal input signals at pins 6, 8 and 10.

15. Typical pulse at fast blanking input (pin 1) as well as OSD inputs (pins 2, 3 and 4) and response at signal outputs (pins 30, 25 and 20) during OSD fast blanking for maximum OSD contrast, maximum gain adjustment and pins 12, 13 and 14 grounded. Small internal threshold and delay differences between fast blanking and signal insertion might cause short signal distortion at begin and end of signal insertion (see Fig.10).

16. OSD contrast control acts on inserted OSD colour signals under I²C-bus control; subaddress 03H (bit resolution 6.7% of OSD contrast range).

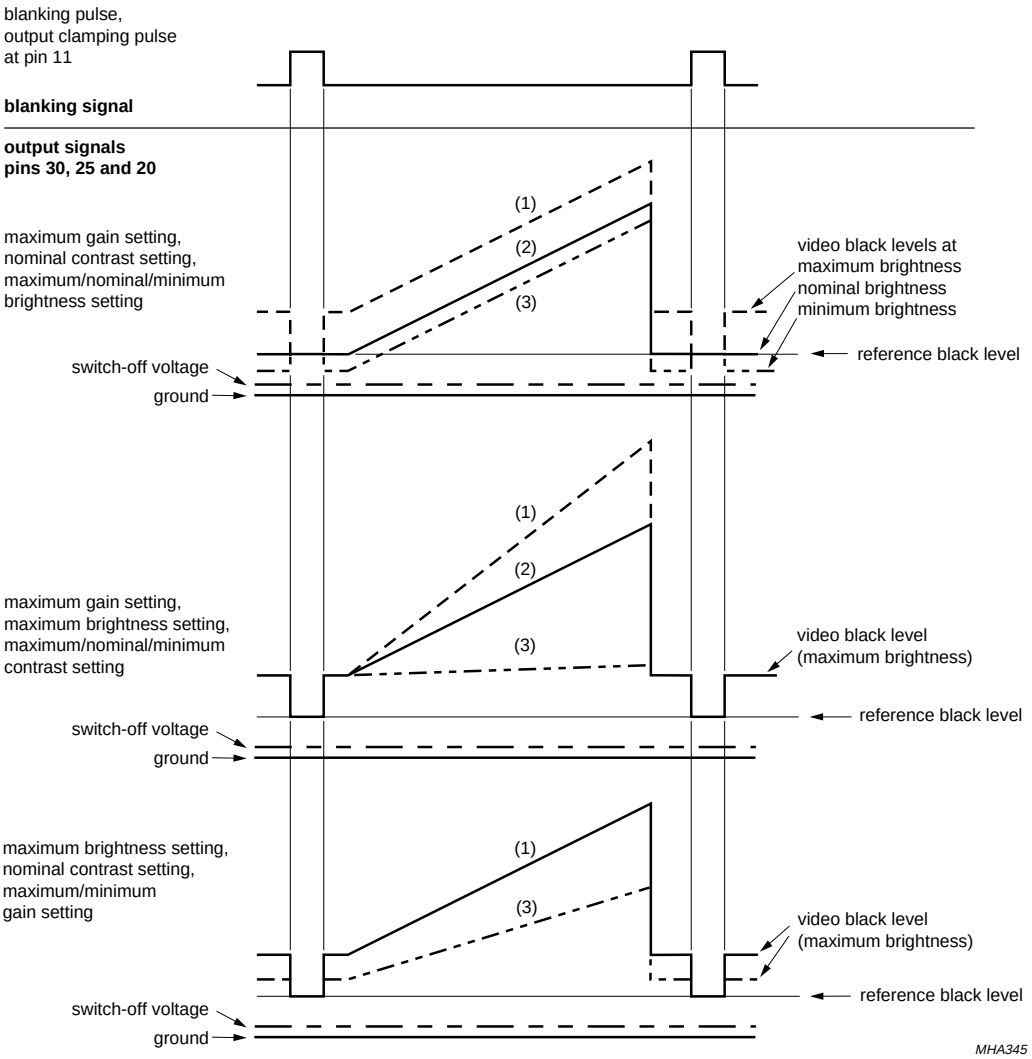
17. This pin can be used for beam current limiting or subcontrast setting. Both the video and OSD contrast are reduced simultaneously (see Figs 9 and 11). Because of the high-ohmic input impedance the pin should be tied to a voltage of more than 5 V or applied with a capacitor of some nF if not used.
18. Brightness control adds an I²C-bus controlled DC offset to the internal colour signal; subaddress 01H (bit resolution 1.6% of brightness range).
19. The voltage difference between video black level and reference black level is related to the colour signal with nominal 0.7 V (peak-to-peak value) input signal, at nominal contrast (subaddress 02H = 26H) and for any gain setting. The voltage difference is proportional to the gain setting (grey scale tracking). The given values of ΔV_{bl} are valid only for video black levels higher than the signal output switch-off voltage $V_{30,\ 25,\ 20(min)}$.
20. Gain control acts on video signals and inserted OSD video signals under I²C-bus control; subaddress 04H (channel 1), 05H (channel 2) and 06H (channel 3; bit resolution 1.6% of gain range).
21. The usage of the gain modulation capability results in a reduction of the overall voltage gain of the TDA4885 but gives enough room for positive and negative modulation. Only pins 12, 13 and 14 connected to ground makes it possible to reach the specified maximum video signals at pins 30, 25 and 20 (see Fig.14). By short-circuiting pins 12, 13 and 14 it is possible to assure that the relations between the video signals remain constant for any modulation (**common gain modulation**).
22. Pedestal blanking produces an ultra black level during blanking and output clamping which is the most negative signal at the signal output pins. The reference black level which should correspond to the 'extended cut-off voltage' at the cathodes is about $\Delta V_{30,\ 25,\ 20PED}$ higher (see Fig.5).
    The use of **pedestal blanking** with AC-coupled cathodes (control bit FPOL = 1) allows a very simple black level restoration with a DC diode clamp instead of a complicated pulse restoration circuit.
23. The signal-to-noise ratio is calculated by the formula (range 1 to 135 MHz):
    $$\frac{S}{N} = 20 \times \log \frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}} \text{ dB}$$
24. There might be short time smearing effects which have no thermal causes. The final amplitude will be reached some 10 ns after pulse step (amplitude differences of about 5%). For compensation methods see Section "Recommendations for building the application board" in Chapter "Test and application information".
25. Ideal input rise/fall time of 0 ns; $t^2_{r,\ out} = t^2_{r,\ ideal} + t^2_{r,\ in}$
26. Crosstalk between any two output pins:
    a) **Input conditions**: any channel (channel A) with nominal input signal and 1 ns rise time. The inputs of the other two channels are capacitively coupled to ground (channel B). Gain setting to maximum (3FH). Contrast setting to nominal (26H)
    b) **Output conditions**: black level set to 1 V for each channel at signal outputs. Output signals are V_A and V_B respectively
    c) **Transient crosstalk suppression**: $\alpha_{ct(tr)} = 20 \times \log \frac{V_A}{V_B}$ dB
27. Internal feedback reference voltage acts under I²C-bus control for control bit FPOL = 0; subaddress 07H (channel 1), 08H (channel 2) and 09H (channel 3; bit resolution 0.4% of voltage range). The internal feedback reference voltages can be measured at feedback inputs (pins 31, 26 and 21) during output clamping (V_{11} > 3.5 V) in closed feedback loop. The feedback loop remains operative at output levels between typically 0.1 to 2.8 V. The reference voltages are not influenced by the value of control bit PEDST. The levels of the internal feedback reference voltages depend on the individual adjustments via I²C-bus (values from 00H to FFH) and the selected feedback polarity (control bit FPOL = 0 or 1):
    a) **Control bit FPOL = 0**: rising values of the data bytes (subaddresses 07H, 08H and 09H), e.g. 00H to FFH, correspond to rising values of the resulting reference black levels at signal outputs (pins 30, 25 and 20)
    b) **Control bit FPOL = 1**: the internal feedback reference voltage remains constant.

28. The external reference voltages act under I²C-bus control independent from control bit FPOL; subaddress 07H (REF_1), 08H (REF_2) and 09H (REF_3; bit resolution 0.4% of voltage range).
29. Slow variations of video supply voltage V_{CRT} will be suppressed at CRT cathode by the clamping feedback loop. A change of V_{CRT} with 5 V leads to a specified change of the cathode voltage.



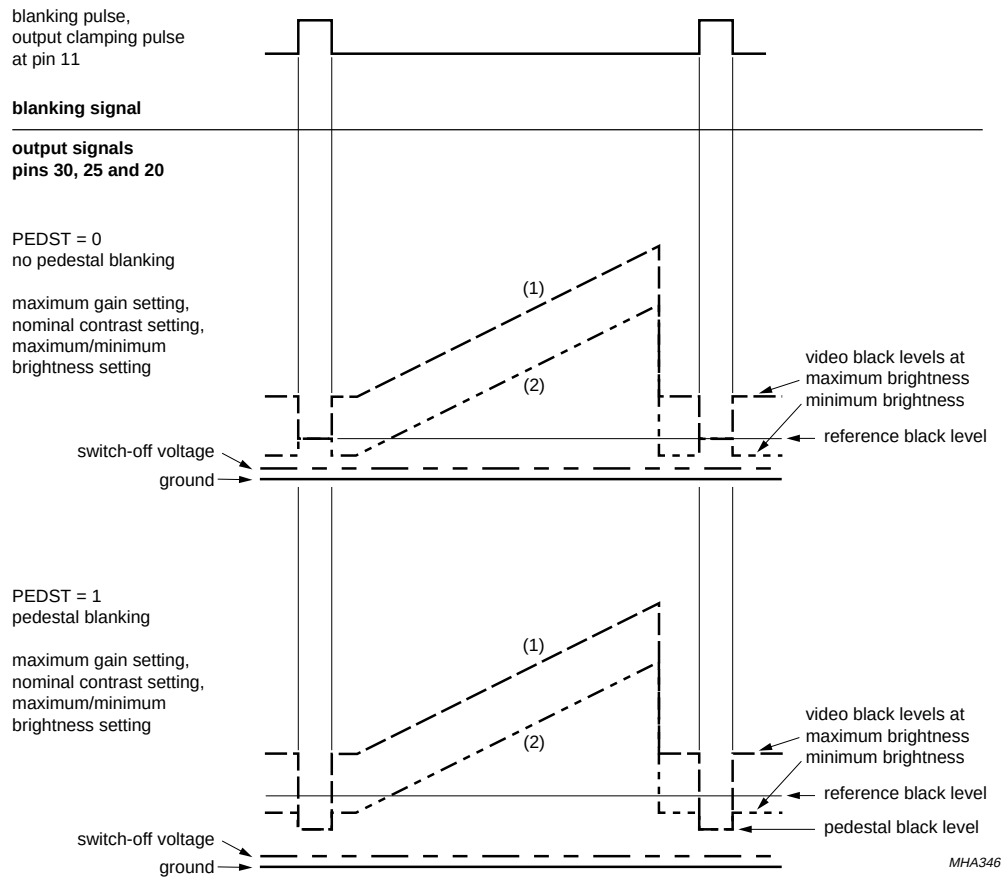
The input video signals have to be on black level during input clamping.

Fig.3 Input signals.



(1) Maximum.
(2) Nominal.
(3) Minimum.

Fig.4 Definition of levels, function of brightness setting, contrast setting, gain setting, no pedestal blanking (PEDST = 0).



(1) Maximum.
(2) Minimum.

Fig.5 Output signals without (PEDST = 0) and with pedestal blanking (PEDST = 1).

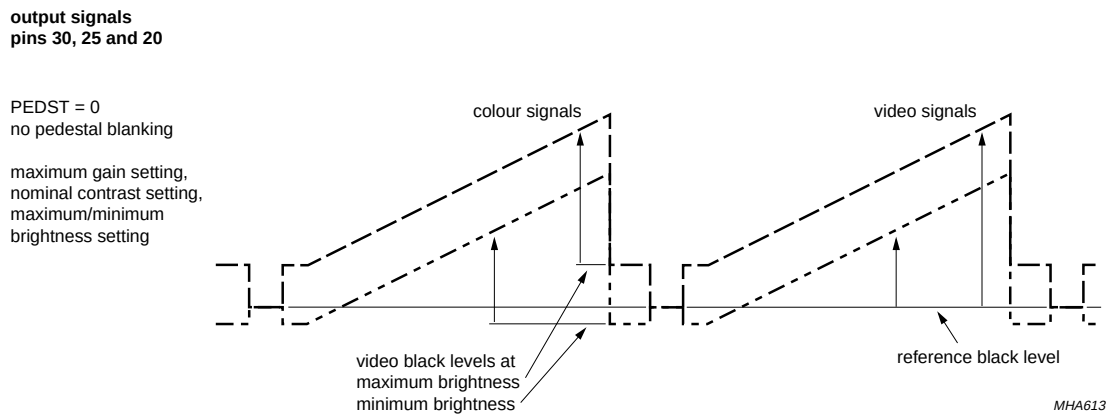


Fig.6 Definition of output signals.

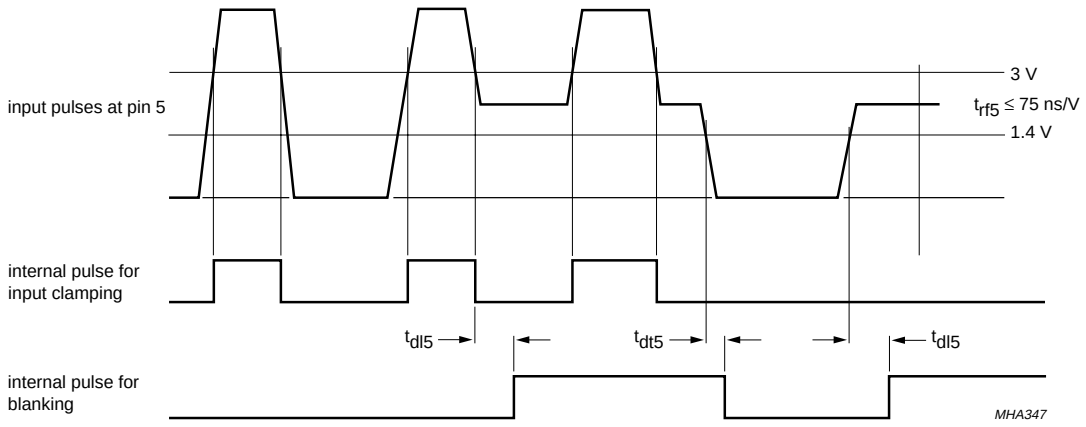


Fig.7 Timing of pulses at pin 5 and derived internal pulses.

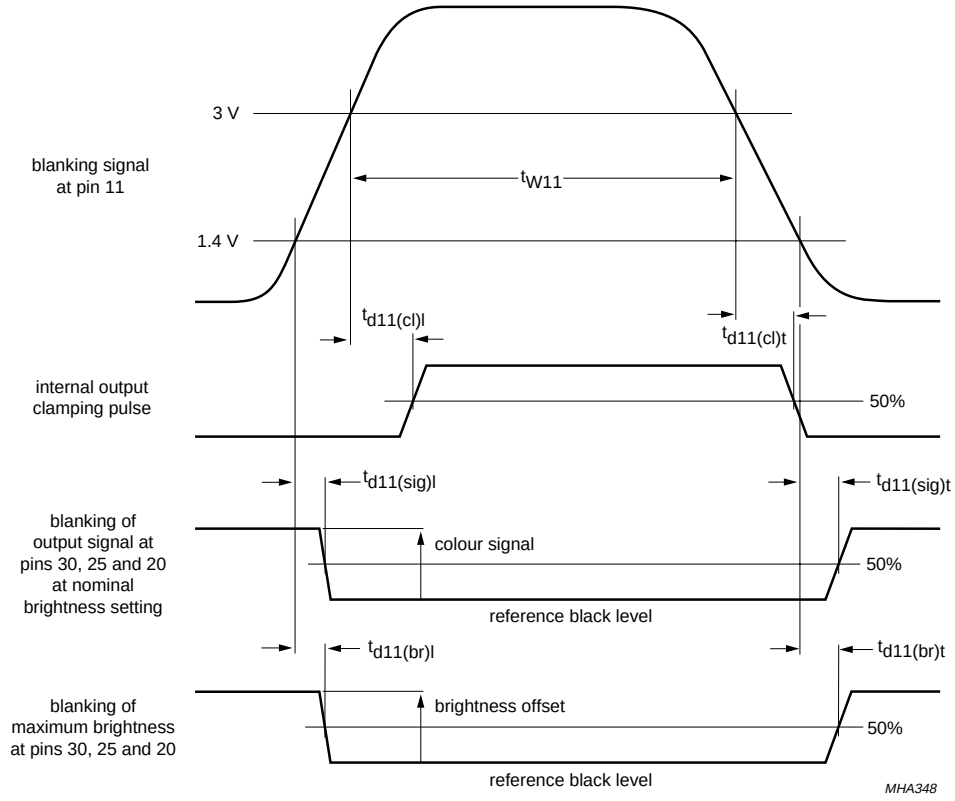
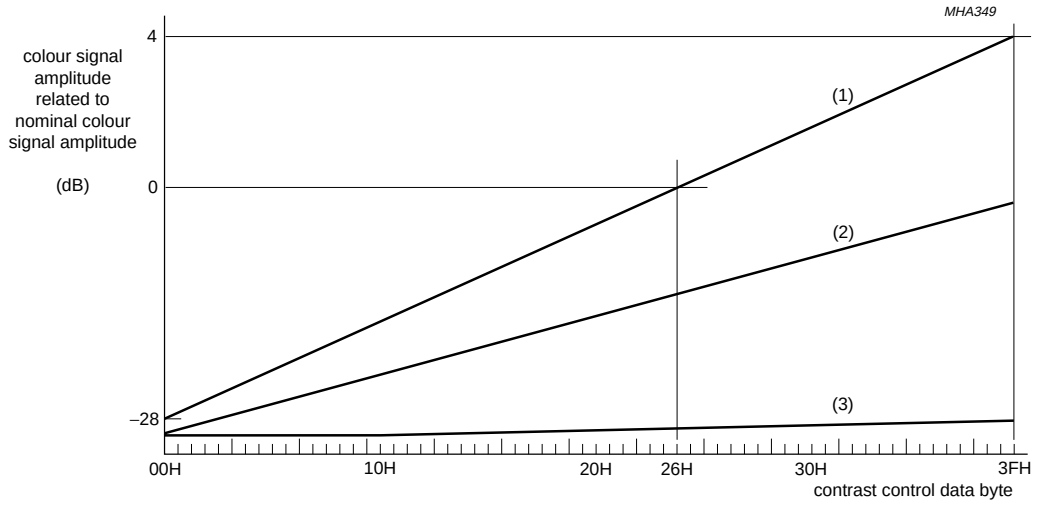
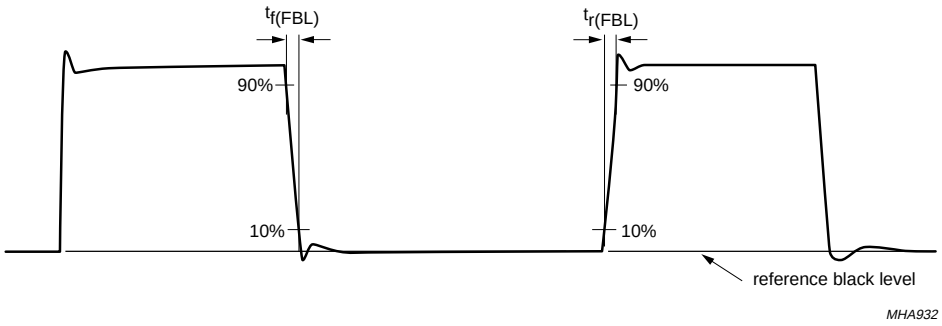


Fig.8 Delay between blanking input and output signal blanking, brightness blanking and output clamping.

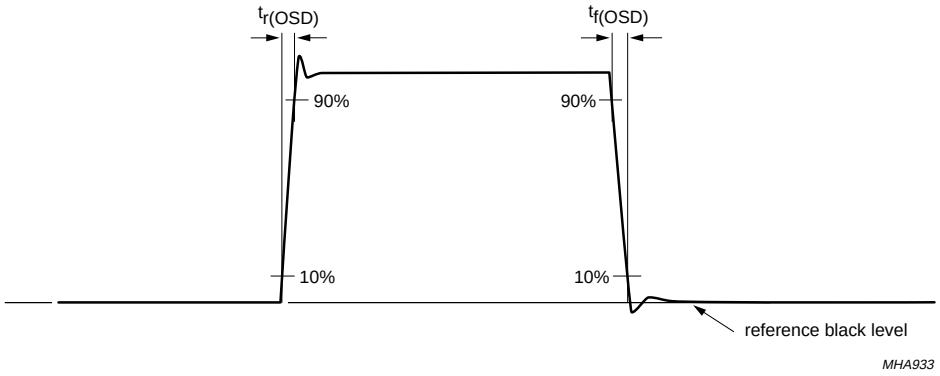


(1) No contrast reduction by limiting.
(2) Partial contrast reduction by limiting.
(3) Full contrast reduction by limiting.

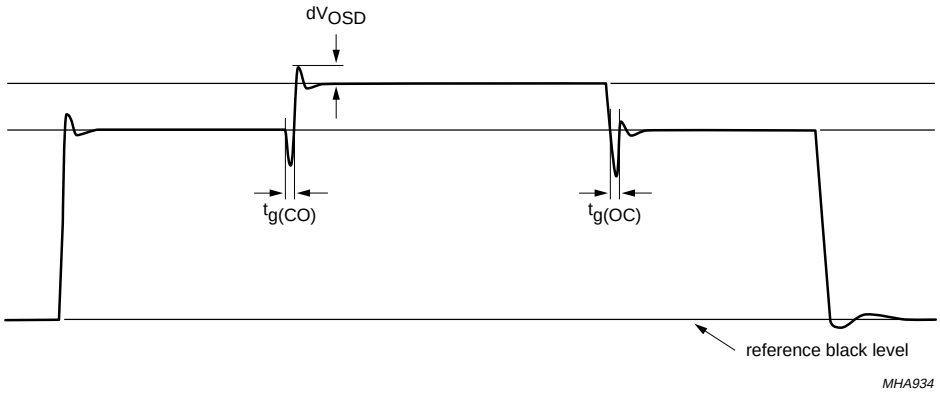
Fig.9 Contrast control characteristic with limiting.



a. Video signal with fast blanking at signal outputs (pins 30, 25 and 20).

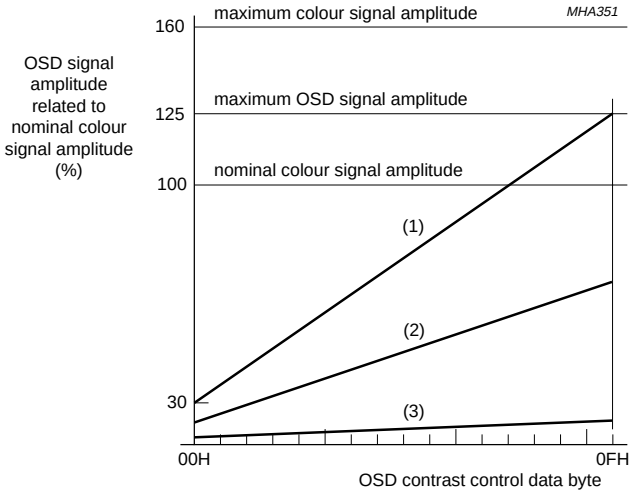


b. OSD signal without video signal at signal outputs (pins 30, 25 and 20).



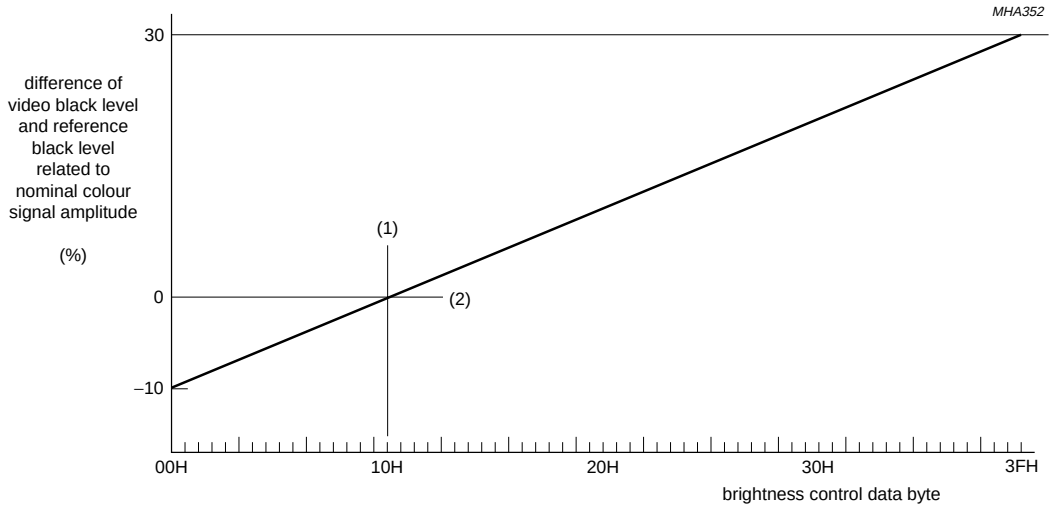
c. Video signal with OSD signal insertion at signal outputs (pins 30, 25 and 20). Identical input pulse at pin 1 (fast blanking) and pins 2, 3 and 4 (OSD signal).

Fig.10 OSD insertion.



(1) No OSD contrast reduction by limiting.
(2) Partial OSD contrast reduction by limiting.
(3) Full OSD contrast reduction by limiting.

Fig.11 OSD contrast control characteristic with limiting.



(1) Nominal adjustment.
(2) Nominal brightness reference black level.

Fig.12 Brightness control characteristic.

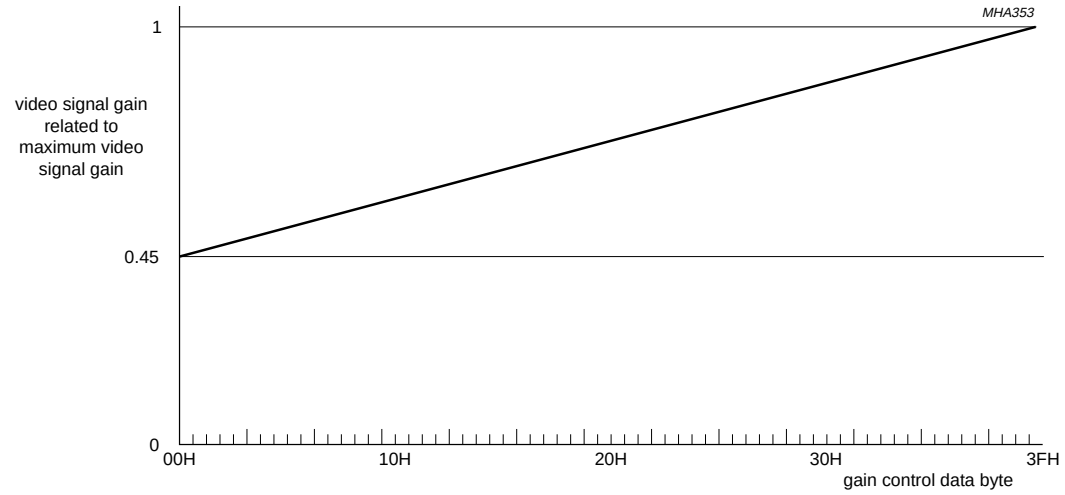
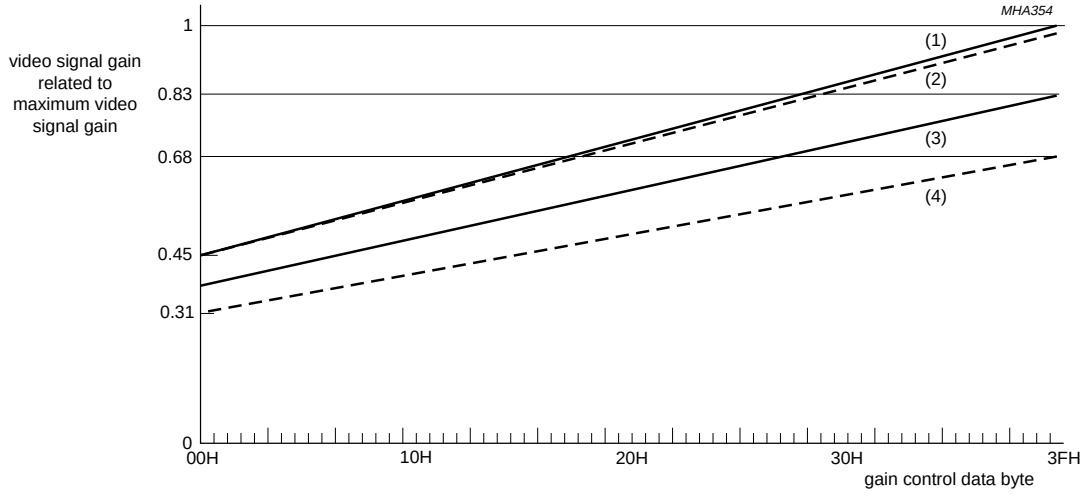
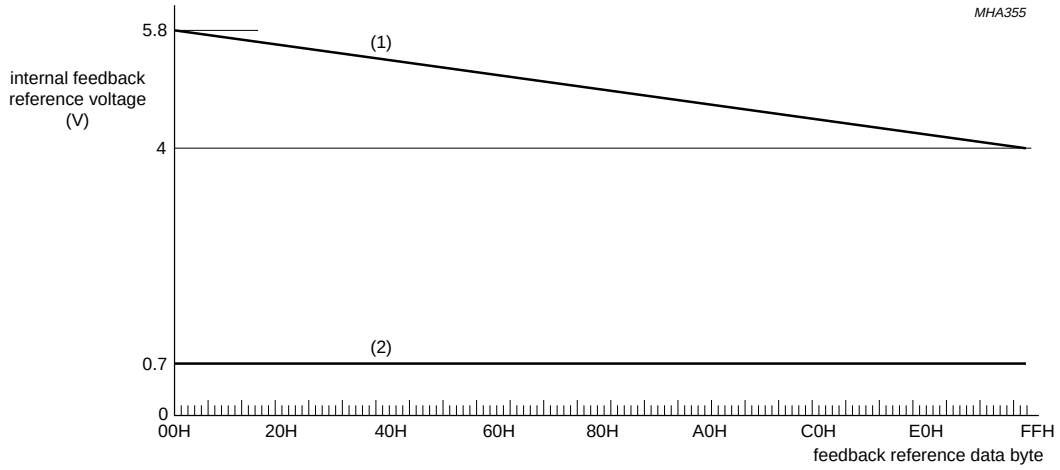


Fig.13 Gain control characteristic.



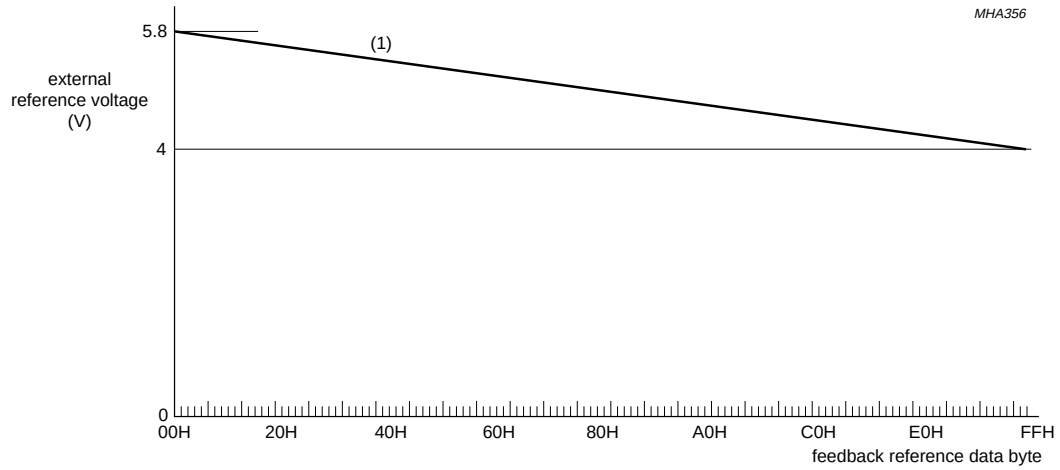
(1) Pin 12, 13 or 14 grounded.
(2) 1 V at pin 12, 13 or 14.
(3) Open-circuit pin 12, 13 or 14.
(4) 3 V at pin 12, 13 or 14.

Fig.14 Gain modulation.



(1) Control bit FPOL = 0.
(2) Control bit FPOL = 1.

Fig.15 Internal feedback reference voltages.



(1) Control bit FPOL = 0 or 1.

Fig.16 External feedback reference voltages.

11 I²C-BUS PROTOCOL

Table 1 Slave address

A6(1)	**A5**(1)	**A4**(1)	**A3**(1)	**A2**(1)	**A1**(1)	**A0**(1)	$\overline{\mathbf{W}}$(2)
1	0	0	0	1	0	0	0

Notes

1. Address bit.
2. Write bit.

Table 2 Slave receiver format

S(1)	SLAVE ADDRESS A(2)	SUBADDRESS A(3)	DATA BYTE A(4)	P(5)

Notes

1. START condition.
2. A = acknowledge.
3. All subaddresses within the range 00H to 09H are automatically incremented. The subaddress counter wraps around from 09H to 00H. The subaddress 0FH is reserved for test purposes under production. Do not use it. Subaddresses outside the range 00H to 0FH are acknowledged by the device but neither auto-increment nor any other internal operation takes place.
4. N data bytes with auto-increment of subaddresses.
5. STOP condition.

Table 3 Subaddress byte and data byte format

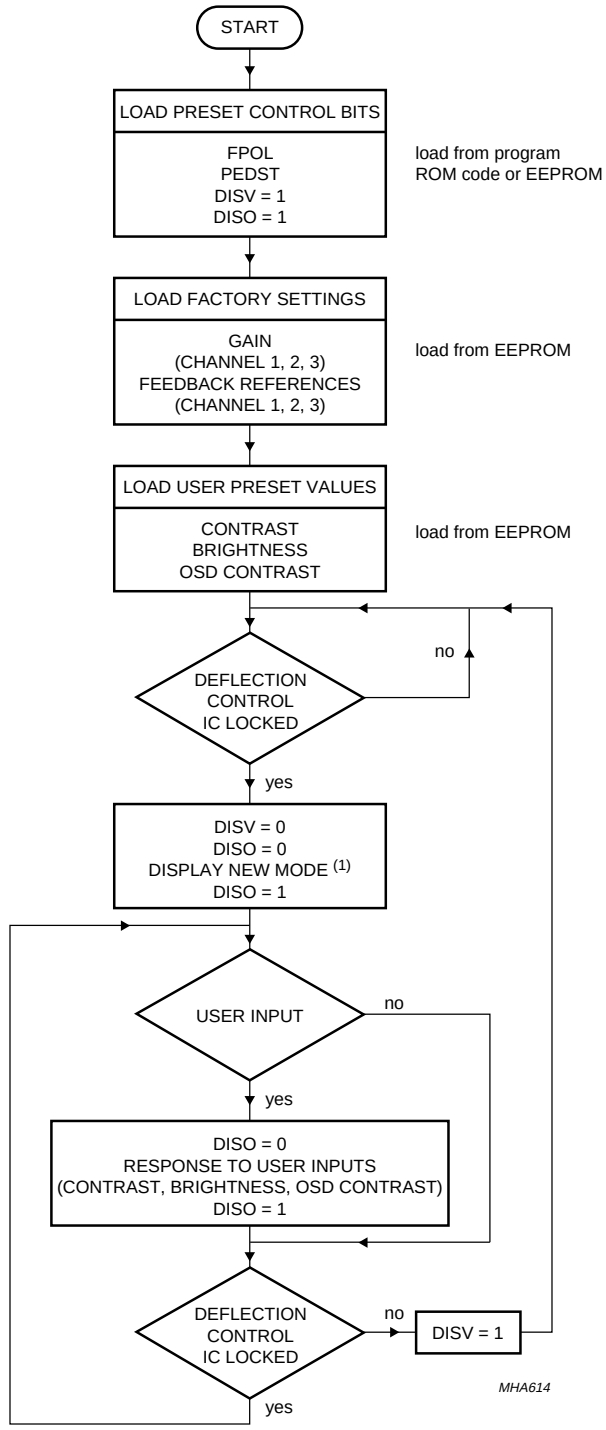
FUNCTION	SUB-ADDRESS	DATA BYTE(1)								NOMINAL VALUE(3)
		D7(2)	D6(2)	D5(2)	D4(2)	D3(2)	D2(2)	D1(2)	D0(2)	
Control register	00H	X(4)	X(4)	X(4)	X(4)	FPOL	DISV	DISO	PEDST	–
Brightness control	01H	X(4)	X(4)	A15	A14	A13	A12	A11	A10	10H
Contrast control	02H	X(4)	X(4)	A25	A24	A23	A22	A21	A20	26H
OSD contrast control	03H	X(4)	X(4)	X(4)	X(4)	A33	A32	A31	A30	0FH
Gain control channel 1	04H	X(4)	X(4)	A45	A44	A43	A42	A41	A40	3FH
Gain control channel 2	05H	X(4)	X(4)	A55	A54	A53	A52	A51	A50	3FH
Gain control channel 3	06H	X(4)	X(4)	A65	A64	A63	A62	A61	A60	3FH
Black level reference channel 1	07H	A77	A76	A75	A74	A73	A72	A71	A70	–
Black level reference channel 2	08H	A87	A86	A85	A84	A83	A82	A81	A80	–
Black level reference channel 3	09H	A97	A96	A95	A94	A93	A92	A91	A90	–
	0AH to 0EH	not used								–
Reserved (note 5)	0FH	X(4)	X(4)	X(4)	X(4)	X(4)	0	0	0	–

Notes

1. The least significant bit (LSB) of an analog alignment register is defined as AX0 (data bit D0).
2. Data bit.
3. After power-on reset control and test register are reset to logic 0 and all alignment registers are set to logic 0 (minimum).
4. X means don't care but for software compatibility with other video ICs with the same slave address, they are preferably set to logic 0.
5. For production tests only.

Table 4 Control register

BIT	FUNCTION
PEDST = 0	no pedestal blanking
PEDST = 1	pedestal blanking enabled
DISO = 0	OSD signals enabled
DISO = 1	OSD signals disabled
DISV = 0	video signals enabled
DISV = 1	video signals disabled
FPOL = 0	negative feedback polarity
FPOL = 1	positive feedback polarity

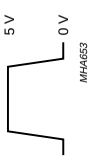
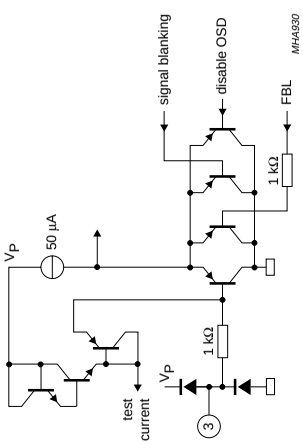
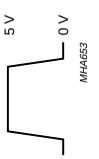
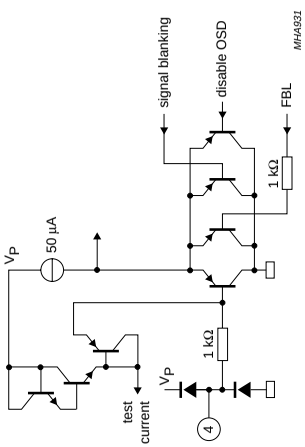


(1) Only synchronized video should be displayed.
Each new mode can be displayed by OSD.
It is recommended to synchronize data transmission (brightness, contrast and OSD contrast) with vertical blanking pulse.

Fig.17 I²C-bus control flow.

12 INTERNAL CIRCUITRY

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
1	FBL; fast blanking input for OSD insertion	open-circuit base		
2	OSD_1; OSD input channel 1	$V_2 < V_P - 1$ V: open-circuit base		
		$V_2 = V_P$: I_2 = 85 to 210 µA		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
3	OSD_2; OSD input channel 2	$V_3 < V_P - 1$ V: open-circuit base		
		$V_3 = V_P$: I_3 = 80 to 280 µA		
4	OSD_3; OSD input channel 3	$V_4 < V_P - 1$ V: open-circuit base		
		$V_4 = V_P$: I_4 = 80 to 280 µA		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
5	CLI; vertical blanking input (input clamping)	$V_5 > 0.2$ V: open-circuit base		
		$V_5 \leq 0.2$ V: source current rising with decreasing voltage		
6	V_{I1}; signal input channel 1	outside clamping pulse: open-circuit base with base current compensation		
		during clamping: $I_6 = -150$ to $+150$ µA		
7	V_P; supply voltage	20 mA		

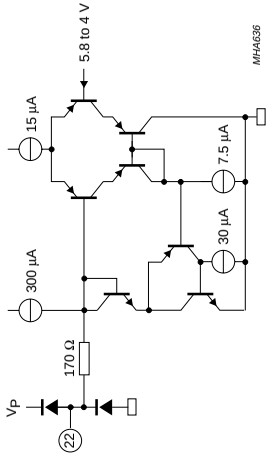
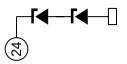
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
8	V_{I2}; signal input channel 2	outside clamping pulse: open-circuit base with base current compensation during clamping: I_6 = –150 to +150 µA		
9	GND; ground			
10	V_{I3}; signal input channel 3	outside clamping pulse: open-circuit base with base current compensation during clamping: I_6 = –150 to +150 µA		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
11	HFB; horizontal flyback input (output clamping, blanking)	V_{11} > 0.2 V: open-circuit base		
		$V_{11} \leq 0.2$ V: source current rising with decreasing voltage		
12	GM_1; gain modulation input channel 1	R_{12} = 20 kΩ; open-circuit voltage V_{12} = 2.0 V		
13	GM_2; gain modulation input channel 2	R_{13} = 20 kΩ; open-circuit voltage V_{13} = 2.0 V		

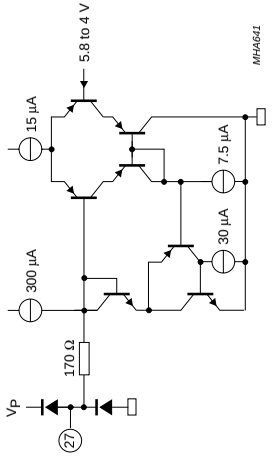
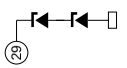
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
14	GM_3; gain modulation input channel 3	R_{14} = 20 kΩ; open-circuit voltage V_{14} = 2.0 V		
15	SDA; I²C-bus serial data input/output	no acknowledge; open-circuit base during acknowledge: I_{15} = 4 mA		
16	SCL; I²C-bus clock input	open-circuit base		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
17	LIM; beam current limiting input	open-circuit voltage V_{17} = 5.0 V		
		V_{17} < 4.5 V: open-circuit base		
18	GND_3; ground channel 3			
19	V_{P3}; supply voltage channel 3	I_{19} = 40 mA		

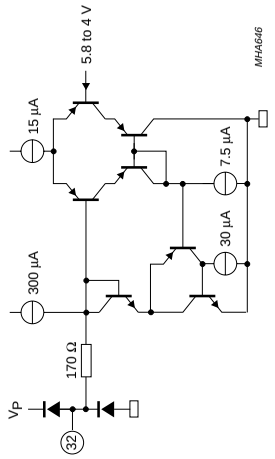
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
20	V_{O3}; signal output channel 3	reference black level 0.1 to 2.8 V	control bit PEDST = 0	
		pedestal black level 0.1 to 2.8 V	control bit PEDST = 1	
21	FB_3; feedback input channel 3	open-circuit base	control bit FPOL = 0	DC coupling; Vs1 = 0 V; Vs2 = 1 V (control bit FPOL = 0) AC coupling; Vs1 = 1 V; Vs2 = 0 V (control bit FPOL = 1)
			control bit FPOL = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
22	REF_3; reference voltage channel 3	−300 to +300 µA		
23	GND_2; ground channel 2			
24	V_{P2}; supply voltage channel 2	I_{24} = 40 mA		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
25	V_{O2}; signal output channel 2	reference black level 0.1 to 2.8 V	control bit PEDST = 0	
		pedestal black level 0.1 to 2.8 V	control bit PEDST = 1	
26	FB_2; feedback input channel 2	open-circuit base	control bit FPOL = 0	DC coupling; Vs1 = 0 V; Vs2 = 1 V (control bit FPOL = 0) AC coupling; Vs1 = 1 V; Vs2 = 0 V (control bit FPOL = 1)
			control bit FPOL = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
27	REF_2; reference voltage channel 2	−300 to +300 µA		
28	GND_1; ground channel 1			
29	V_{P1}; supply voltage channel 1	I_{29} = 40 mA		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
30	V_{O1}; signal output channel 1	reference black level 0.1 to 2.8 V	control bit PEDST = 0	
		pedestal black level 0.1 to 2.8 V	control bit PEDST = 1	
31	FB_1; feedback input channel 1	open-circuit base	control bit FPOL = 0	DC coupling; Vs1 = 0 V; Vs2 = 1 V (control bit FPOL = 0) AC coupling; Vs1 = 1 V; Vs2 = 0 V (control bit FPOL = 1)
			control bit FPOL = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
32	REF_1; reference voltage channel 1	−300 to +300 µA		

13 TEST AND APPLICATION INFORMATION

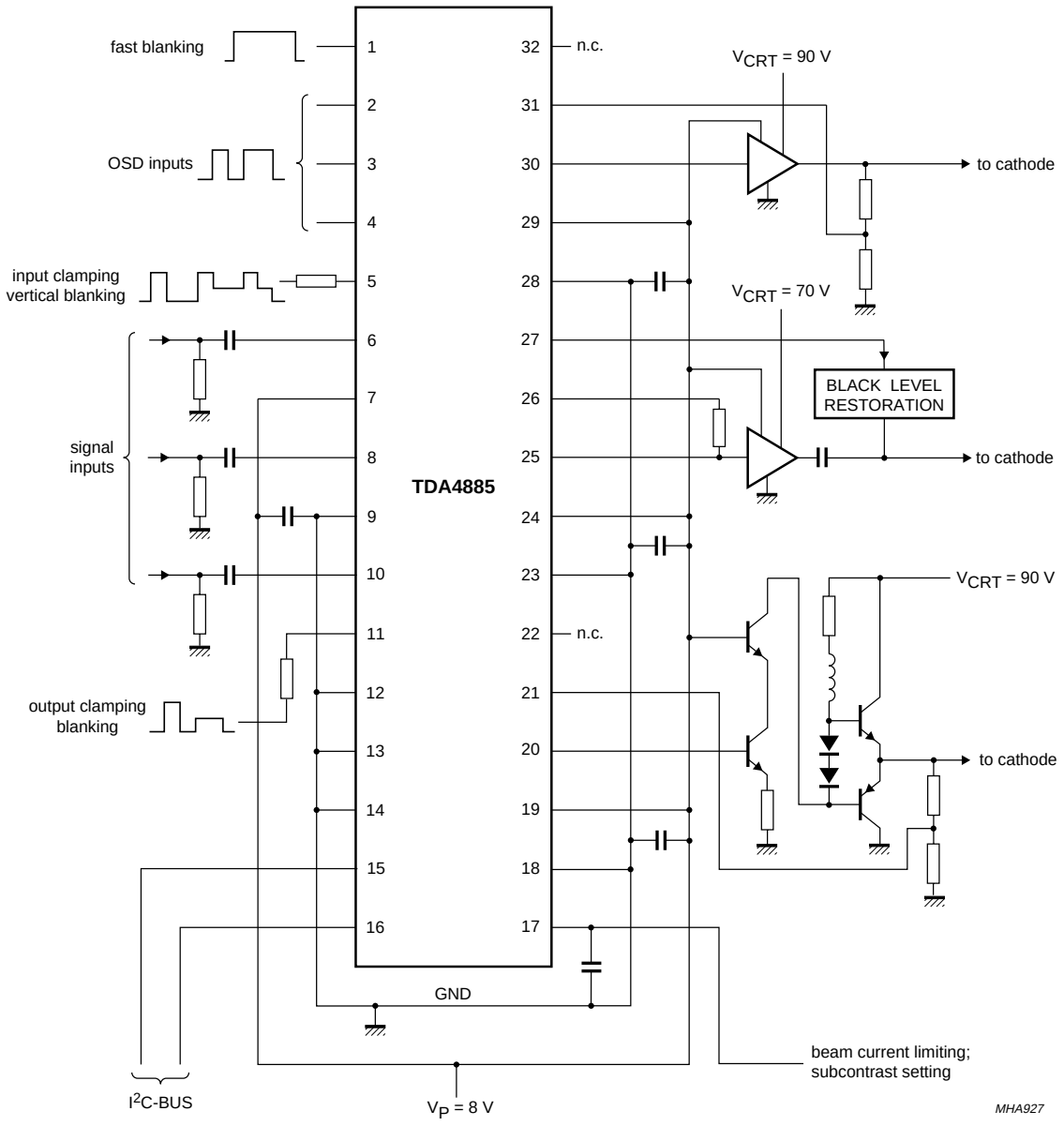


Fig.18 Basic application for different output stages with DC coupling (FPOL = 0) or AC coupling (FPOL = 1).

13.1 Test application

For high frequency measurements a special test application and printed-circuit board with only a few external components is built. Figure 19 shows the test application circuit and Figs 20 and 21 the layout of the double sided printed board. Most components are of SMD type. Short HF loops and minimum crosstalk between the channels and between signal inputs and outputs are achieved by properly shaped ground areas.

The HF input signal can be fed to the subclick connectors V_{I1}, V_{I2} and V_{I3} by a 50 Ω line. The line is then terminated by a 50 Ω resistor on the board. In channel 3 (pin 10) the HF input signal can be measured (probe socket).

For operation without input clamping the DC bias can be provided by VINDC if a short-circuit at J1, J2 and J3 is made.

OSD input signals (subclick: OSD_1, OSD_2, OSD_3, FBL) and blanking/clamping inputs (subclick: CLI, HFB) are terminated with 50 Ω on the board.

The gain modulation input GM (subclick) can be connected to the three inputs by the jumpers J8 and J4, J5 and J6. With jumper J7 pins 12, 13 and 14 can be connected to ground (no gain reduction).

There is a separate 4-pin connector for the I²C-bus controller, SDA and SCL have 10 kΩ pull up resistors to 5 V digital supply.

The beam current limiting pin is fed to the 10-pin main connector without any special application and should be connected to the 5 V supply if not used.

DC supply voltage V_P with a series resistor of 5.6 Ω can be measured directly at pin 7 via a resistor of 1 kΩ (V_P sense).

The supply voltage for the signal channels is fed to VPX separately and connected to pins 19, 24 and 29 with decoupling resistors of 5.6 Ω. The supply voltage V_{P1} (pin 29) can be measured via 1 kΩ at pin V_{P1} sense.

All supply voltages are filtered near to their pins with 150 pF and 100 nF SMD capacitors and low impedance 0.47 µF/63 V electrolytic capacitors.

The signal outputs are loaded with 10 kΩ and 3 pF to ground and are connected to a probe socket. With a probe capacitance of 2 pF the total capacitive load is 5 pF.

The feedback inputs are connected to the voltage outputs with a 0 Ω resistor (short circuit; RFB1) and via 10 kΩ (RFB2) connected to the pin VFBDC. The blanking level can be adjusted with a variation of RFB1, RFB2 and VFBDC but the resistive output load will be changed. The blanking level is:

$$U_{outbl} = \left(1 + \frac{RFB1}{RFB2}\right) \times 0.7\ V - \frac{RFB1}{RFB2} \times VFBDC$$

The reference outputs are connected to solder pins.

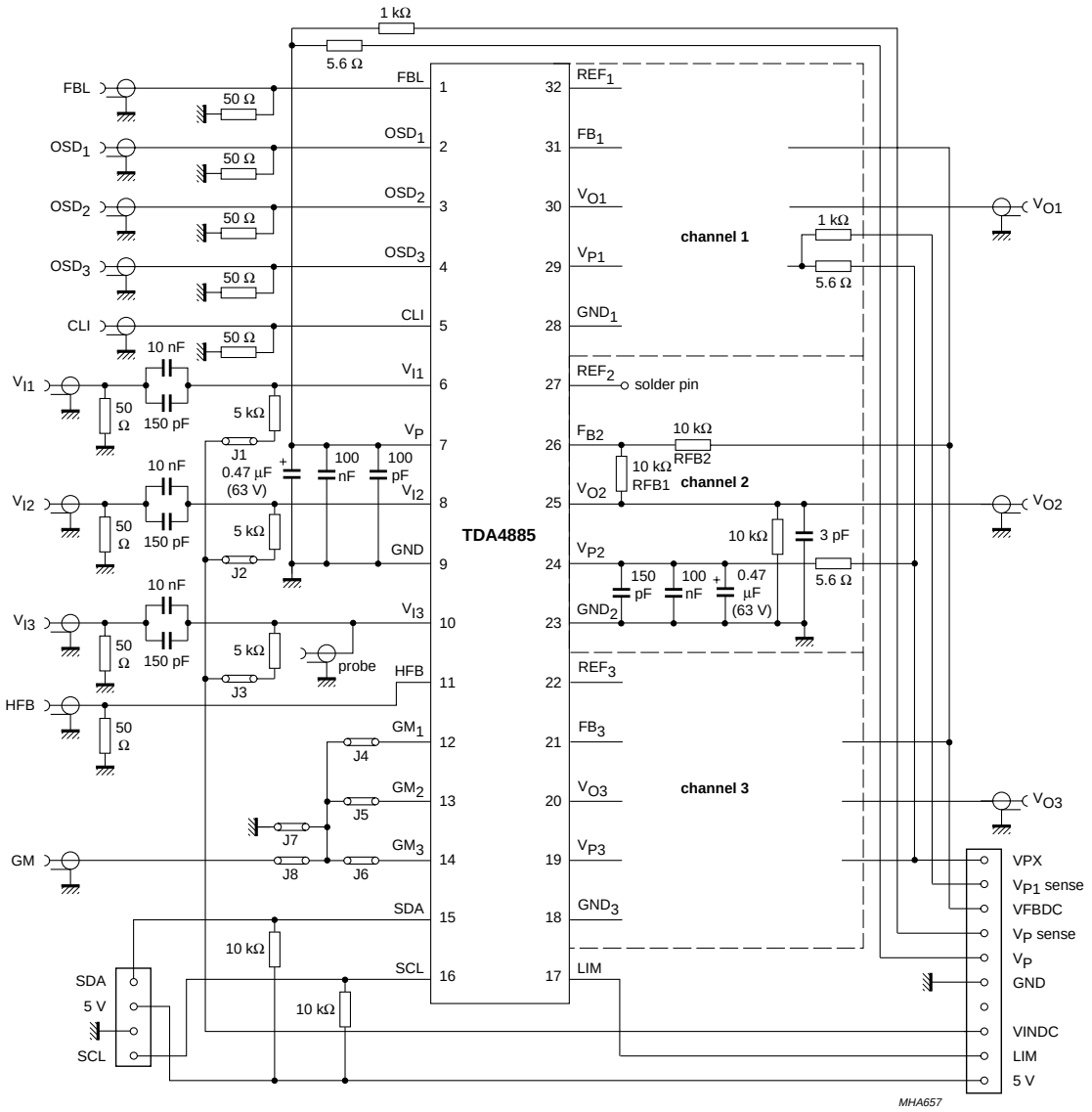
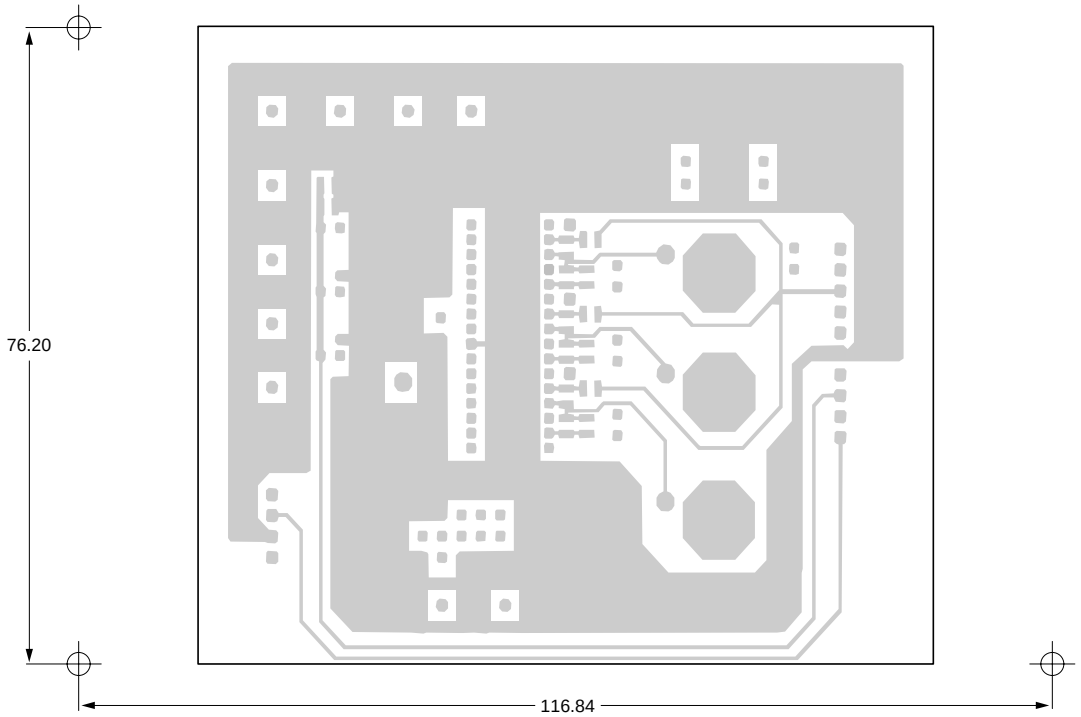


Fig.19 Test board.



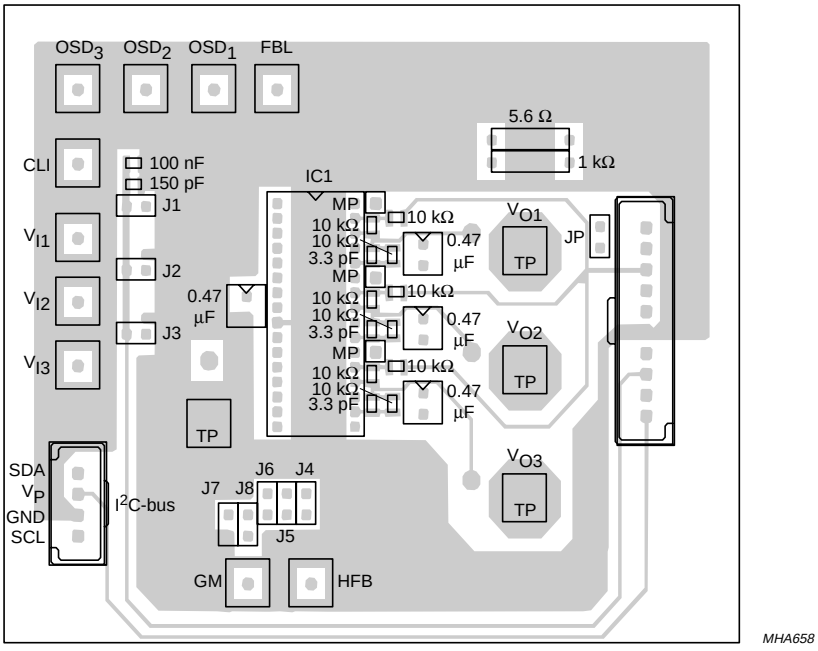


Fig.20 Component layout and printed-circuit board; side A (for side B see Fig.21).

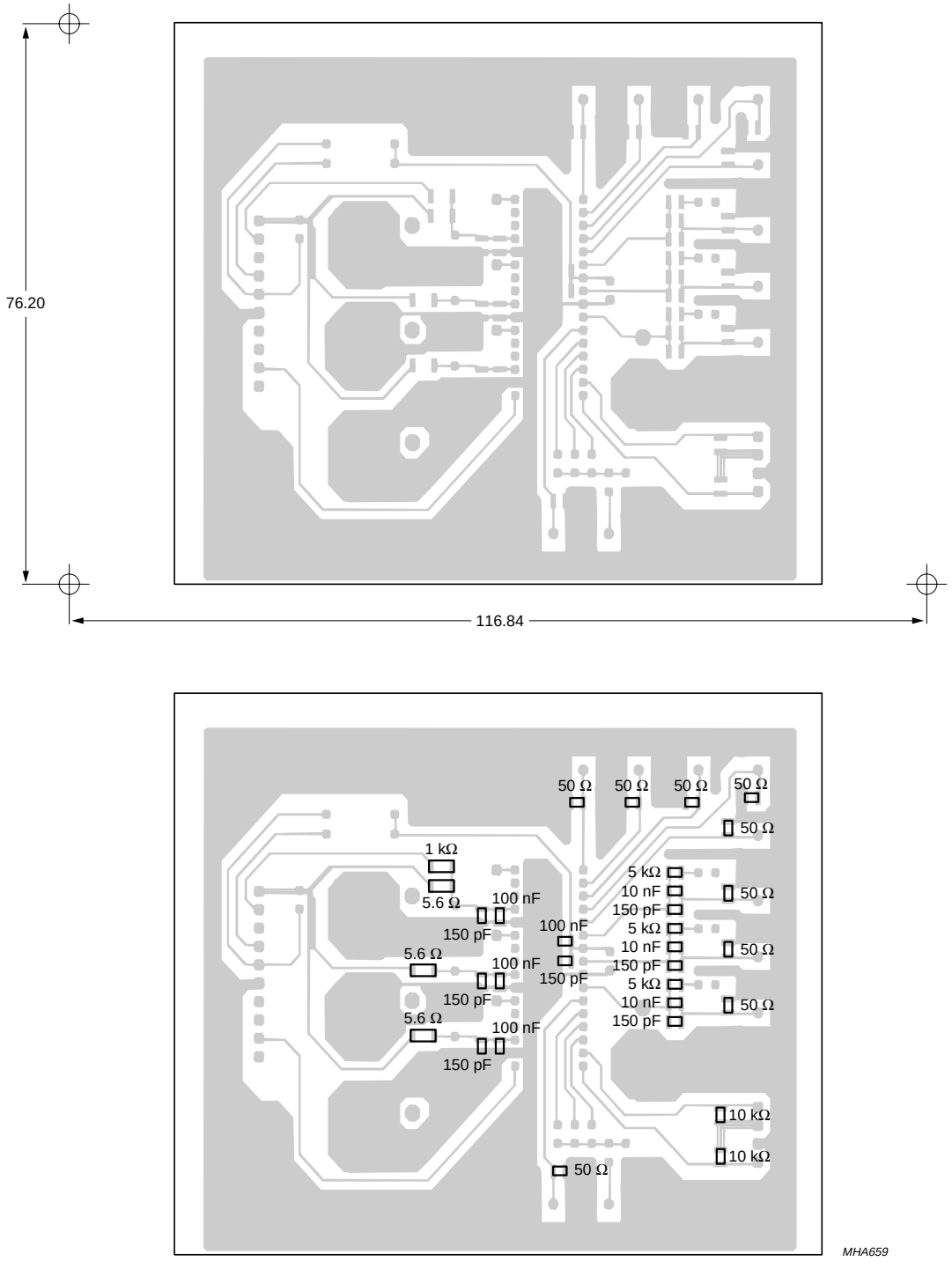


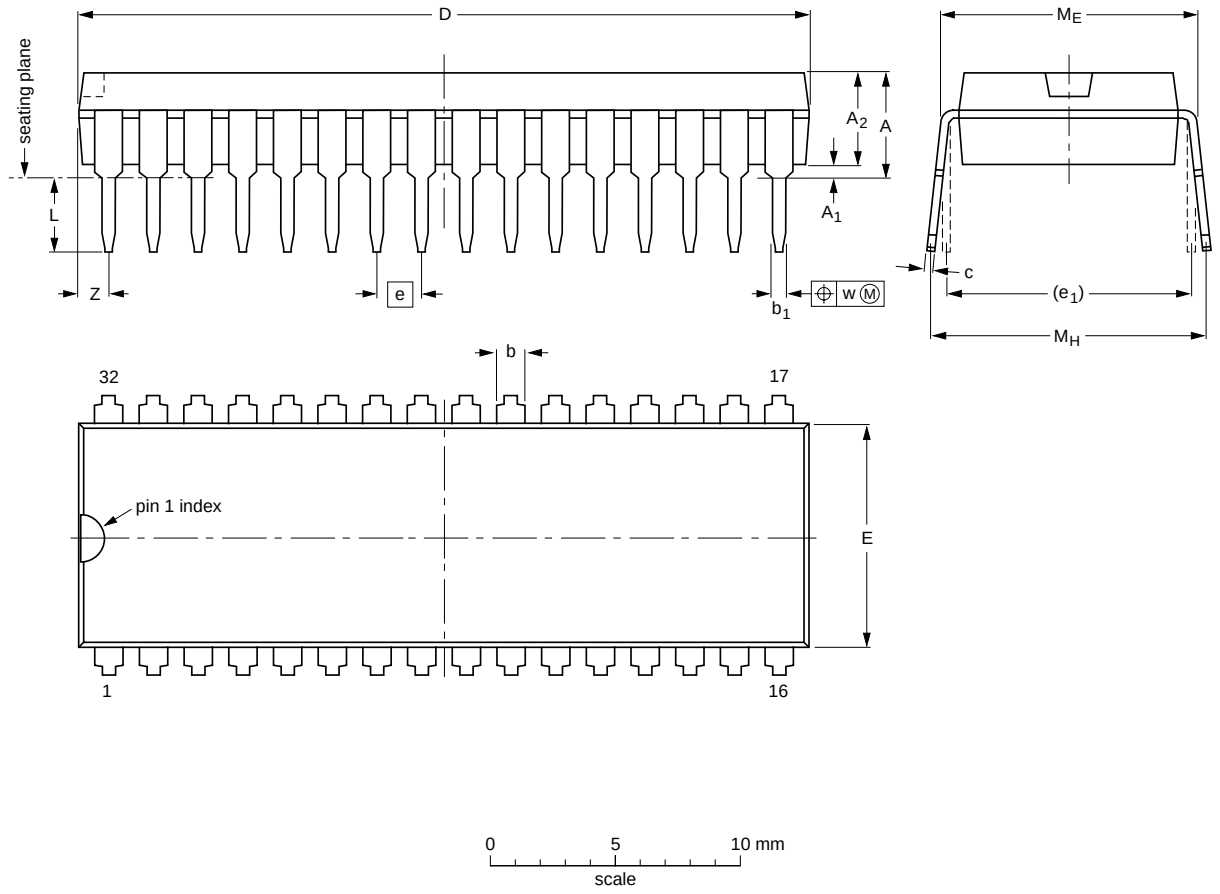
Fig.21 Component layout and printed-circuit board; side B (for side A see Fig.20).

13.2 Recommendations for building the application board

- General
  - Double-sided board
  - Short HF loops by large ground plane on the rear
  - SMD components with minimum parasitics.
- Voltage outputs
  - Capacitive loads as small as possible
  - Be aware of internal output resistance (80 Ω).
- Supply voltages
  - Capacitors as near as possible to the pins
  - Use electrolytic capacitors with small serial resistance and inductance.
- Smearing
  - Additional peaking circuit at emitter of driver transistor of cascode stage (time constant approximately 100 ns).

14 PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.3 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale

18 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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