NEC

MOS INTEGRATED CIRCUIT

μPD3768

7500 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD3768 is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD3768 has 3 rows of 7500 pixels, and it is a 2-output/color type CCD sensor with 2 rows/color of charge transfer register, which transfers the photo signal electrons of 7500 pixels separately in odd and even pixels. Therefore, it is suitable for 600 dpi/A3 high-speed color digital copiers, color scanners and so on.

FEATURES

- Valid photocell : 7500 pixels × 3
- Photocell pitch : 9.325 μm
- Line spacing : 37.3 μm (4 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 24 dot/mm A3 (297 × 420 mm) size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 44 MHz MAX. (22 MHz/1 output)
- Output type : 2 outputs in phase/color
- Power supply : +10 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD3768D	CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

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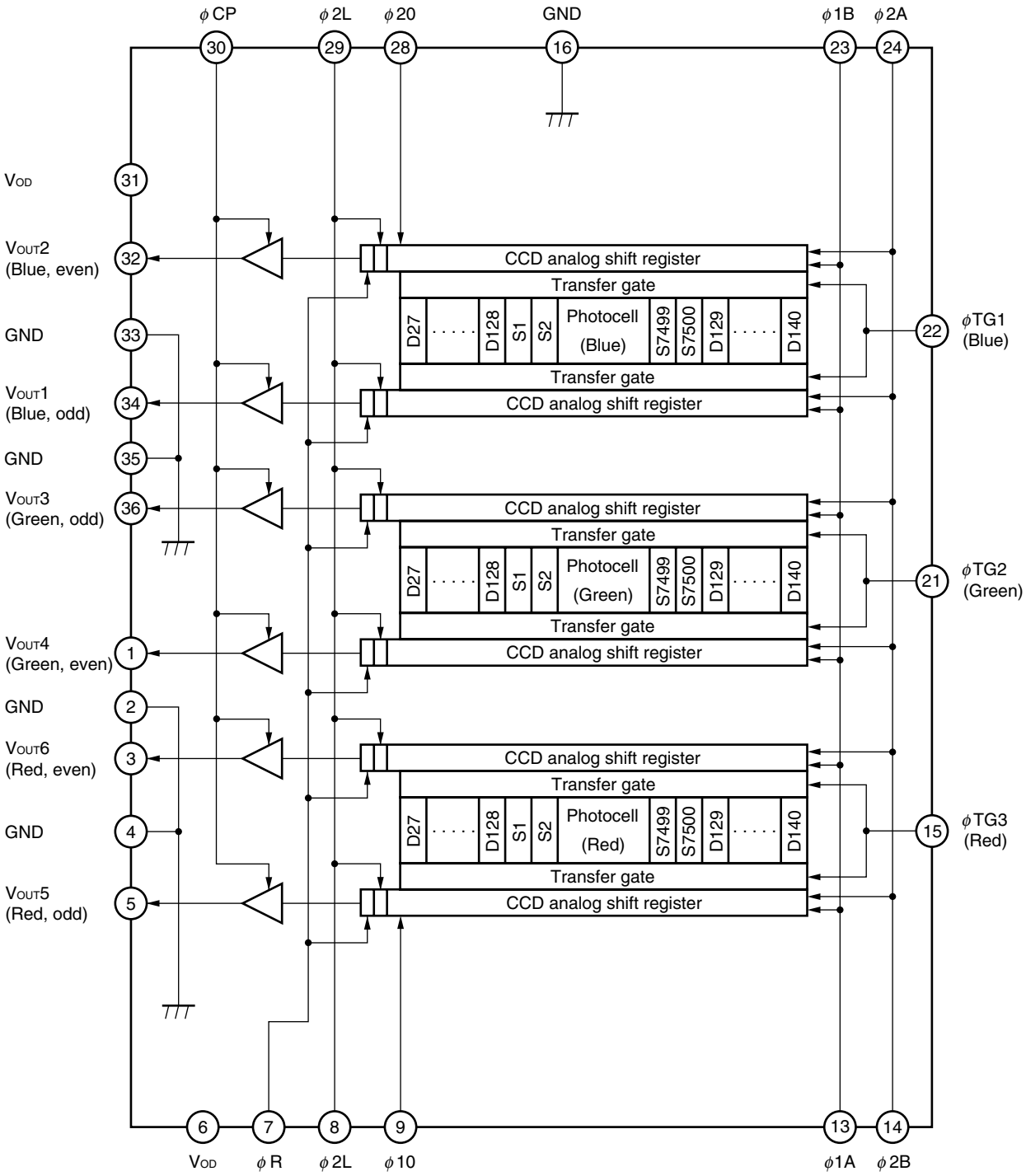
Date Published September 2002 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

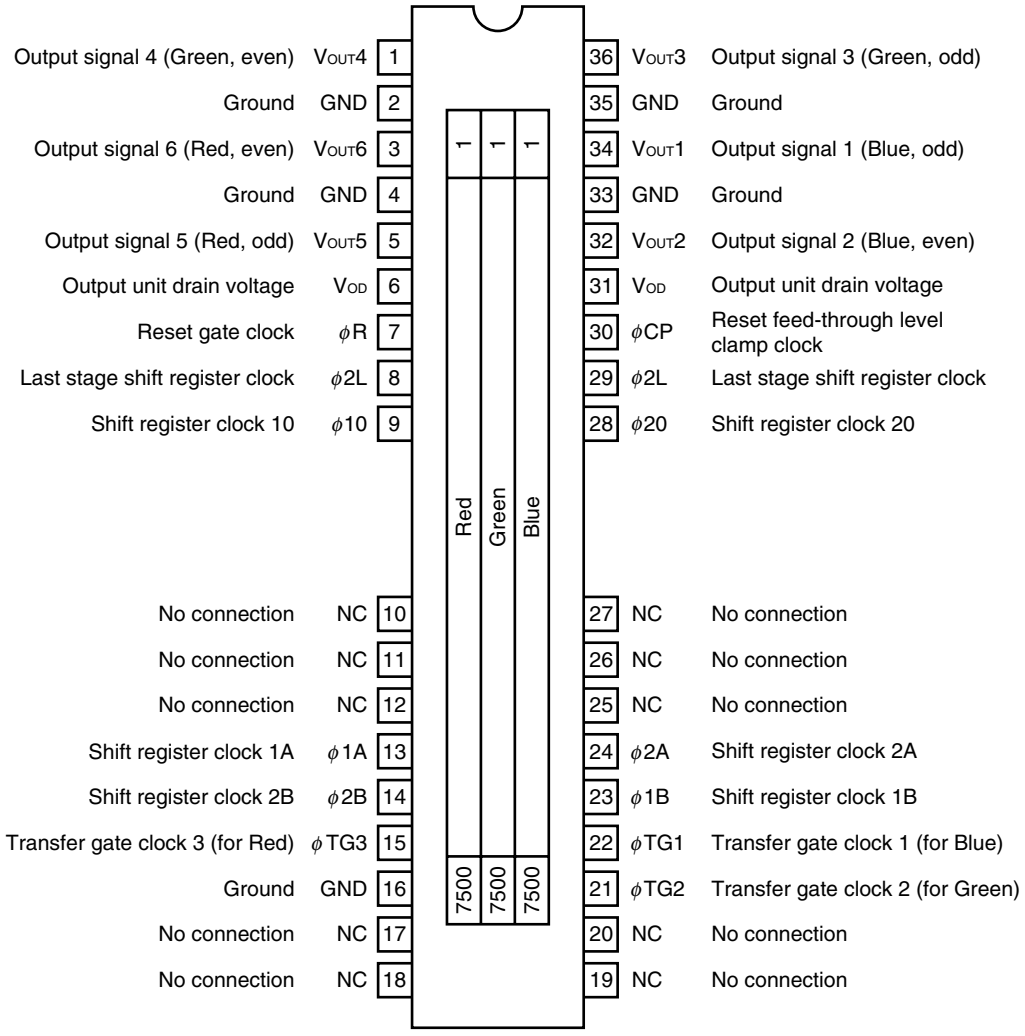
BLOCK DIAGRAM



★ PIN CONFIGURATION (Top View)

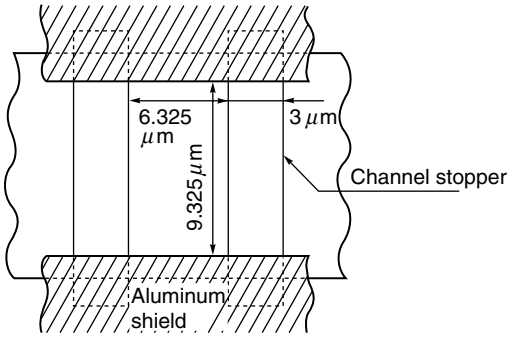
CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

• μPD3768D

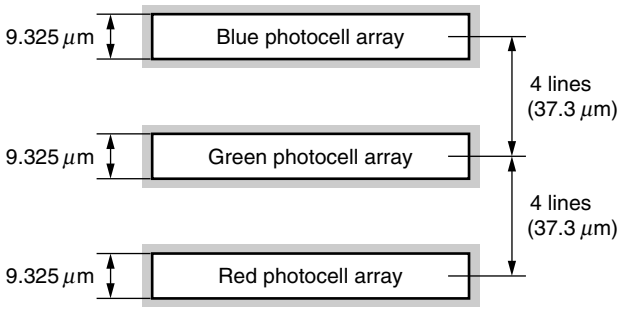


Caution Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +12	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	–0.3 to +8	V
Last gate shift register clock voltage	$V_{\phi 2L}$	–0.3 to +8	V
Reset gate clock voltage	$V_{\phi R}$	–0.3 to +8	V
Clamp clock voltage	$V_{\phi CP}$	–0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	–0.3 to +8	V
Operating ambient temperature Note	T_A	–25 to +60	°C
Storage temperature	T_{stg}	–40 to +100	°C

★ **Note** Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V_{OD}	9.5	10.0	10.5	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$	4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$	–0.3	0	+0.5	V
Last gate shift register clock high level	$V_{\phi 2LH}$	4.5	5.0	5.5	V
Last gate shift register clock low level	$V_{\phi 2LL}$	–0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi RH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RL}$	–0.3	0	+0.5	V
Clamp clock high level	$V_{\phi CPH}$	4.5	5.0	5.5	V
Clamp clock low level	$V_{\phi CPL}$	–0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.5	$V_{\phi 1H}$ Note	$V_{\phi 1H}$ Note	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	–0.3	0	+0.5	V
Data rate	$2f_{\phi R}$	1	2	44	MHz

Note When Transfer gate clock high level ($V_{\phi TG1H}$ to $V_{\phi TG3H}$) is higher than Shift register clock high level ($V_{\phi 1H}$), Image lag can increase.

ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{OD} = 10 V, $f_{\phi R}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p}, light source (except Response1) : 2950 K halogen lamp + CM-500S (infrared cut filter, t = 1 mm)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage		V_{sat}		1.5	2.0	–	V
Saturation exposure	Red	SER	2950 K halogen lamp + CM-500S	–	0.14	–	lx•s
	Green	SEG		–	0.13	–	lx•s
	Blue	SEB		–	0.26	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6.0	18.0	%
Photo response non-uniformity at low illumination		PRNU2	V_{OUT} = 0.1 V	–	6.0	18.0	%
Average dark signal		ADS	Light shielding, data rate = 2 MHz, storage time = 10 ms	–	1.0	5.0	mV
Dark signal non-uniformity		DSNU	Light shielding, data rate = 2 MHz, storage time = 10 ms	–	3.0	12.0	mV
Power consumption		P_W		–	700	900	mW
Output impedance		Z_O		–	0.2	0.4	kΩ
Response1	Red	R_R	3200 K halogen lamp + C-500S + HA-50	15.4	22.0	28.6	V/lx•s
	Green	R_G		12.6	18.0	23.4	V/lx•s
	Blue	R_B		5.6	8.0	10.4	V/lx•s
Response2	Red	R_R	2950 K halogen lamp + CM-500S	9.8	14.0	18.2	V/lx•s
	Green	R_G		10.7	15.3	19.9	V/lx•s
	Blue	R_B		5.3	7.6	9.9	V/lx•s
Image lag		IL	V_{OUT} = 500 mV	–	40	80	mV
Image lag color difference		IL-DIF	V_{OUT} = 500 mV	–	5	20	mV
Image lag O/E		IL-O/E	V_{OUT} = 500 mV	–	10	30	mV
Offset level Note 1		V_{OS}		3.8	4.5	5.2	V
Output fall delay time Note 2		t_d		–	14	–	ns
Register imbalance		RI	V_{OUT} = 1.0 V	–	0	5	%
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, $f_{\phi R}$ = 22 MHz	94	98	–	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	445	–	nm
Dynamic range		DR1	V_{sat}/DSNU	–	666	–	times
		DR2	V_{sat}/σdark	–	870	–	times
Reset feed-through noise		RFTN	Light shielding	−1000	−200	+500	mV
Light shielding random noise		σdark	Bit clamp, t17 = 10 ns	–	2.3	–	mV

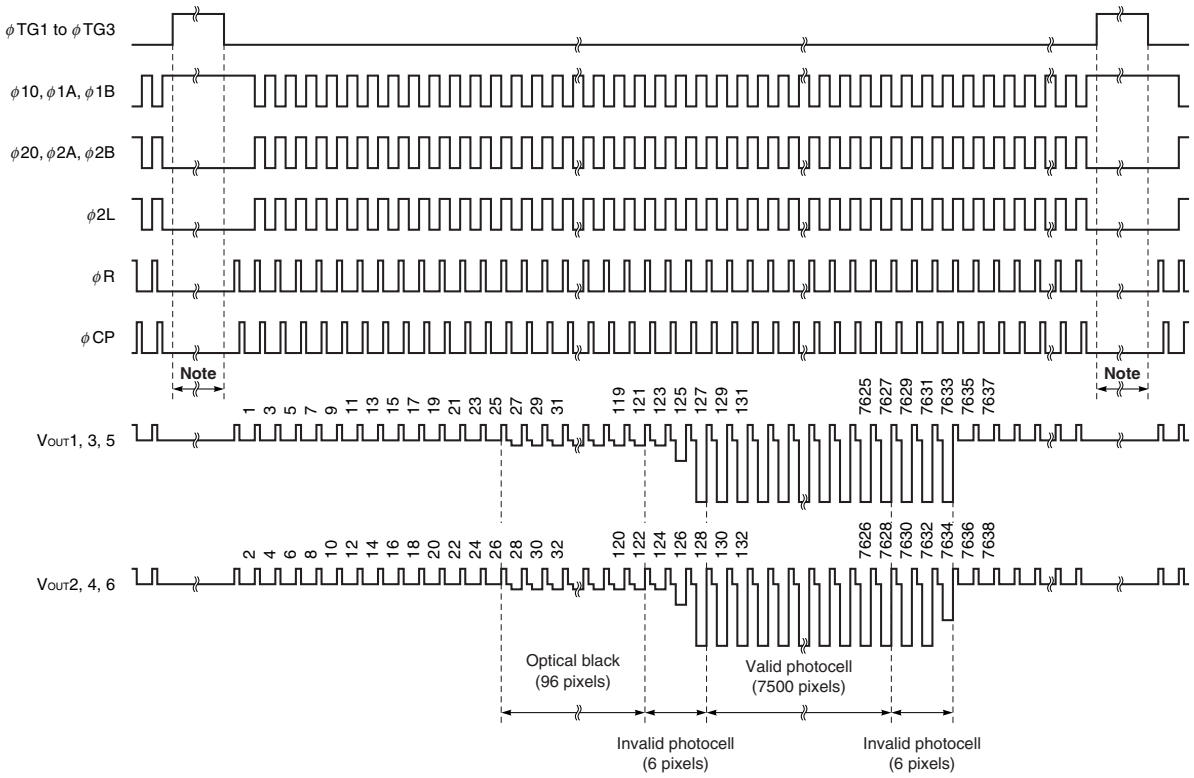
Notes 1. Refer to **TIMING CHART 2** and **TIMING CHART 4**.

2. t_d is defined as periods from 10% of ϕ2L to 10% of V_{OUT}1 to V_{OUT}6 (refer to **APPLICATION CURCUIT EXAMPLE**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 10 V)

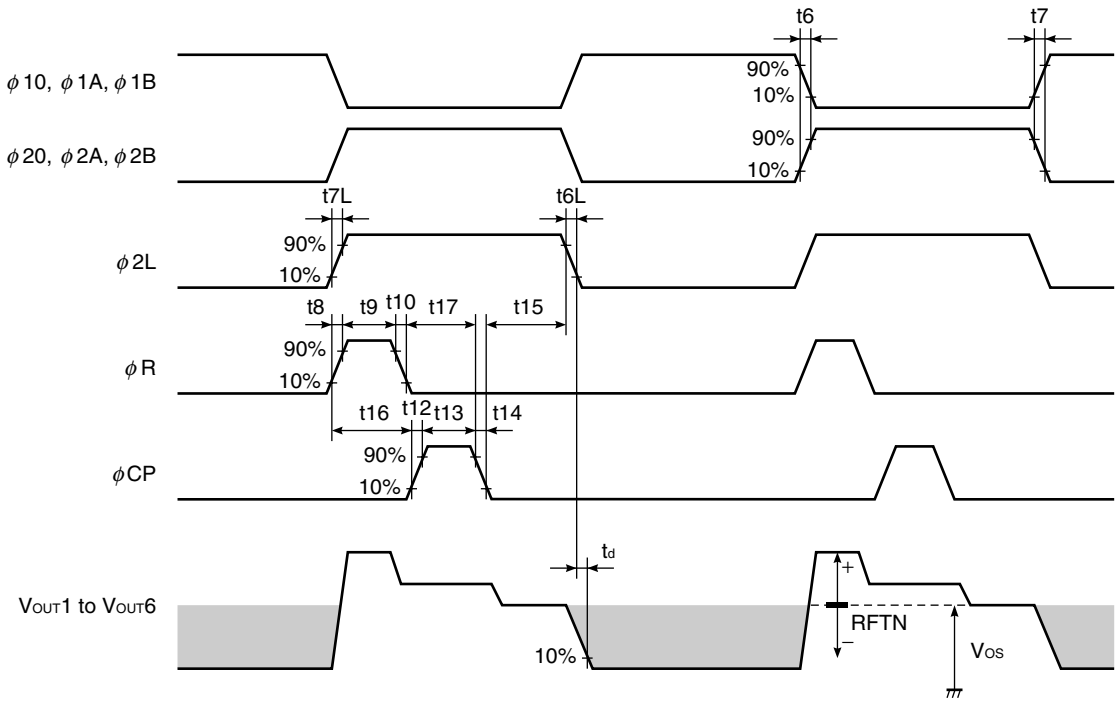
Parameter	Symbol	Pin	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance	$C_{\phi 1}$	ϕ10	9	–	330	450	pF
		ϕ1A	13	–	330	450	pF
		ϕ1B	23	–	330	450	pF
	$C_{\phi 2}$	ϕ2B	14	–	330	450	pF
		ϕ2A	24	–	330	450	pF
		ϕ20	28	–	330	450	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ2L	8	–	10	20	pF
			29	–	10	20	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR	7	–	10	20	pF
Clamp clock pin capacitance	$C_{\phi CP}$	ϕCP	30	–	10	20	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG1	22	–	100	150	pF
		ϕTG2	21	–	100	150	pF
		ϕTG3	15	–	100	150	pF

★ **TIMING CHART 1 (Bit clamp mode, for each color)**



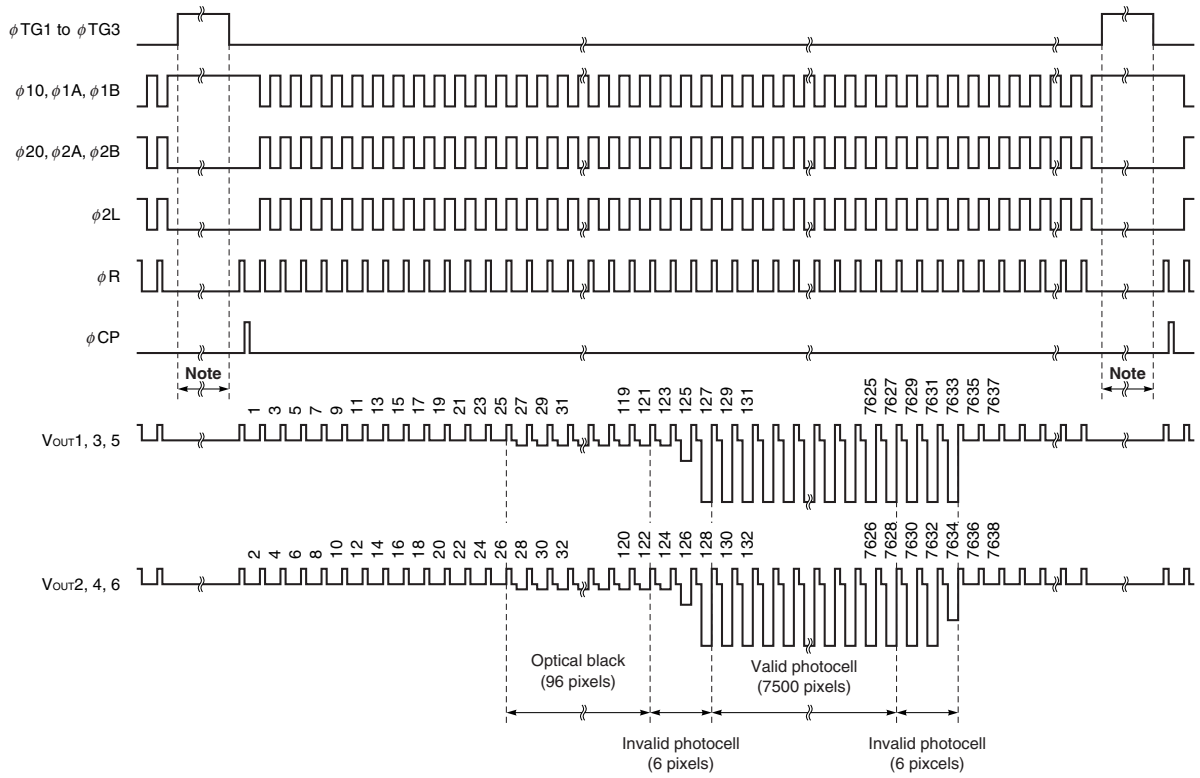
Note Set the φR and φCP pulse to low level during this period.

TIMING CHART 2 (Bit clamp mode, for each color)



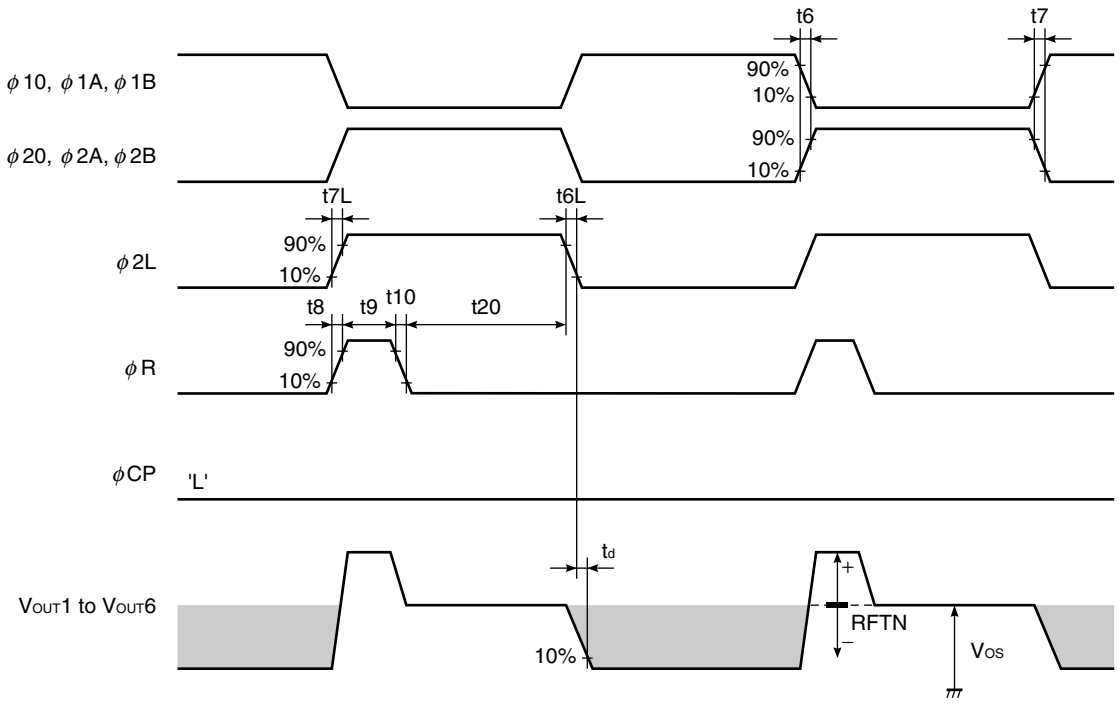
Symbol	Min.	Typ.	Max.	Unit
t6, t7	0	50	–	ns
t6L, t7L	0	5	–	ns
t8, t10	0	5	–	ns
t9	10	125	–	ns
t12, t14	0	5	–	ns
t13	10	125	–	ns
t15	0	250	–	ns
t16	8	125	–	ns
t17	8	125	–	ns

★ **TIMING CHART 3 (Line clamp mode, for each color)**



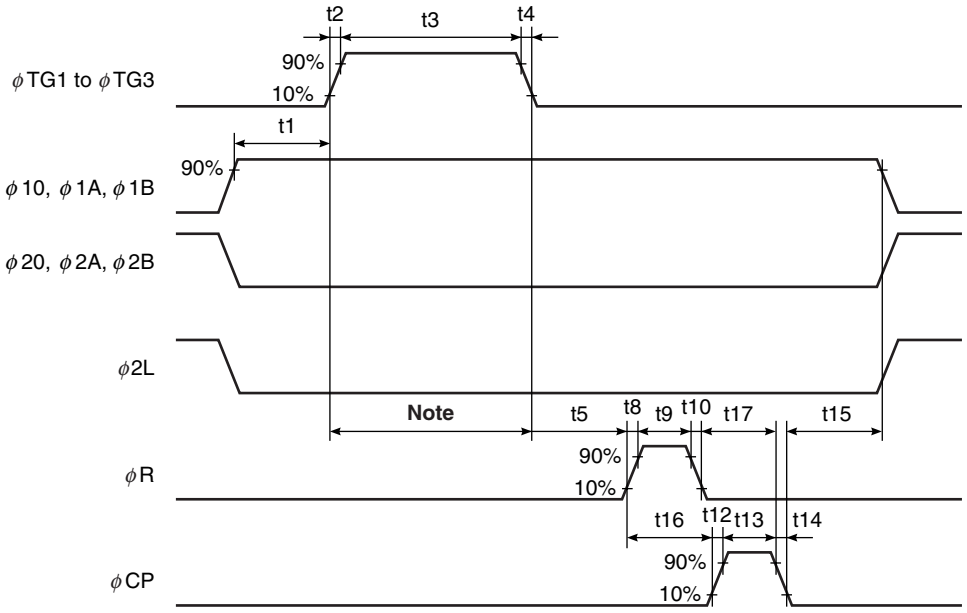
Note Set the φR and φCP pulse to low level during this period.

★ **TIMING CHART 4 (Line clamp mode, for each color)**



Symbol	Min.	Typ.	Max.	Unit
t6, t7	0	50	–	ns
t6L, t7L	0	5	–	ns
t8, t10	0	5	–	ns
t9	10	125	–	ns
t20	5	250	–	ns

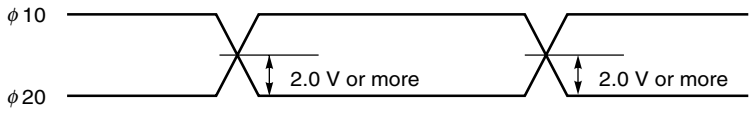
TIMING CHART 5 (Bit clamp mode, line clamp mode, for each color)



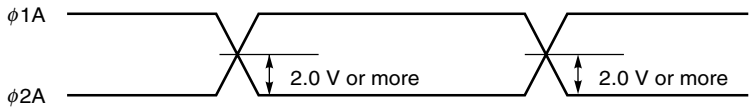
Symbol	Min.	Typ.	Max.	Unit
t1, t5	200	300	–	ns
t2, t4	0	50	–	ns
t3	3000	5000	–	ns
t8, t10	0	5	–	ns
t9	10	125	–	ns
t12, t14	0	5	–	ns
t13	10	125	–	ns
t15	0	250	–	ns
t16	8	125	–	ns
t17	8	125	–	ns

Note Set the φR and φCP pulse to low level during this period.

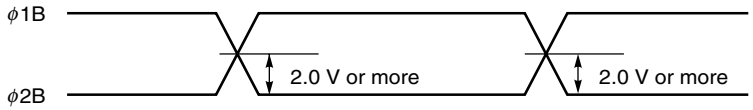
φ10, φ20 cross points



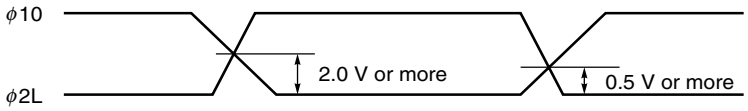
φ1A, φ2A cross points



φ1B, φ2B cross points



φ10, φ2L cross points



Remark Adjust cross points (φ10, φ20), (φ1A, φ2A), (φ1B, φ2B) and (φ10, φ2L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

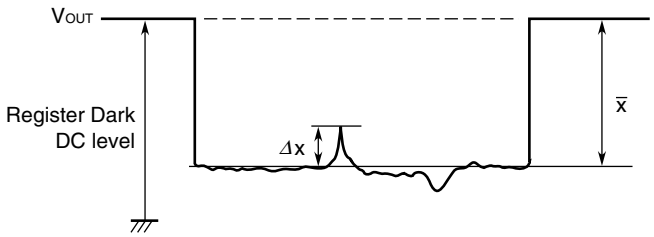
3. Photo response non-uniformity : **PRNU**
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula, and it is defined by each six of them.

$$PRNU\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{7500} x_j}{7500}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each six of them.

$$ADS\ (mV) = \frac{\sum_{j=1}^{7500} d_j}{7500}$$

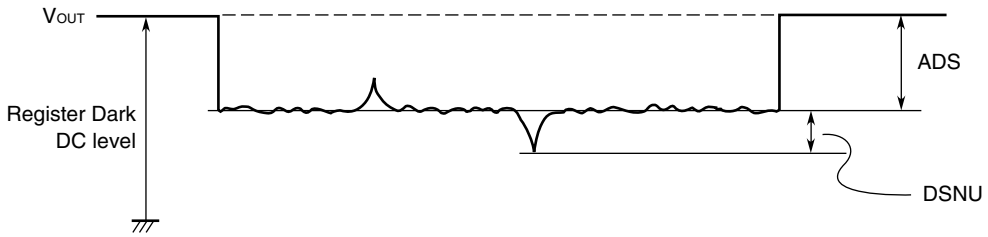
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each six of them.

DSNU (mV) : maximum of $|d_j - ADS|_{j = 1 \text{ to } 7500}$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

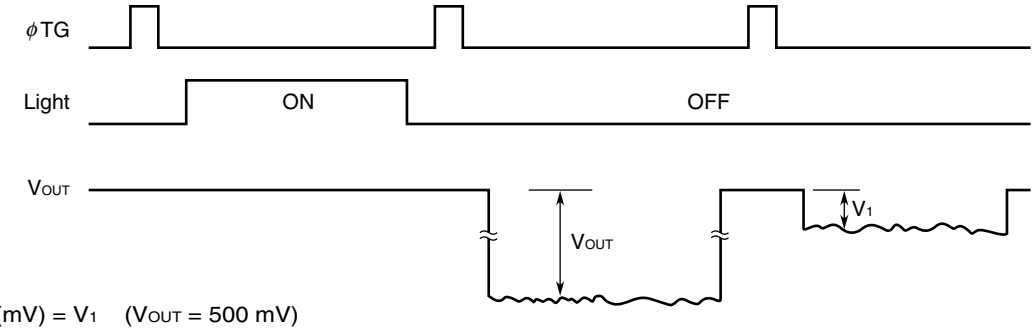
7. Response : **R**

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



IL (mV) = V_1 (V_{OUT} = 500 mV)

9. Image lag color difference : **IL-DIF**

It is defined as a difference between colors of the average of image lag.

It is expressed with the next expression to be concrete.

| (average of image lag of blue output) – (average of image lag of green output) |

| (average of image lag of green output) – (average of image lag of red output) |

| (average of image lag of red output) – (average of image lag of blue output) |

10. Image lag O/E : **IL-O/E**

It is defined as a difference of the average of image lag of odd and even pixels for each color.

11. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

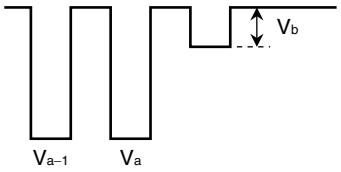
$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels
V_j : Output voltage of each pixel

★ 12. Total transfer efficiency : **TTE**

The total transfer rate of CCD analog shift register. This is calculated by the following formula, it is difined by each output.

TTE (%) = (1 – V_b / average output of all the valid pixels) × 100



V_{a-1} : The last pixel output – 1 (Odd pixel: 7631th pixel)

V_a : The last pixel output (Odd pixel: 7633th pixel)

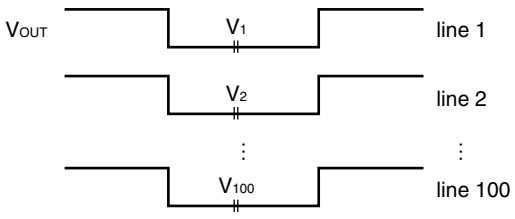
V_b : The spilt pixel output (Odd pixel: 7635th pixel)

13. Light shielding random noise : **σdark**

Light shielding random noise σdark is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

$$\sigma\,\text{dark (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}}, \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

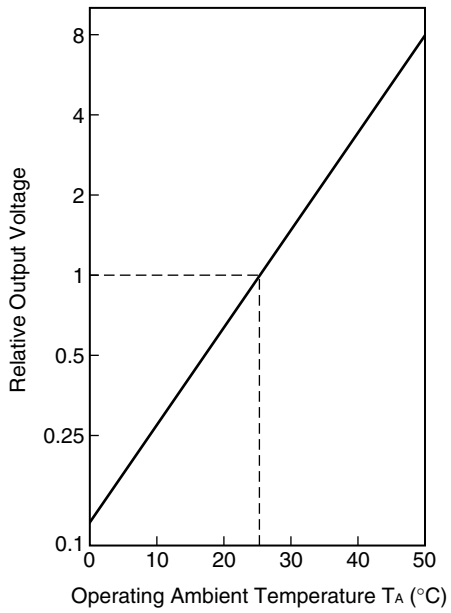
V_i : A valid pixel output signal among all of the valid pixels for each color



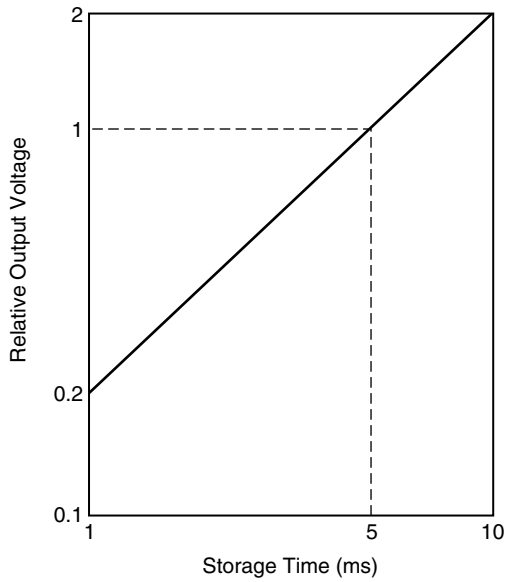
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES (Reference Value)

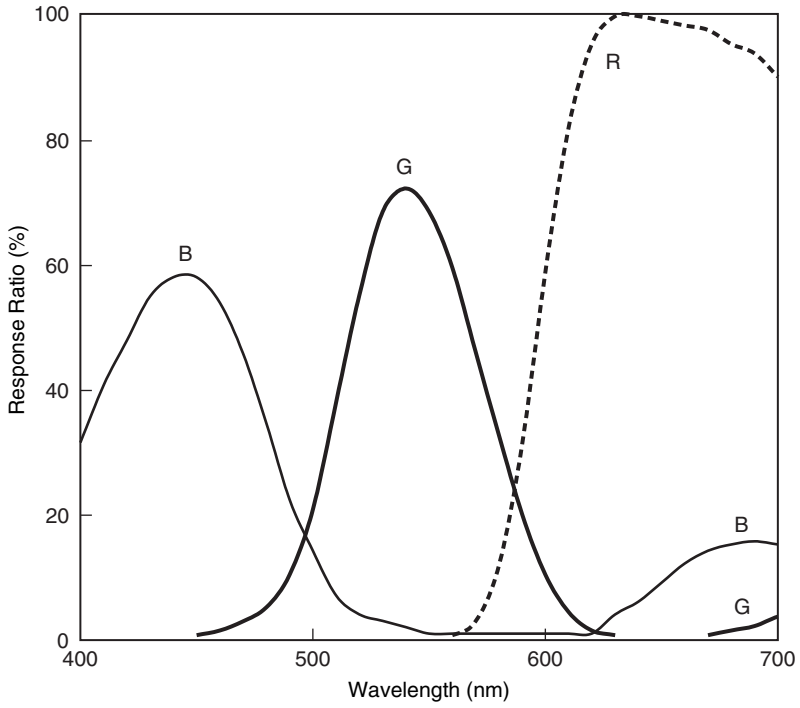
DARK OUTPUT TEMPERATURE CHARACTERISTIC



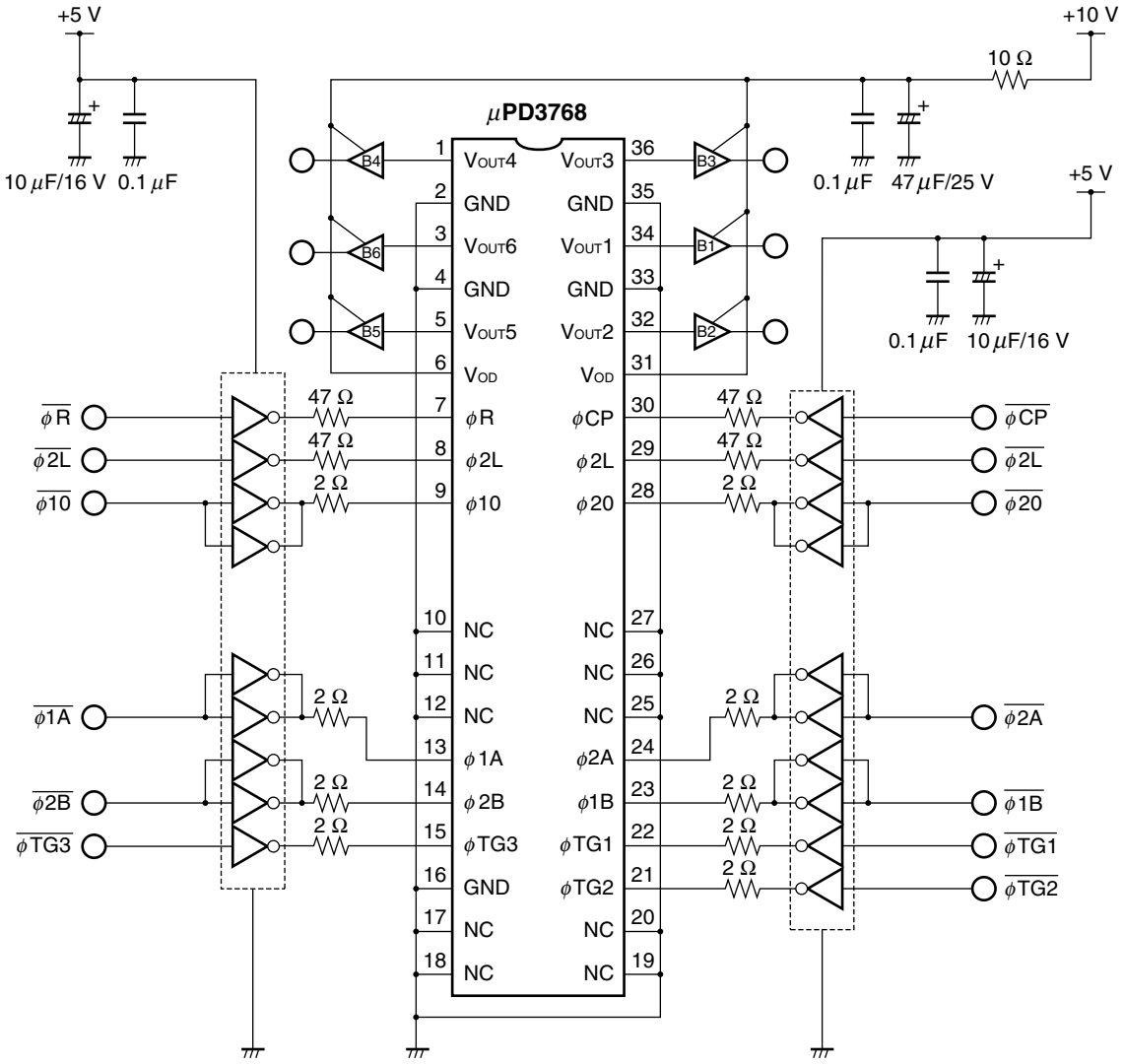
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (T_A = +25°C)



APPLICATION CIRCUIT EXAMPLE

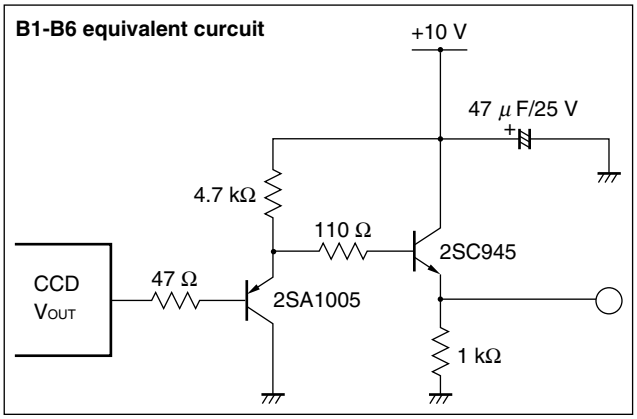


Caution Connect the No connection pins (NC) to GND.

Remarks 1. Connect two inverters (74AC04) to each ϕ10, ϕ1A, ϕ1B, ϕ20, ϕ2A, ϕ2B pin.

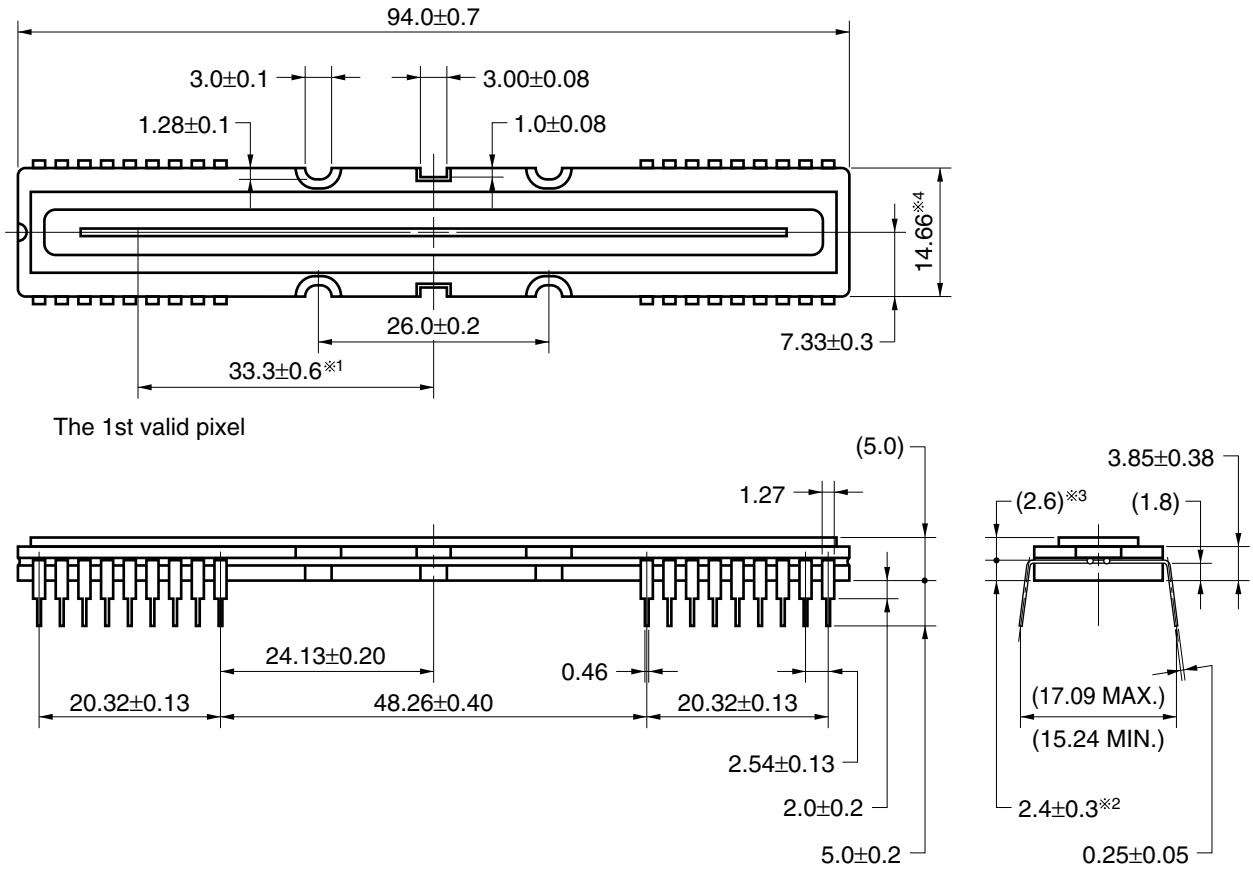
2. Inverters shown in the above application circuit example are the 74AC04.

3. B1 to B6 in the application circuit example are shown in the figure below.



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 36-PIN CERAMIC DIP (15.24 mm (600))



Name	Dimension	Refractive index
Glass cap	91.0×9.0×1.1	1.5

※1 1st valid pixel ⟷ Center of package

※2 The bottom of package ⟷ The surface of the chip

※3 The surface of the chip ⟷ The surface of the glass cap

※4 The tolerance of packge dimension
±0.25 : less than 10 mm from W/F edge
±0.50 : equal or more than 10 mm from W/F edge

36D-1CCD-PKG3-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD3768D : CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

★ **Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.**

2. Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.

★ # NOTES ON HANDLING THE PACKAGES

① MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

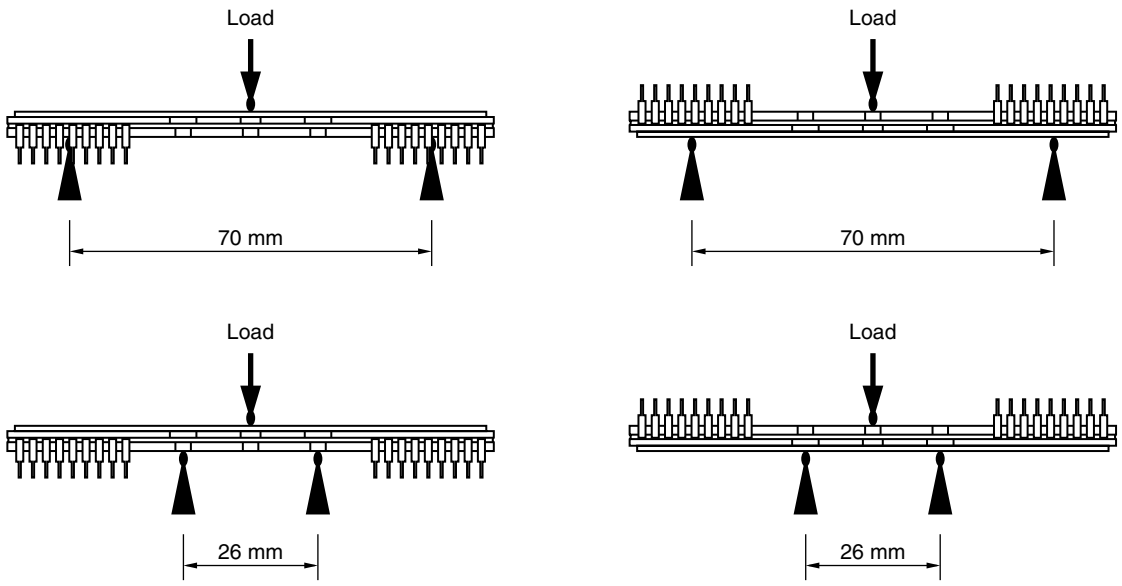
Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

For this product, the reference value for the three-point bending strength [Note] is 180 [N] (at distance between supports: 70 mm), is 500 [N] (at distance between supports: 26 mm). Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body (ceramic).

Note Three-point bending strength test

Distance between supports: 70 mm or 26 mm, Support R: R 2 mm, Loading rate: 0.5 mm/min.



② GLASS CAP

Don't either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

★ NOTES ON HANDLING THE PACKAGES

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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