Integrated Device Technology, Inc.

# FAST CMOS OCTAL REGISTERED TRANSCEIVERS

**IDT29FCT52A/B/C**
**IDT29FCT53A/B/C**

## FEATURES:

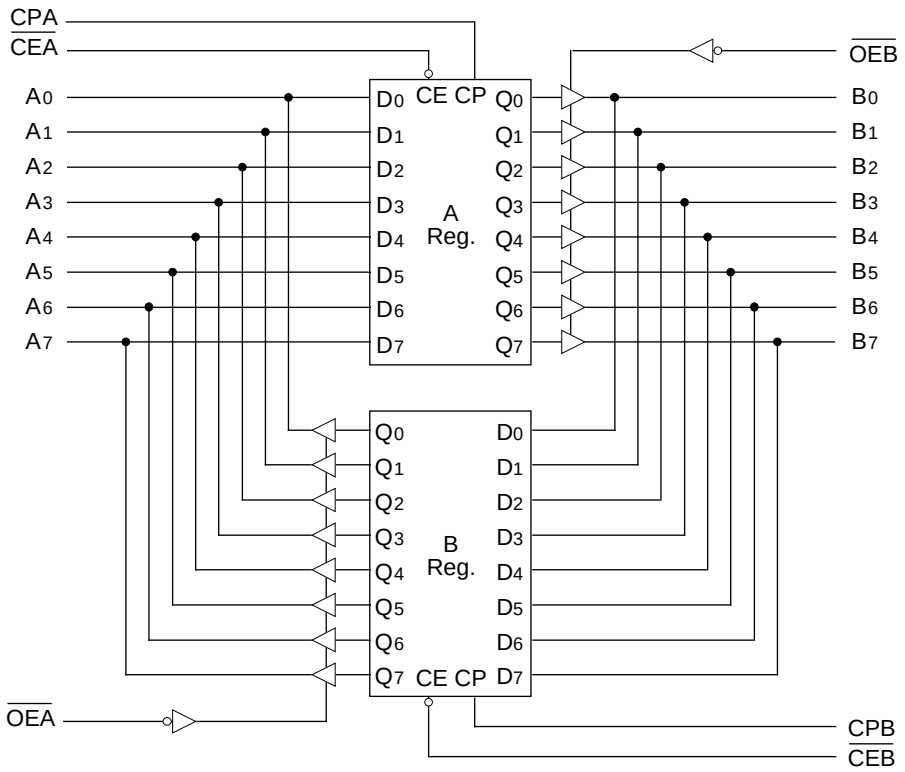
- Equivalent to AMD's Am2952/53 and National's 29F52/53 in pinout/function
- IDT29FCT52A/53A equivalent to FAST™ speed
- **IDT29FCT52B/53B 25% faster than FAST**
- **IDT29FCT52C/53C 37% faster than FAST**
- $I_{OL}$ = 64mA (commercial) and 48mA (military)
- $I_{IH}$ and $I_{IL}$ only 5µA max.
- CMOS power levels (2.5mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin DIP, SOIC, 28-pin LCC with JEDEC standard pinout
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT29FCT52A/B/C and IDT29FCT53A/B/C are 8-bit registered transceivers manufactured using an advanced dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52A/B/C is a non-inverting option of the IDT29FCT53A/B/C.

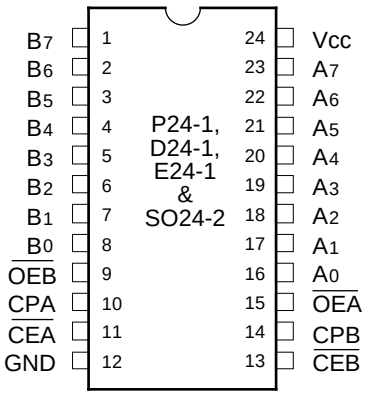
## FUNCTIONAL BLOCK DIAGRAM(1)



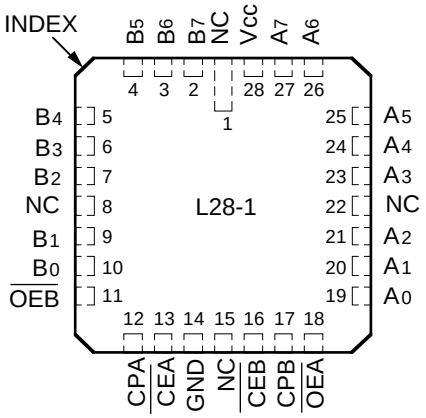

2533 drw 01

**NOTE:**
1. IDT29FCT52 function is shown.

## PIN CONFIGURATIONS




**DIP/CERPACK/SOIC**
**TOP VIEW**




**LCC**
**TOP VIEW**

2533 drw 02

## PIN DESCRIPTION

| Name | I/O | Description |
|---|---|---|
| $A_{0-7}$ | I/O | Eight bidirectional lines carrying the A Register inputs or B Register outputs. |
| $B_{0-7}$ | I/O | Eight bidirectional lines carrying the B Register inputs or A Register outputs. |
| CPA | I | Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. |
| $\overline{CEA}$ | I | Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions. |
| $\overline{OEB}$ | I | Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the $B_{0-7}$ lines. When $\overline{OEB}$ is HIGH, the $B_{0-7}$ outputs are in the high-impedance state. |
| CPB | I | Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. |
| $\overline{CEB}$ | I | Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions. |
| $\overline{OEA}$ | I | Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the $A_{0-7}$ lines. When $\overline{OEA}$ is HIGH, the $A_{0-7}$ outputs are in the high-impedance state. |

2533 tbl 01

## REGISTER FUNCTION TABLE[1]
**(Applies to A or B Register)**

| Inputs | | | Internal | |
|---|---|---|---|---|
| D | CP | $\overline{CE}$ | Q | Function |
| X | X | H | NC | Hold Data |
| L | ↑ | L | L | Load Data |
| H | ↑ | L | H | |

2533 tbl 02

## OUTPUT CONTROL[1]

| | Internal | Y-Outputs | | |
|---|---|---|---|---|
| $\overline{OE}$ | Q | 52 | 53 | Function |
| H | X | Z | Z | Disable Outputs |
| L | L | L | H | Enable Outputs |
| L | H | H | L | |

2533 tbl 03

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ | –0.5 to $V_{CC}$ | V |
| $T_A$ | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 0.5 | 0.5 | W |
| $I_{OUT}$ | DC Output Current | 120 | 120 | mA |

**NOTES:** 2533 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed +0.5V unless otherwise noted.
2. Inputs and $V_{CC}$ terminals only.
3. Outputs and I/O terminals only.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | 10 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 0V | 8 | 12 | pF |

**NOTE:** 2533 tbl 05

1. This parameter is guaranteed by characterization data and not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC}$ = 0.2V; $V_{HC}$ = $V_{CC}$ – 0.2V
Commercial: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions(1) | | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current (Except I/O Pins) | $V_{CC}$ = Max. | $V_I$ =$V_{CC}$ | — | — | 5 | µA |
| | | | $V_I$ = 2.7V | — | — | 5(4) | |
| $I_{IL}$ | Input LOW Current (Except I/O Pins) | | $V_I$ = 0.5V | — | — | –5(4) | |
| | | | $V_I$ = GND | — | — | –5 | |
| $I_{IH}$ | Input HIGH Current (I/O Pins Only) | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | 15 | µA |
| | | | $V_I$ = 2.7V | — | — | 15(4) | |
| $I_{IL}$ | Input LOW Current (I/O Pins Only) | | $V_I$ = 0.5V | — | — | –15(4) | |
| | | | $V_I$ = GND | — | — | –15 | |
| $V_{IK}$ | Clamp Diode Voltage | Vcc = Min., $I_N$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | Vcc = Max.(3), $V_O$ = GND | | –60 | –120 | — | mA |
| $V_{OH}$ | Output HIGH Voltage | Vcc = 3V, $V_{IN}$ = $V_{LC}$ or $V_{HC}$, $I_{OH}$ = –32µA | | $V_{HC}$ | $V_{CC}$ | — | V |
| | | Vcc = Min. | $I_{OH}$ = –300µA | $V_{HC}$ | $V_{CC}$ | — | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –15mA MIL. | 2.4 | 4.0 | — | |
| | | | $I_{OH}$ = –24mA COM'L. | 2.4 | 4.0 | — | |
| $V_{OL}$ | Output LOW Voltage | Vcc = 3V, $V_{IN}$ = $V_{LC}$ or $V_{HC}$, $I_{OL}$ = 300µA | | — | GND | $V_{LC}$ | V |
| | | Vcc = Min. | $I_{OL}$ = 300µA | — | GND | $V_{LC}$(4) | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 48mA MIL.(5) | — | 0.3 | 0.55 | |
| | | | $I_{OL}$ = 64mA COM'L.(5) | — | 0.3 | 0.55 | |

**NOTES:** 2533 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum $I_{OL}$ values per output, for 8 outputs turned on simultaneously. Total maximum $I_{OL}$ (all outputs) is 512mA for commercial and 384mA for military. Derate $I_{OL}$ for number of outputs exceeding 8 turned on simultaneously.

## POWER SUPPLY CHARACTERISTICS

$V_{LC}$ = 0.2V; $V_{HC}$ = $V_{CC}$ – 0.2V

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max.<br>$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ | | — | 0.5 | 1.5 | µA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current TTL Inputs HIGH | Vcc = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | Vcc = Max.<br>Outputs Open<br>$\overline{OEA}$ or $\overline{OEB}$= GND<br>One Input Toggling<br>50% Duty Cycle | $V_{IN} \geq V_{HC}$<br>$V_{IN} \leq V_{LC}$ | — | 0.15 | 0.25 | mA/ MHz |
| $I_C$ | Total Power Supply Current[6] | Vcc = Max.<br>Outputs Open<br>$f_{CP}$ = 10MHz<br>50% Duty Cycle<br>$\overline{OEA}$ or $\overline{OEB}$= GND<br>One Bit Toggling<br>at fi = 5MHz<br>50% Duty Cycle | $V_{IN} \geq V_{HC}$<br>$V_{IN} \leq V_{LC}$<br>(FCT) | — | 2.0 | 4.0 | mA |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 2.5 | 6.0 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$ = 10MHz<br>50% Duty Cycle<br>$\overline{OEA}$ or $\overline{OEB}$ = GND<br>Eight Bits Toggling<br>at $f_i$ = 2.5MHz<br>50% Duty Cycle | $V_{IN} \geq V_{HC}$<br>$V_{IN} \leq V_{LC}$<br>(FCT) | — | 4.3 | 7.8[5] | |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 6.5 | 16.8[5] | |

2533 tbl 07

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$
   All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[1] | IDT29FCT52A/53A | | | | IDT29FCT52B/53B | | | | IDT29FCT52C/53C | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay CPA, CPB to $A_n$, $B_n$ | $C_L$ = 50pF<br>$R_L$ = 500Ω | 2.0 | 10.0 | 2.0 | 11.0 | 2.0 | 7.5 | 2.0 | 8.0 | 2.0 | 6.3 | 2.0 | 7.3 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to $A_n$ or $B_n$ | | 1.5 | 10.5 | 1.5 | 13.0 | 1.5 | 8.0 | 1.5 | 8.5 | 1.5 | 7.0 | 1.5 | 8.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to $A_n$ or $B_n$ | | 1.5 | 10.0 | 1.5 | 10.0 | 1.5 | 7.5 | 1.5 | 8.0 | 1.5 | 6.5 | 1.5 | 7.5 | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW $A_n$, $B_n$ to CPA, CPB | | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_H$ | Hold Time HIGH or LOW $A_n$, $B_n$ to CPA, CPB | | 2.0 | — | 2.0 | — | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB | | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |
| $t_H$ | Hold Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_W$ | Pulse Width, HIGH[3] or LOW CPA or CPB | | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |

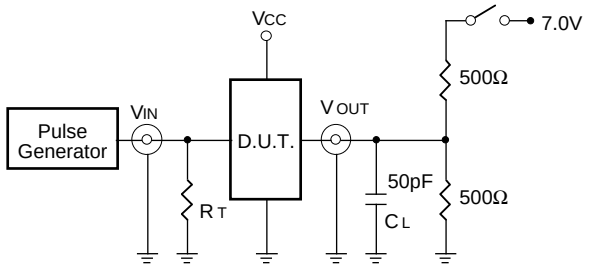
**NOTES:**

2533 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




## SWITCH POSITION

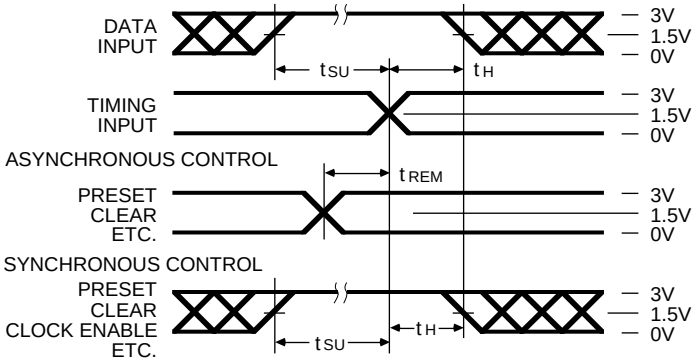
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

2533 tbl 09

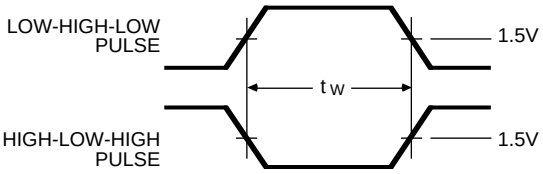
**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

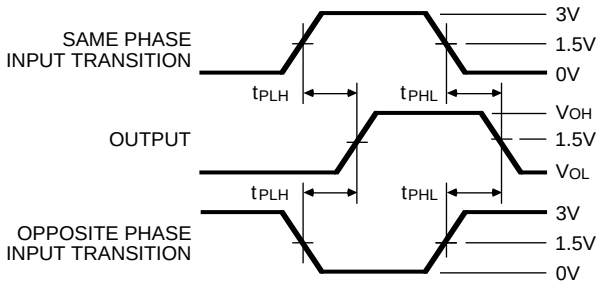
## SET-UP, HOLD AND RELEASE TIMES



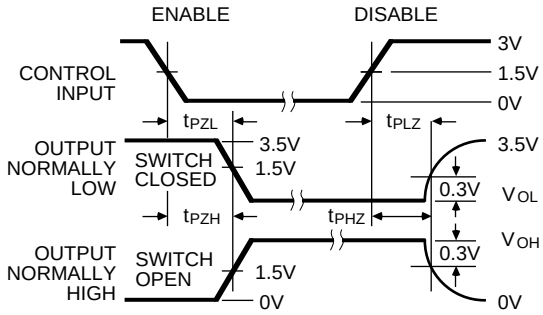

## PULSE WIDTH




## PROPAGATION DELAY




## ENABLE AND DISABLE TIMES

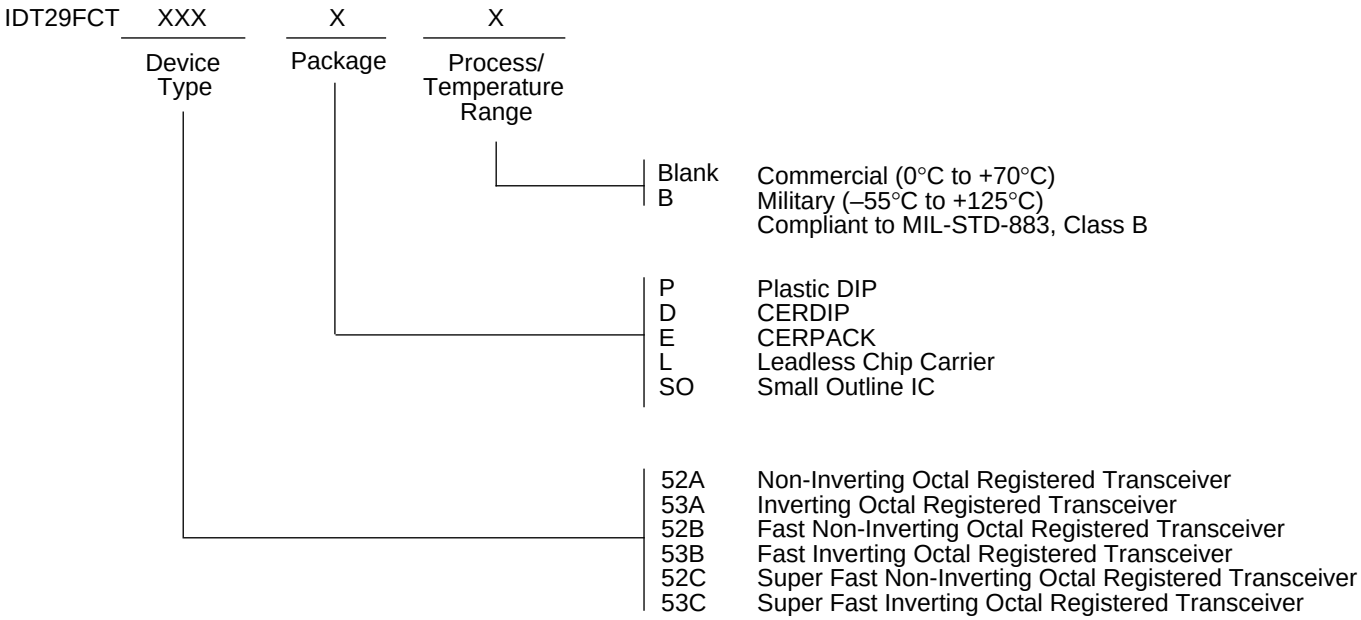



2533 drw 04

**NOTES**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O$ ≤ 50Ω; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.

## ORDERING INFORMATION




2533 drw 03