

Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA without External Pass Transistors

The CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2V to 37V at currents up to 150mA.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150mA and in excess of 10A with the use of suitable NPN or PNP external pass transistors.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0723E	-55 to 125	14 Ld PDIP	E14.3
CA0723T	-55 to 125	10 Pin Can	T10.C
CA0723CE	0 to 70	14 Ld PDIP	E14.3

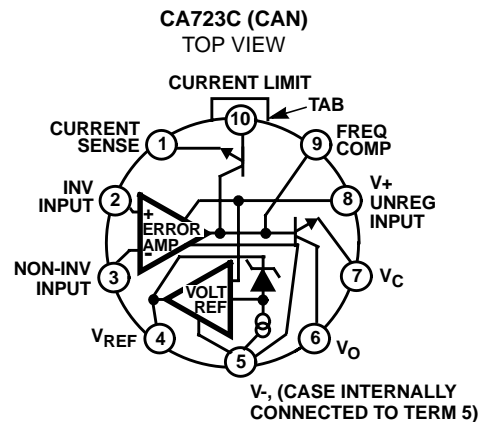
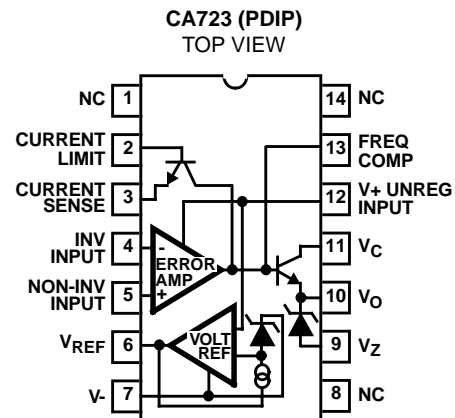
Features

- Up to 150mA Output Current
- Positive and Negative Voltage Regulation
- Regulation in Excess of 10A with Suitable Pass Transistors
- Input and Output Short-Circuit Protection
- Load and Line Regulation0.03%
- Direct Replacement for 723 and 723C Industry Types
- Adjustable Output Voltage 2V to 37V

Applications

- Series and Shunt Voltage Regulator
- Floating Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Temperature Controller

Pinouts



Functional Block Diagram

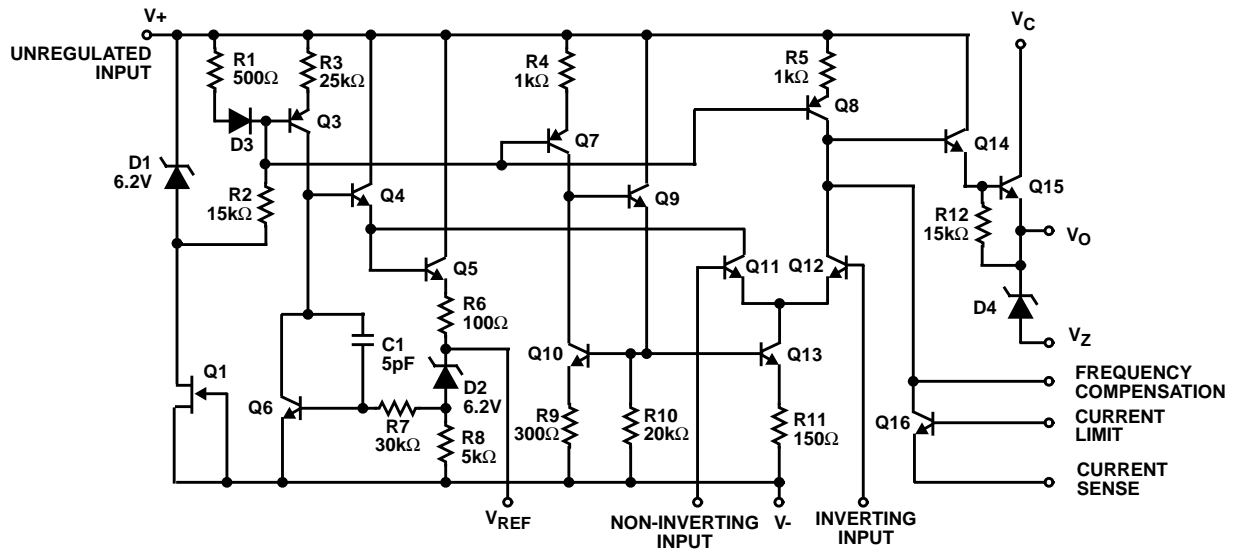
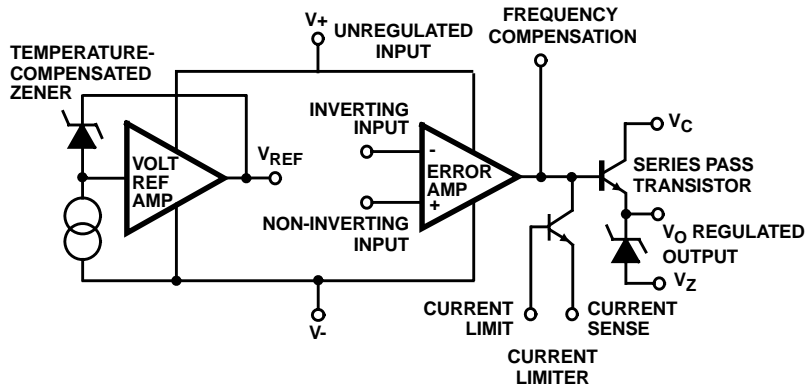


FIGURE 1. EQUIVALENT SCHEMATIC DIAGRAM OF THE CA723 AND CA723C

CA723, CA723C

Absolute Maximum Ratings

DC Supply Voltage40V
(Between V+ and V- Terminals)	
Pulse Voltage for 50ms	
Pulse Width (Between V+ and V- Terminals)50V
Differential Input-Output Voltage40V
Differential Input Voltage	
Between Inverting and Noninverting Inputs	±5V
Between Noninverting Input and V-8V
Current From Zener Diode Terminal (V _Z)	25mA

Operating Conditions

Temperature Range	-55°C to 125°C
-----------------------------	----------------

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	120	N/A
Metal Can	136	65
Device Dissipation		
CA723T, Up to T _A = 25°C900mW	
CA723E, CA723CE, Up to T _A = 25°C	1.000mW	
CA723T, Above T _A = 25°C	7.4mW/°C	
CA723E, CA723CE, Above T _A = 25°C	8.3mW/°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature, During Soldering	265°C	
At a distance 1/16" ± 1/32" (1.59mm ± 0.79mm) from case for 10s Max		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

T_A = 25°C, V+ = V_C = V_I = 12V, V- = 0, V_O = 5V, I_L = 1mA, C₁ = 100pF, C_{REF} = 0, R_{SCP} = 0, Unless Otherwise Specified. Divider impedance R₁ R₂ ÷ R₁ + R₂ at noninverting input, Terminal 5 = 10kΩ. (Figure 20)

PARAMETER	TEST CONDITION	CA723			CA723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Quiescent Regulator Current, I _Q	I _L = 0, V _I = 30V	-	2.3	3.5	-	2.3	4	mA
Input Voltage Range, V _I		9.5	-	40	9.5	-	40	V
Output Voltage Range, V _O		2	-	37	2	-	37	V
Differential Input-Output Voltage, V _I - V _O		3	-	38	3	-	38	V
Reference Voltage, V _{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (Note 2)	V _I = 12V to 40V	-	0.02	0.2	-	0.1	0.5	% V _O
	V _I = 12V to 15V	-	0.01	0.1	-	0.01	0.1	% V _O
	V _I = 12V to 15V, T _A = -55°C to 125°C	-	-	0.3	-	-	-	% V _O
	V _I = 12V to 15V, T _A = 0°C to 70°C	-	-	-	-	-	0.3	% V _O
Load Regulation (Note 2)	I _L = 1mA to 50mA	-	0.03	0.15	-	0.03	0.2	% V _O
	I _L = 1mA to 50mA, T _A = -55°C to 125°C	-	-	0.6	-	-	-	% V _O
	I _L = 1mA to 50mA, T _A = 0°C to 70°C	-	-	-	-	-	0.6	% V _O
Output-Voltage Temperature Coefficient, ΔV _O	T _A = -55°C to 125°C	-	0.002	0.015	-	-	-	%/°C
	T _A = 0°C to 70°C	-	-	-	-	0.003	0.015	%/°C
Ripple Rejection (Note 3)	f = 50Hz to 10kHz	-	74	-	-	74	-	dB
	f = 50Hz to 10kHz, C _{REF} = 5μF	-	86	-	-	86	-	dB
Short Circuit Limiting Current, I _{LIM}	R _{SCP} = 10Ω, V _O = 0	-	65	-	-	65	-	mA

CA723, CA723C

DC Electrical Specifications $T_A = 25^\circ\text{C}$, $V_+ = V_C = V_I = 12\text{V}$, $V_- = 0$, $V_O = 5\text{V}$, $I_L = 1\text{mA}$, $C_1 = 100\text{pF}$, $C_{REF} = 0$, $R_{SCP} = 0$, Unless Otherwise Specified. Divider impedance $R_1 R_2 \div R_1 + R_2$ at noninverting input, Terminal 5 = $10\text{k}\Omega$. (Figure 20) **(Continued)**

PARAMETER	TEST CONDITION	CA723			CA723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Equivalent Noise RMS Output Voltage, V_N (Note 3)	$BW = 100\text{Hz to } 10\text{kHz}$, $C_{REF} = 0$	-	-20	-	-	20	-	μV
	$BW = 100\text{Hz to } 10\text{kHz}$, $C_{REF} = 5\mu\text{F}$	-	2.5	-	-	2.5	-	μV

NOTES:

- Line and load regulation specifications are given for condition of a constant chip temperature. For high dissipation condition, temperature drifts must be separately taken into account.
- For C_{REF} (See Figure 20)

Typical Performance Curves (CA723)

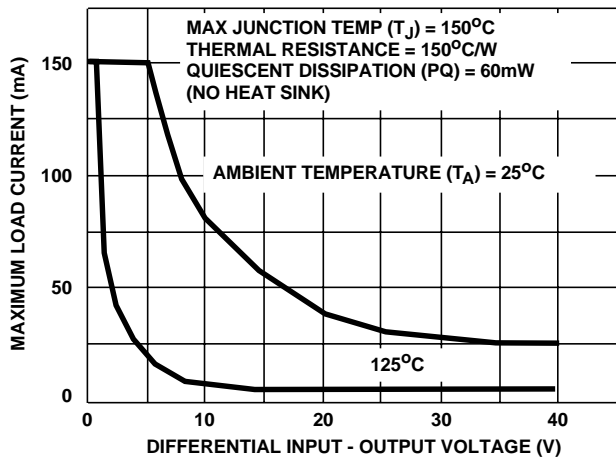


FIGURE 2. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

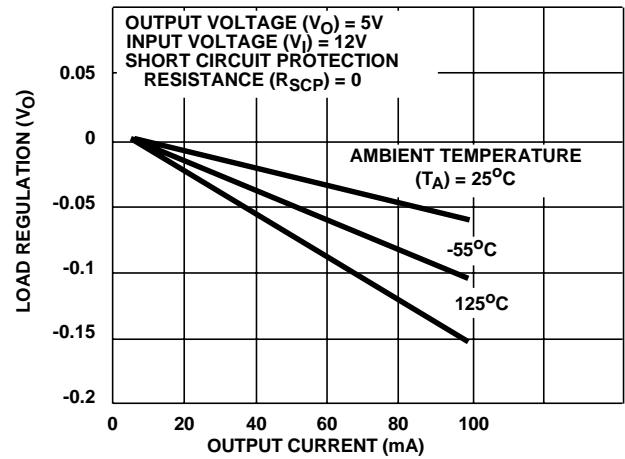


FIGURE 3. LOAD REGULATION WITHOUT CURRENT LIMITING

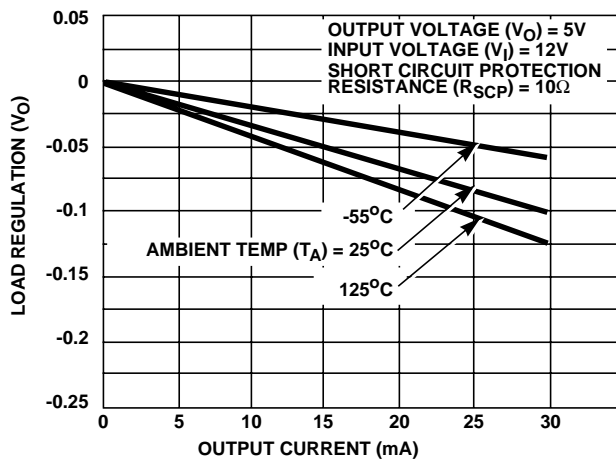


FIGURE 4. LOAD REGULATION WITH CURRENT LIMITING

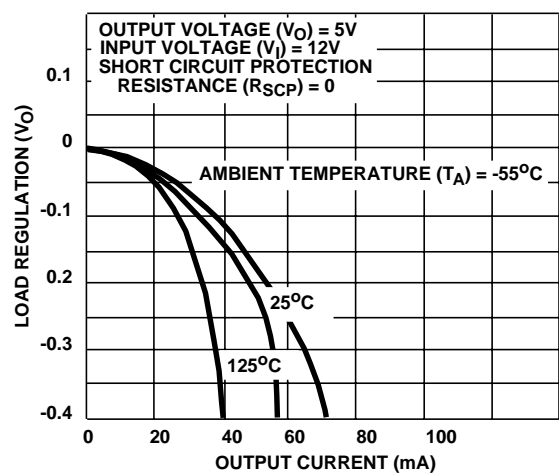


FIGURE 5. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

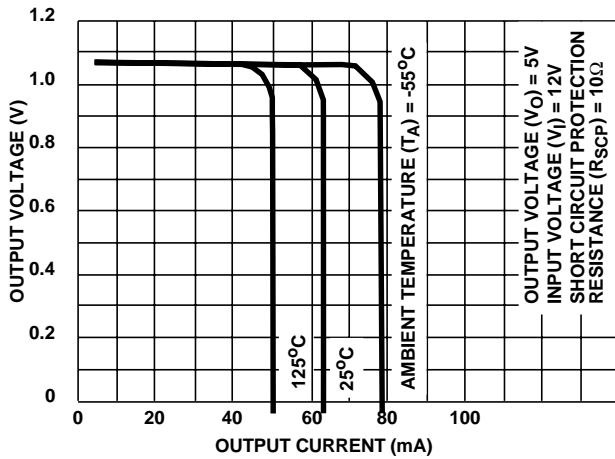


FIGURE 6. CURRENT LIMITING CHARACTERISTICS

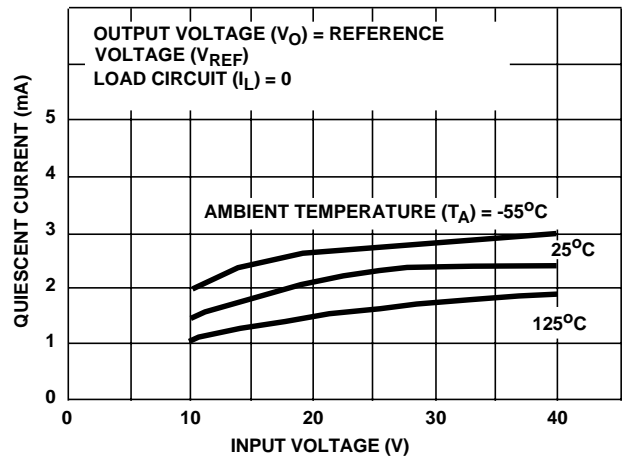


FIGURE 7. QUIESCENT CURRENT vs INPUT VOLTAGE

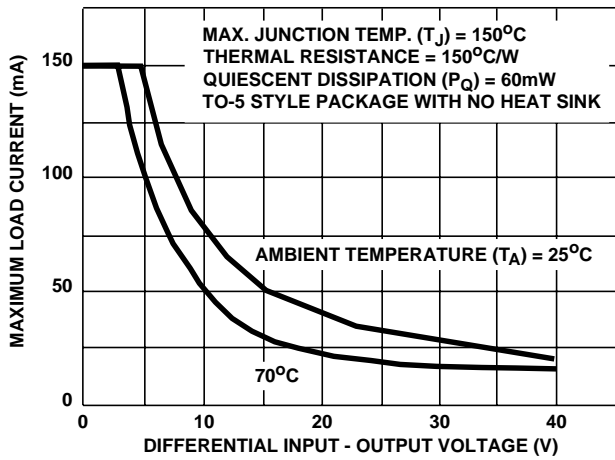


FIGURE 8. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

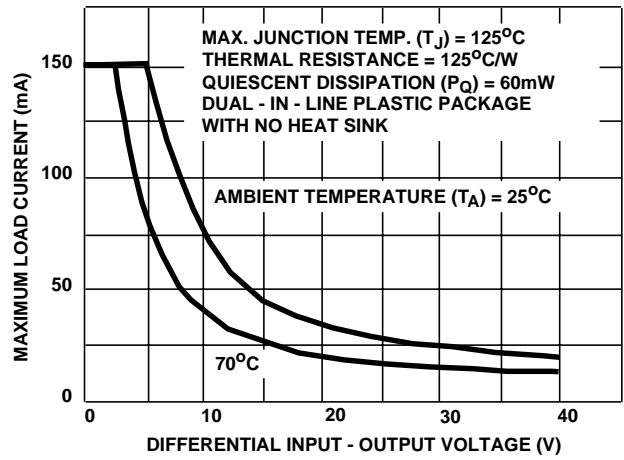


FIGURE 9. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE FOR CA723CE

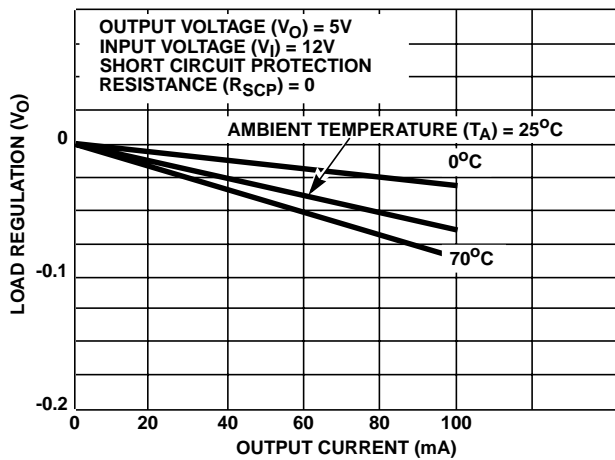


FIGURE 10. LOAD REGULATION WITHOUT CURRENT LIMITING

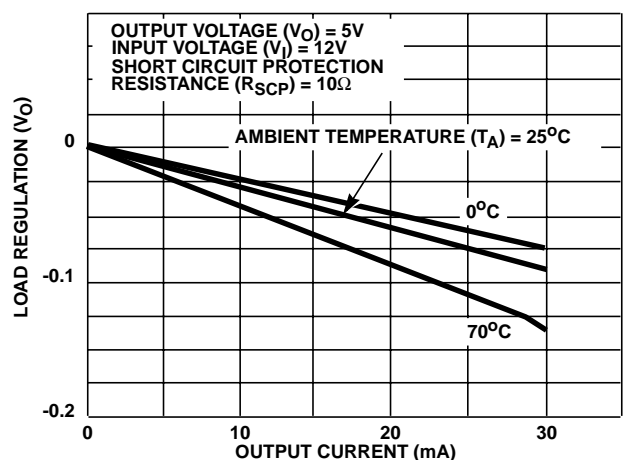


FIGURE 11. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

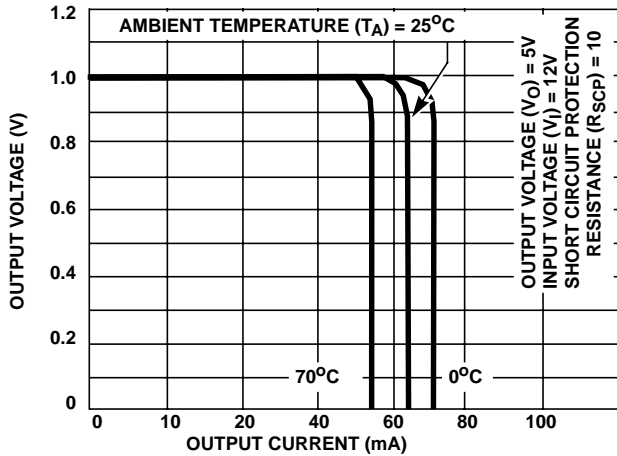


FIGURE 12. CURRENT LIMITING CHARACTERISTICS

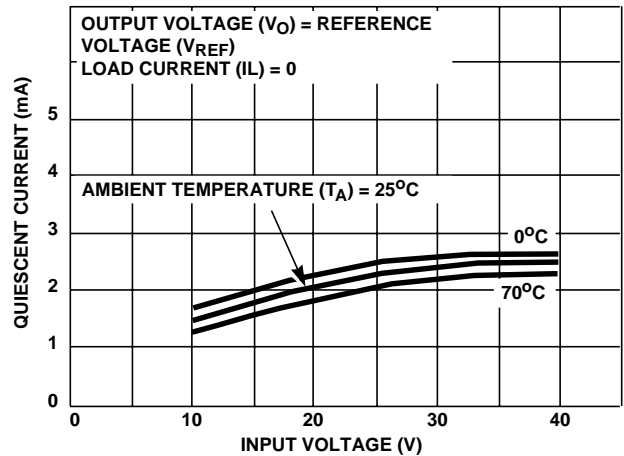


FIGURE 13. QUIESCENT CURRENT vs INPUT VOLTAGE

Typical Performance Curves (CA723 and CA723C)

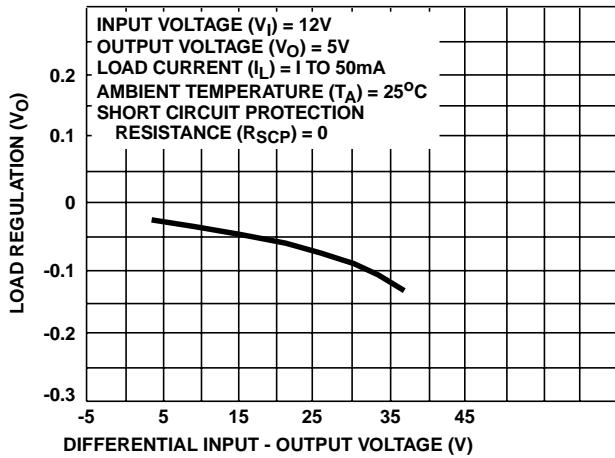


FIGURE 14. LOAD REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

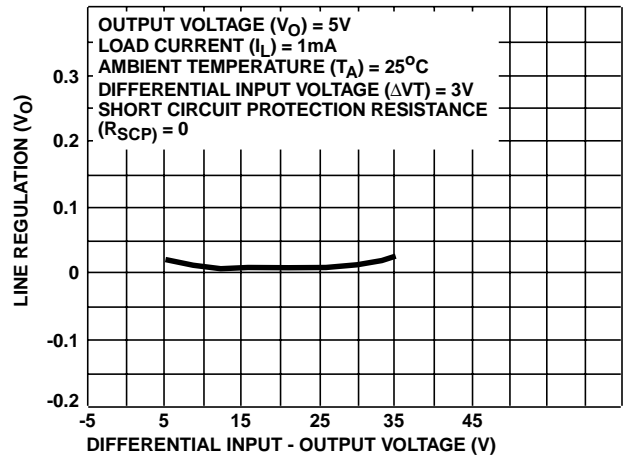


FIGURE 15. LINE REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

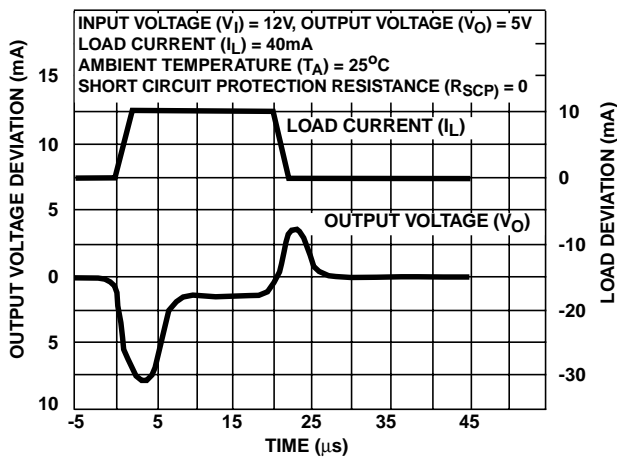


FIGURE 16. LINE TRANSIENT RESPONSE

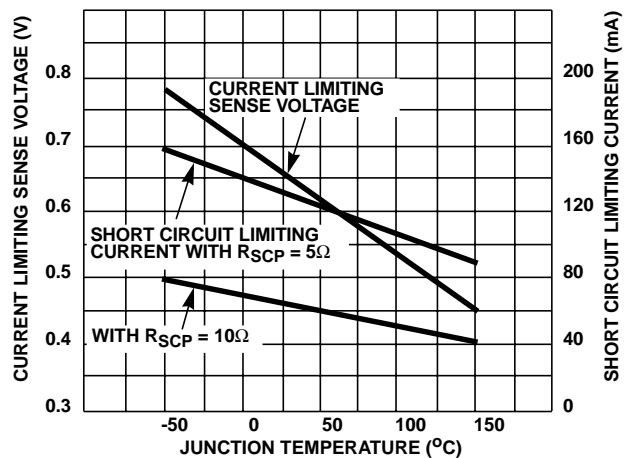


FIGURE 17. CURRENT LIMITING CHARACTERISTIC vs JUNCTION TEMPERATURE

Typical Performance Curves (CA723 and CA723C) (Continued)

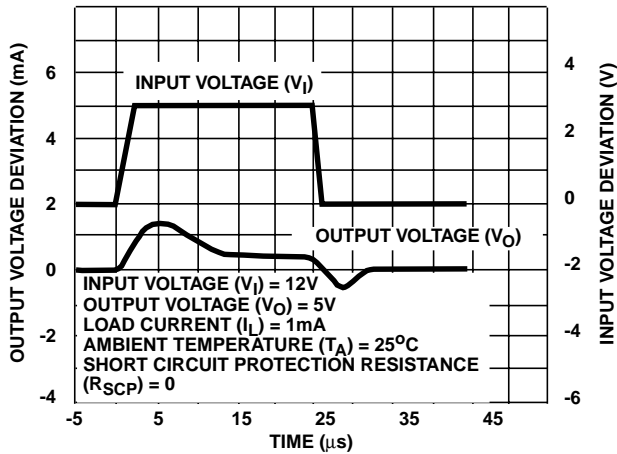


FIGURE 18. LOAD TRANSIENT RESPONSE

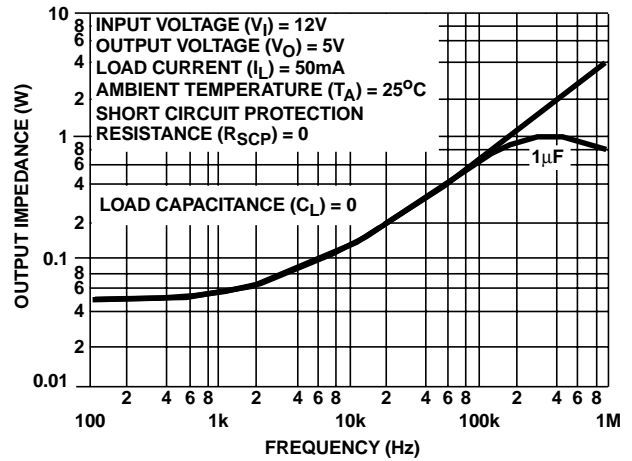
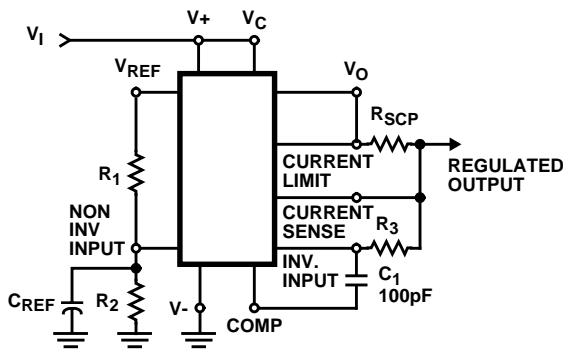


FIGURE 19. OUTPUT IMPEDANCE vs FREQUENCY

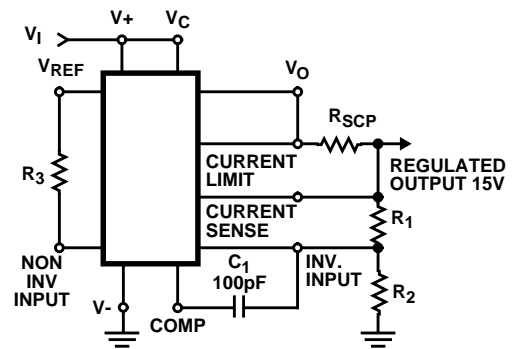
Typical Application Circuits



Circuit Performance Data:
 Regulated Output Voltage 5V
 Line Regulation ($\Delta V_1 = 3V$) 0.5mV
 Load Regulation ($\Delta I_L = 50mA$) 1.5mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ For Minimum Temperature Drift

FIGURE 20. LOW VOLTAGE REGULATOR CIRCUIT (V_O = 2V TO 7V)



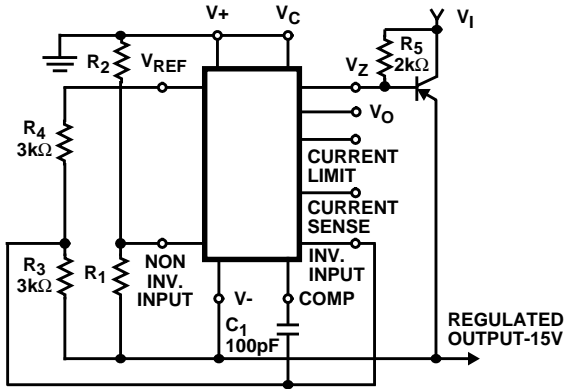
Circuit Performance Data:
 Line Regulation ($\Delta V_1 = 3V$) 1.5mV
 Load Regulation ($\Delta I_L = 50mA$) 4.5mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ For Minimum Temperature Drift

R₃ May Be Eliminated For Minimum Component Count

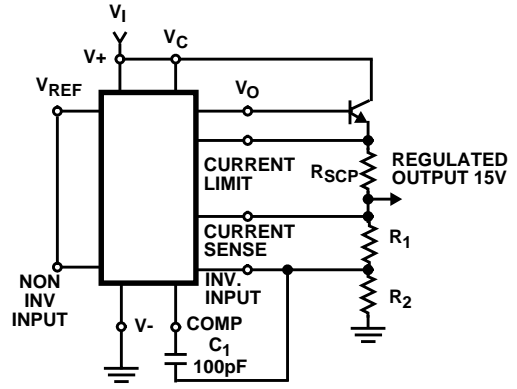
FIGURE 21. HIGH VOLTAGE REGULATOR CIRCUIT (V_O = 7V TO 37V)

Typical Application Circuits (Continued)



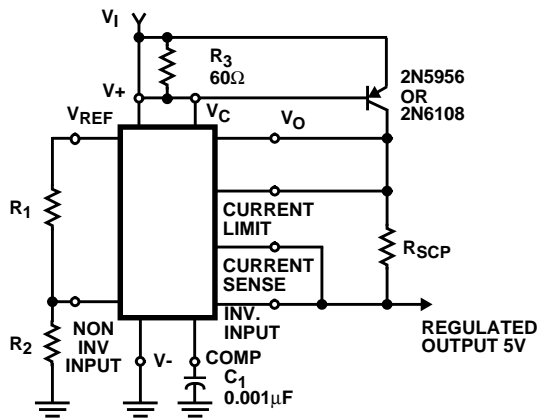
Circuit Performance Data:
 Line Regulation ($\Delta V_I = 3V$) 1mV
 Load Regulation ($\Delta I_L = 100mA$) 2mV
 Note: For Applications Employing the TO-5 Style Package and Where V_Z Is Required, An External; 6.2V Zener Diode Should be Connected in Series with V_O (Terminal 6).

FIGURE 22. NEGATIVE VOLTAGE REGULATOR CIRCUIT



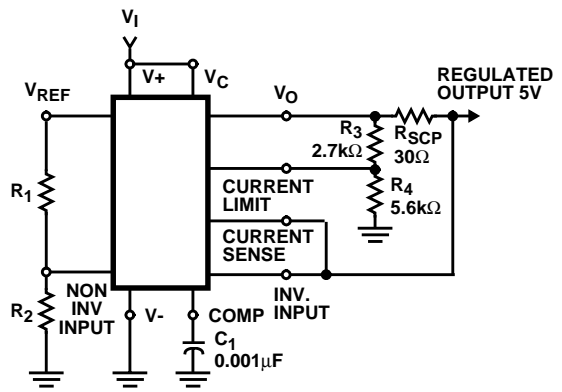
Circuit Performance Data:
 Line Regulation ($\Delta V_I = 3V$) 1.5mV
 Load Regulation ($\Delta I_L = 1A$) 15mV

FIGURE 23. POSITIVE VOLTAGE REGULATOR CIRCUIT (WITH EXTERNAL NPN PASS TRANSISTOR)



Circuit Performance Data:
 Line Regulation ($\Delta V_I = 3V$) 0.5mV
 Load Regulation ($\Delta I_L = 1A$) 5mV

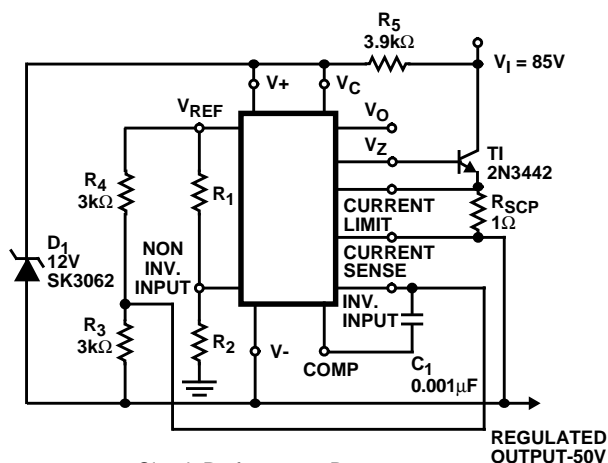
FIGURE 24. POSITIVE VOLTAGE REGULATOR CIRCUIT (WITH EXTERNAL PNP PASS TRANSISTOR)



Circuit Performance Data:
 Line Regulation ($\Delta V = 3V$) 0.5mV
 Load Regulation ($\Delta I_L = 10mA$) 1mV
 Short Circuit Current 20mA

FIGURE 25. FOLDBACK CURRENT LIMITING CIRCUIT

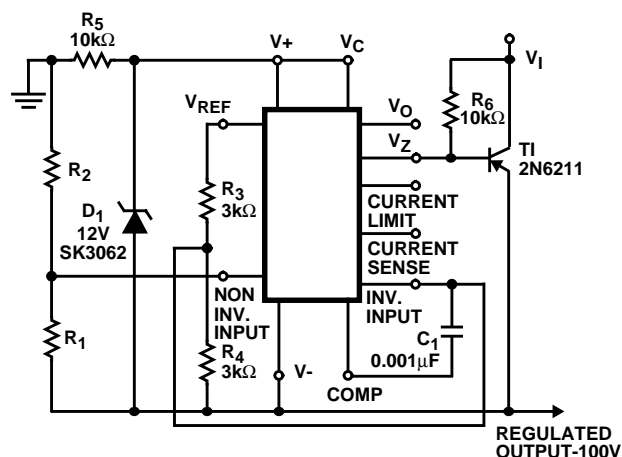
Typical Application Circuits (Continued)



Circuit Performance Data:
 Line Regulation ($\Delta V = 20V$) 15mV
 Load Regulation ($\Delta I_L = 50mA$) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

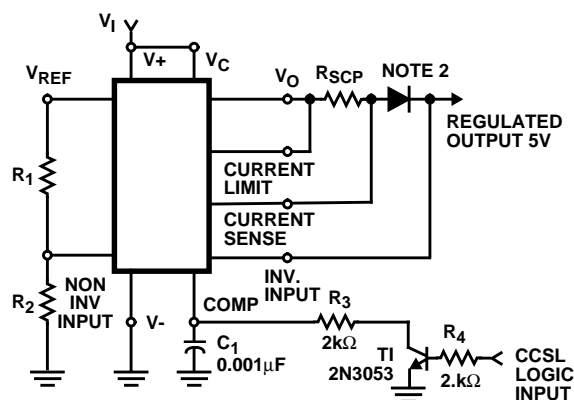
FIGURE 26. POSITIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
 Line Regulation ($\Delta V_1 = 20V$) 30mV
 Load Regulation ($\Delta I_L = 100mA$) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

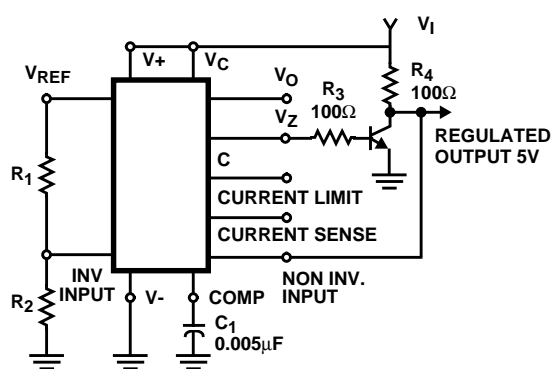
FIGURE 27. NEGATIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
 Line Regulation ($\Delta V_1 = 3V$) 0.5mV
 Load Regulation ($\Delta I_L = 50mA$) 1.5mV
 Short Circuit Current 20mA

NOTE: 1. A current limiting transistor may be used for shutdown if current limiting is not required.
 2. Add a diode if $V_O > 10V$.

FIGURE 28. REMOTE SHUTDOWN REGULATOR CIRCUIT WITH CURRENT LIMITING



Circuit Performance Data:
 Line Regulation ($\Delta V_1 = 10V$) 0.5mV
 Load Regulation ($\Delta I_L = 100mA$) 1.5mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6).

FIGURE 29. SHUNT REGULATOR CIRCUIT

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>